

**Evaluating the LTC3302A, 3.3 V to 1.2 V at 2 A, 2 MHz Synchronous Step-Down Regulator in a 2 mm × 2 mm SWF FCQFN****FEATURES**

- ▶ LTC3302A evaluation board
- ▶ Transient circuit included for load-transient evaluation
- ▶ EMI filter included to reduce noise in EMI emission tests

**EVALUATION KIT CONTENTS**

- ▶ DC3251A evaluation board

**DOCUMENTS NEEDED**

- ▶ LTC3302A data sheet

**EQUIPMENT NEEDED**

- ▶ One 5 V, 2 A, DC power supply
- ▶ One 2 A, Electronic load
- ▶ Three digital voltmeters
- ▶ Two digital ammeters

**GENERAL DESCRIPTION**

Demonstration Circuit DC3251A features the LTC3302A, 5 V, 2 A synchronous step-down silent switcher operating as a 2 MHz, 3.3 V to 1.2 V, 2 A buck regulator. The LTC3302A supports adjustable output voltages from 0.5 V to  $V_{IN}$ . The LTC3302A is a compact, high efficiency, and high-speed synchronous monolithic step-down switching regulator. A minimum on-time of 27 ns enables high  $V_{IN}$  to low  $V_{OUT}$  conversion.

The DC3251A operating mode can be selected as Burst Mode operation, skip (PS) or forced continuous (FC) mode. Setting JP1 to the SKIP position allows the LTC3302A to sync to a clock frequency from 1.6 MHz to 2.4 MHz. The LTC3302A operates in forced continuous mode when syncing to an external clock.

The DC3251A also has an EMI filter to reduce conducted EMI. This EMI filter can be included by applying the input voltage at the  $V_{IN}$  EMI terminal. The EMI performance of the board is shown in the [EMI Test Results](#) section. The red lines in the EMI performance graphs show the CISPR25 Class 5 peak limits for the conducted and radiated emission tests.

The LTC3302A data sheet gives a complete description of the device, operation, and application information. Full specifications on the LTC3302A are available in the LTC3302A data sheet available from Analog Devices, Inc., and must be consulted with this user guide when using the DC3251A evaluation board. The LTC3302A is assembled in a 2 mm × 2 mm FCQFN package with side wettable flanks (SWF) for visual solder inspection. The layout recommendations for low EMI operation and maximum thermal performance are available in the data sheet section Low EMI PCB Layout.

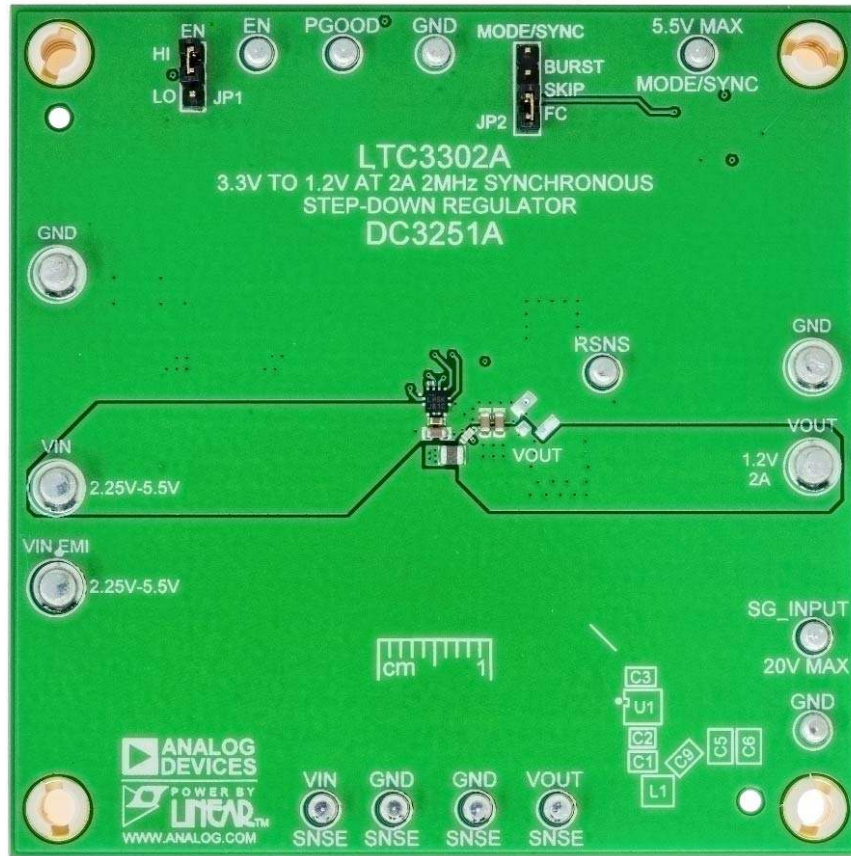
[Figure 7](#) shows the efficiency and the power loss of the circuit with a 3.3 V input in Burst Mode operation.

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**REVISION HISTORY****3/2023—Revision 0: Initial Version**

DC3251A EVALUATION BOARD PHOTOGRAPH



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Figure 1. DC3251A Evaluation Board Photograph

**PERFORMANCE SUMMARY**

Specifications are at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 1. Performance Summary**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VOLTAGE RANGE						
Input	$V_{IN}$		2.25		5.5	V
Output <sup>1</sup>	$V_{OUT}$		1.183	1.2	1.217	V
OUTPUT CURRENT	$I_{OUT}$		2			A
SWITCHING FREQUENCY	$f_{SW}$	$V_{IN} > V_{OUT}$	1.6	2.0	2.4	MHz
TOP SWITCH MINIMUM ON-TIME	$t_{ON}$			27		ns
TOP SWITCH DUTY CYCLE			100			%

<sup>1</sup> With 1% resistors. Accuracy improves to within 1% using 0.1% FB resistors or a fixed voltage version of the [LTC3302A](#).

## QUICK START PROCEDURE

Demonstration circuit DC3251A is easy to set up and use to evaluate the performance of the [LTC3302A](#). For the proper measurement equipment setup, see [Figure 3](#) and follow the procedure below:

NOTE: For accurate  $V_{IN}$ ,  $V_{OUT}$ , and efficiency measurements, measure  $V_{IN}$  at the  $V_{IN}$  SNSE and GND SNSE turrets, and  $V_{OUT}$  at the  $V_{OUT}$  SNSE and GND SNSE turrets as shown as VM1 and VM2 in [Figure 3](#). When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the output voltage ripple by touching the probe tip directly across the output turrets or to TP1 as shown in [Figure 4](#). TP1 is designed for a 50  $\Omega$  coax cable to reduce any high frequency noise that might couple into the oscilloscope probes.

- Set the JP1 Jumper to the SKIP position and JP2 to the HI position.
- With power off, connect the input power supply to  $V_{IN}$  and GND. If the input EMI filter is required, connect the input power supply to  $V_{IN}$  EMI.
- Slowly increase PS1 to 1.0 V. If AM1 reads less than 20 mA, increase PS1 to 3.3 V. Verify that VM1 reads 3.3 V and VM2 reads 1.2 V.
- Connect an oscilloscope voltage probe as shown in [Figure 4](#) in parallel with VM2. Set Channel to AC-coupled, voltage scale to 20 mV and time base to 10  $\mu$ s. Observe the  $V_{OUT}$  ripple voltage.
- Verify that PGOOD turret is above 1 V.
- Increasing the load by 1 A intervals up to 2 A and record VM1, VM2, AM1, and AM2 for each interval.
- Repeat step 6 for PS1 set to 2.5 V and again for PS1 set to 5.0 V.
- Set the load to a constant 1 A. Remove the oscilloscope voltage probe from  $V_{OUT}$ . Place a ground clip on PGND terminal and set the voltage scale to 1 V and the time scale to 500 ns/Division. Trigger on the rising edge of the voltage probe. Using a tip on the voltage probe, contact the SW node on the pad of L1. Observe the duty cycle and the period of the switching waveform (~500 ns).
- Set the load current to 0.1 A and repeat step 8. Observe that the switching waveform is now operating in pulse skip mode.
- Move the jumper on JP2 to LO. Verify that  $V_{OUT}$  reads 0 V and verify that PGOOD is low. Return jumper on JP2 to HI and verify that VM2 is 1.2 V and verify that PGOOD is above 1 V.
- If forced continuous or Burst Mode is required, set PS1 to 0 V. Move JP1 to FC or BURST. Repeat steps 3 through 9. In step 9, observe that the switching waveform is now operating in forced continuous or Burst Mode.
- To test the transient response with a base load, add the required resistor to produce a minimum load between  $V_{OUT}$  and RSNS turrets (RL shown on [Figure 3](#)). Note that the total load resistance is RL plus R8 (100 m $\Omega$ ).
- Adjust a signal generator with a 10 ms period, 10% duty cycle, and an amplitude from 1 V to 2 V to start.
- Measure the RSNS voltage to observe the current,  $V_{RSNS}/100$  m $\Omega$ . Adjust the amplitude of the pulse to provide the required transient. Adjust the rising and falling edge of the pulse to provide the required ramp rate. For more details, see [Figure 9](#) and the optional transient response circuit shown in [Figure 6](#).
 
$$I_{OUT} = V_{RSNS}/100m\Omega \quad (1)$$
- When done, turn off PS1 and Load. Remove all connections to the demo board.

QUICK START PROCEDURE

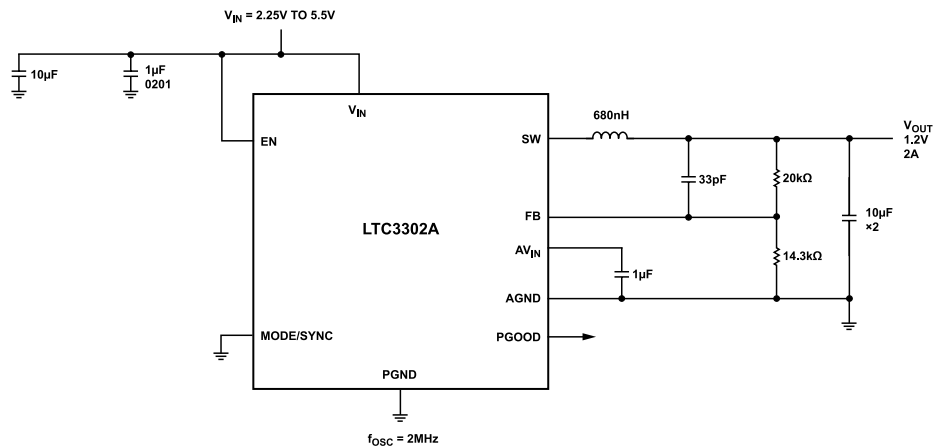


Figure 2. DC3251A Simplified Schematic

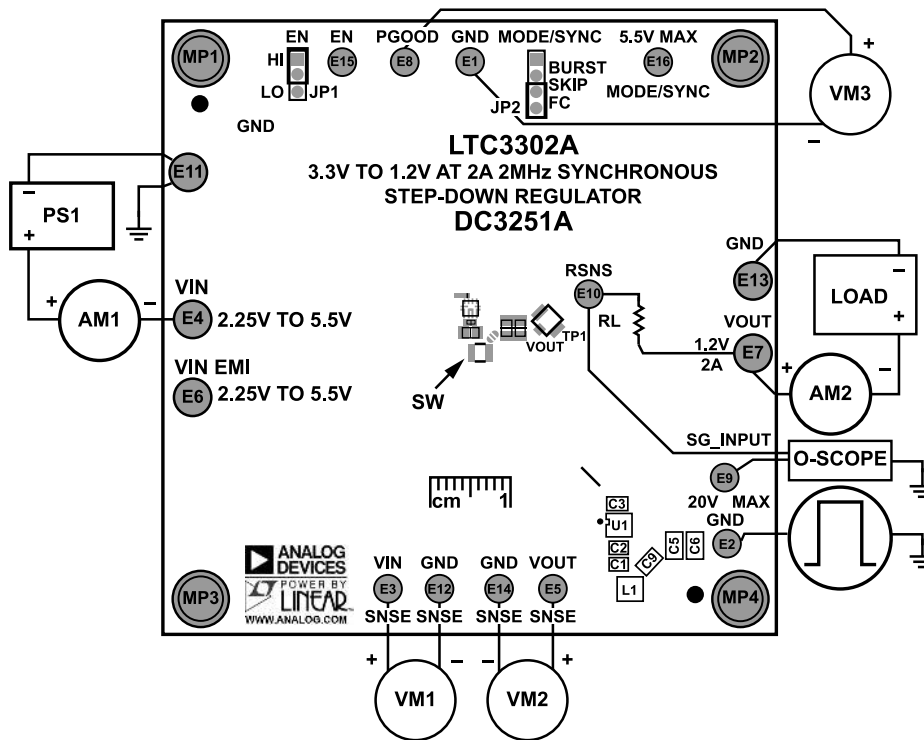


Figure 3. Test Setup for the DC3251A Demo Board

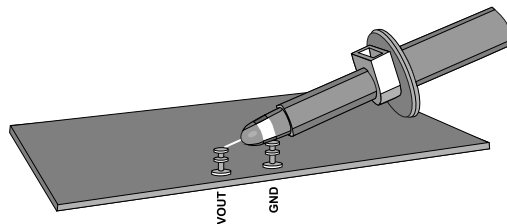
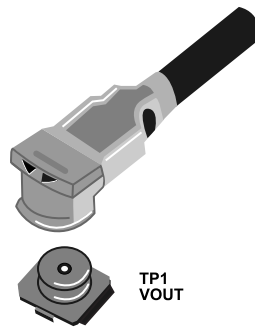


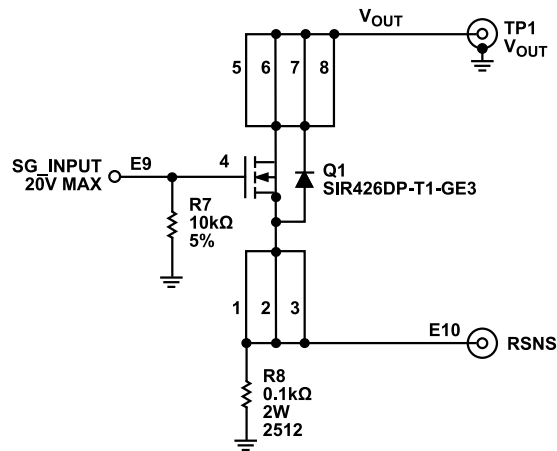
Figure 4. Technique for Measuring Output Ripple and Step Response with a Scope Probe

QUICK START PROCEDURE



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Figure 5. Technique for Measuring Output Ripple and Step Response with a Low Inductance Connector (Not Supplied)



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Figure 6. Optional Transient Response Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

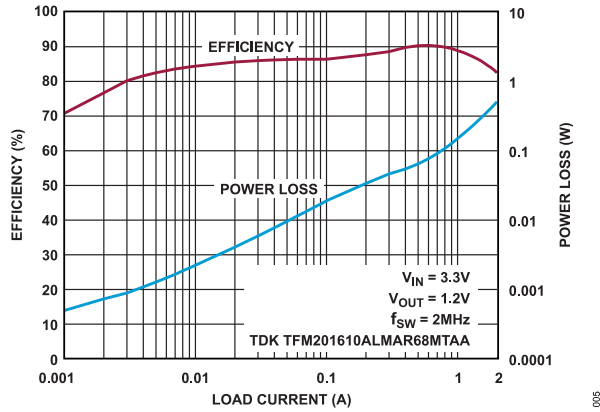


Figure 7. Efficiency and Power Loss in Burst Mode Operation

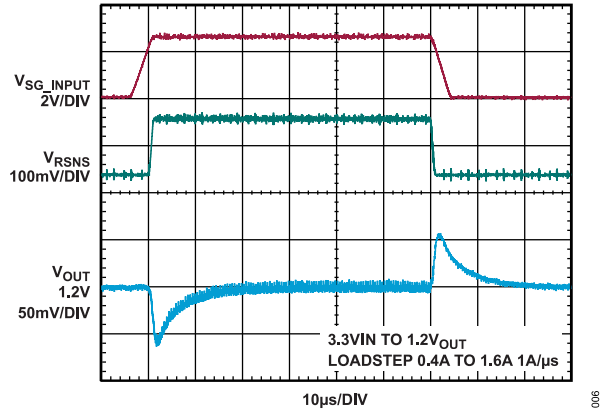


Figure 9. Load Transient Response Forced Continuous Mode

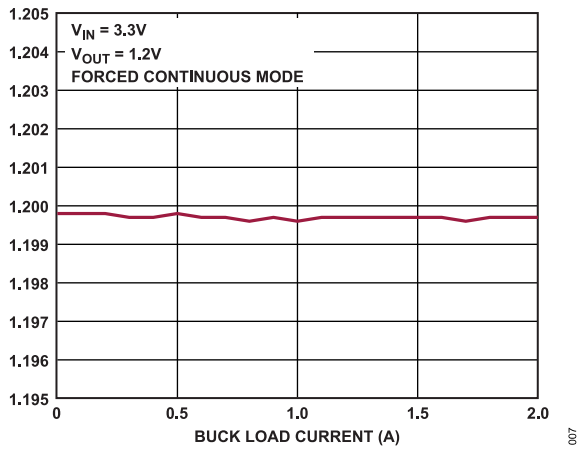


Figure 8. Buck Load Regulation



EMI TEST RESULTS

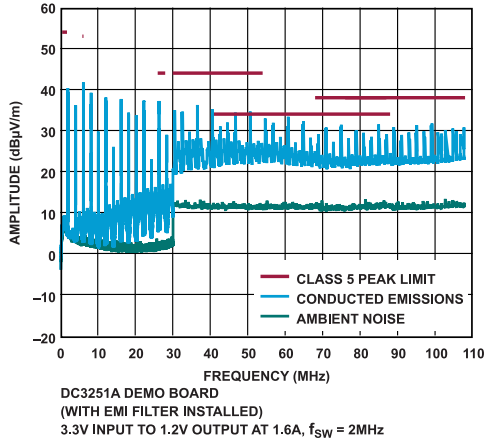


Figure 10. Conducted EMI Performance (CISPR25 Conducted Emission Test with Class 5 Peak Limits)

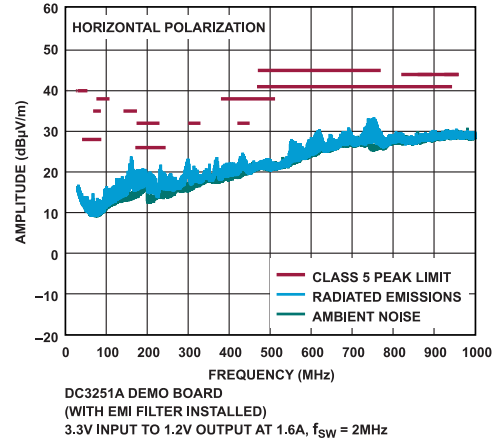


Figure 12. Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits, Horizontal)

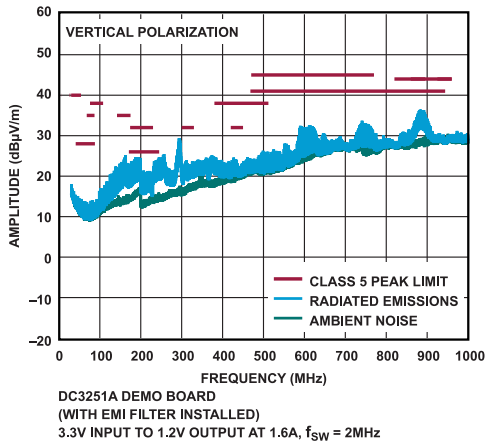


Figure 11. Radiated EMI Performance (CISPR25 Radiated Emission Test with Class 5 Peak Limits, Vertical)

## EVALUATION BOARD HARDWARE

## INTRODUCTION TO THE DC3251A

The DC3251A demonstration circuit features the [LTC3302A](#), a low voltage synchronous step-down regulator. The LTC3302A is a monolithic, constant frequency, current mode step-down DC-DC converter. A 2 MHz oscillator turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch comparator trips and turns off the top power switch. If the EN pin is low, the LTC3302A is in shutdown and in a low quiescent current state. When the EN pin is above its threshold, the switching regulator is enabled.

The MODE/SYNC pin sets the switching mode to pulse skip, forced continuous, or Burst Mode. If an external 1.6 MHz to 2.4 MHz clock is connected to the MODE/SYNC turret while the JP1 is set to the SKIP position, the LTC3302A switching frequency sync to the external clock. The LTC3302A operates in forced continuous mode while syncing. For more detailed information, refer to the LTC3302A data sheet.

## ACCURATELY MEASURING OUTPUT RIPPLE OF THE LTC3302A

With the fast edge rates of the circuit, high frequency noise can be observed when measuring the output voltage with 1 M $\Omega$  terminated oscilloscope probes. To better view the output ripple with oscilloscopes of 400 MHz bandwidth and above a 50  $\Omega$  coax cable connected as close to the output caps as possible should be used with the oscilloscope channel terminated to 50  $\Omega$  at the scope. This helps to reduce the noise coupling onto and displaying on the scope. The demo board is set up to solder an U.FL, RECEPT, ST SMD, 0 Hz to 6 GHz, 50  $\Omega$  connector (TP1) near the output cap C6. These pads can also be used to solder a coax cable or other oscilloscope probe connector if required.

The high frequency spikes are partially attributed to the inter-winding capacitance of the inductor and the voltage step is partially attributed to the inductance in the output capacitors. This can be reduced by choosing low ESL capacitors or adding small low ESL capacitors in parallel to the output capacitors as close to the inductor as possible. [Figure 13](#) and [Figure 14](#) show the output ripple using a 500 MHz scope, 50  $\Omega$  probe with an added low ESL X2Y capacitor added, C9, close to the inductor and GND return to the input capacitors to reduce the inductance of the return path and better filter the high frequency spikes.

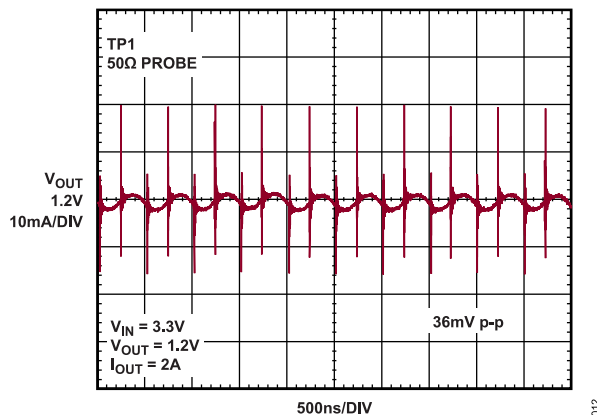


Figure 13. V<sub>OUT</sub> Ripple Without C9 X2Y Capacitor

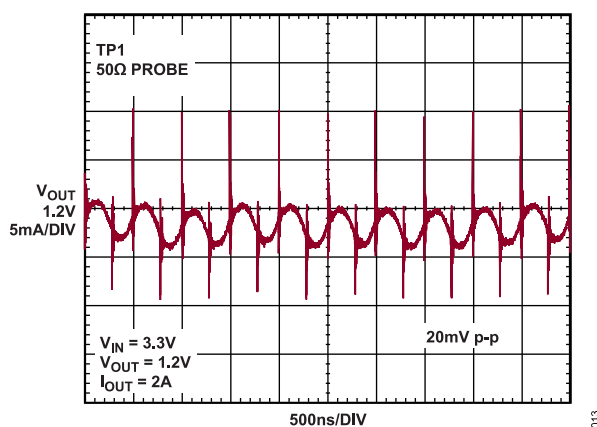


Figure 14. V<sub>OUT</sub> Ripple with C9 X2Y Capacitor

EVALUATION BOARD SCHEMATIC

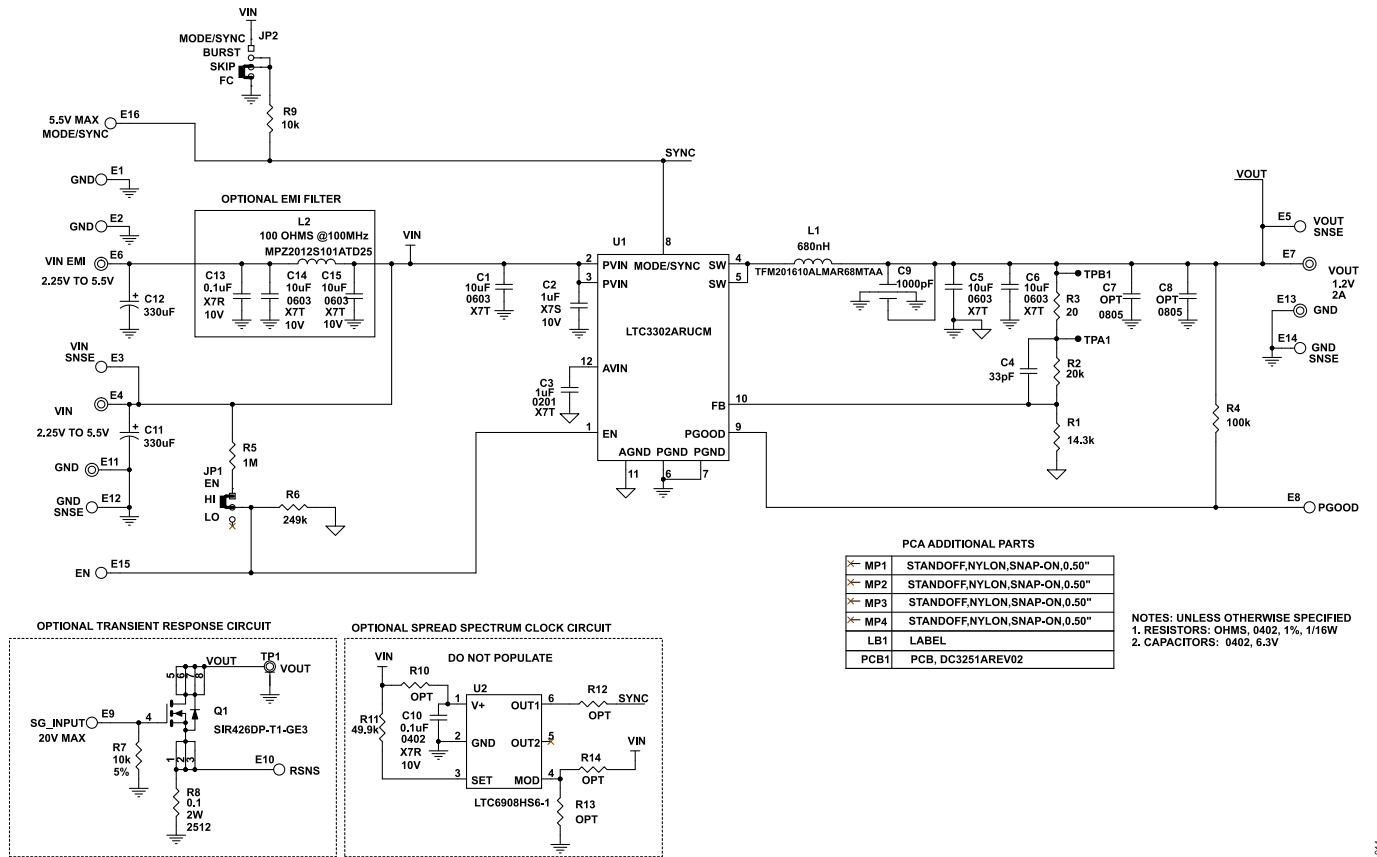


Figure 15. DC3251A Schematic Diagram

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 2. DC3251A Bill of Materials

Item	Quantity	Reference Designator	Part Description	Manufacturer, Part Number
<b>Required Circuit Components</b>				
1	3	C1, C5, C6	Capacitors, 10 $\mu$ F, X7T, 10 V, 20%, 0603, AEC-Q200	Murata, GRT188D71A106ME13D
2	1	C2	Capacitor, 1 $\mu$ F, X7S, 10 V, 10%, 0402, AEC-Q200, no substitutes allowed	Murata, GCM155C71A105KE38D
3	1	C3	Capacitor, 1 $\mu$ F, X7T, 6.3 V, 20%, 0201, AEC-Q200	Murata, GRT033D70J105ME13D
4	1	C4	Capacitor, 33 pF, C0G, 50 V, 5%, 0402	AVX, 04025A330JAT2A
5	1	L1	Inductor, 680 nH, power, 20%, 4.3 A, 53 m $\Omega$ , 0806, AEC-Q200	TDK, TFM201610ALMAR68MTAA
		L1 (Alternate)	Inductor, 680 nH, power, 20%, 2 A, 65 m $\Omega$ , 0806, AEC-Q200	Würth, 744383430068
6	1	Q1	Transistor, N-MOSFET, 40 V, 15.9 A, PPAK SO-8	Vishay, SIR426DP-T1-GE3
7	1	R1	Resistor, 14.3 k $\Omega$ , 1%, 1/16 W, 0402	Vishay, CRCW040214K3FKED
8	1	R2	Resistor, 20 k $\Omega$ , 1%, 1/16 W, 0402, AEC-Q200	NIC, NRC04F2002TRF
9	1	U1	IC, 5 V, 2 A, 2 MHz, synchronous step-down regulator	Analog Devices Inc., <a href="#">LTC3302ARUCM#TRPBF</a>
<b>Additional Demo Board Circuit Components</b>				
1	0	C7, C8	Capacitors, option, 0805	Not applicable
2	1	C9	Capacitor, 1000 pF, X7R, 50 V, 20%, 0402, 3-Term, X2Y EMI filter	Johanson Dielectrics, 500X07W102MV4T
3	0	C10	Capacitor, 0.1 $\mu$ F, X7R, 10 V, 10%, 0402, AEC-Q200	Murata, GCM155R71A104KA55D
4	2	C11, C12	Capacitors, 330 $\mu$ F, Tantalum, POSCAP TPE, 6.3 V, 20%, 7343, 25 m $\Omega$	Panasonic, 6TPE330ML
5	1	C13	Capacitor, 0.1 $\mu$ F, X7R, 10 V, 10%, 0402, AEC-Q200	Murata, GCM155R71A104KA55D
6	2	C14, C15	Capacitors, 10 $\mu$ F, X7T, 10 V, 20%, 0603, AEC-Q200	Murata, GRT188D71A106ME13D
7	1	L2	Inductor, ferrite bead, 100 $\Omega$ at 100 MHz, 25%, 4 A, 20 m $\Omega$ , 0805, AEC-Q200	TDK, MPZ2012S101ATD25
8	1	R3	Resistor, 20 $\Omega$ , 1%, 1/16 W, 0402, AEC-Q200	NIC, NRC04F20R0TRF
9	1	R4	Resistor, 100 k $\Omega$ , 5%, 1/16 W, 0402	Yageo, RC0402JR-07100KL
10	1	R5	Resistor, 1 m $\Omega$ , 1%, 1/16 W, 0402, AEC-Q200	Stackpole Electronics Inc., RMCF0402FT1M00
11	1	R6	Resistor, 249 k $\Omega$ , 1%, 1/16 W, 0402, AEC-Q200	NIC, NRC04F2493TRF
12	1	R7	Resistor, 10 k $\Omega$ , 5%, 1/10 W, 0402, AEC-Q200	Panasonic, ERJ2GEJ103X
13	1	R8	Resistor, 0.1 $\Omega$ , 1%, 2 W, 2512, sense, AEC-Q200	TT Electronics, LRC-LR2512LF-01-R100-F
14	1	R9	Resistor, 10 k $\Omega$ , 5%, 1/16 W, 0402, AEC-Q200	NIC, NRC04J103TRF
15	0	R10, R12 to R14	Resistors, option, 0402	Not applicable
16	0	R11	Resistor, 49.9 k $\Omega$ , 1%, 1/16 W, 0402, AEC-Q200	NIC, NRC04F4992TRF
17	0	TP1	Connector, U.FL, RCPT, male, ST, 3.0 mm $\times$ 3.1 mm, SMD, 50 $\Omega$	Hirose Electric, U.FL-R-SMT-1(10)

## ORDERING INFORMATION

Table 2. DC3251A Bill of Materials (Continued)

Item	Quantity	Reference Designator	Part Description	Manufacturer, Part Number
18	0	U2	IC, oscillator silicon programmable, TSOT-23-6	Analog Devices Inc., LTC6908HS6-1#TRMPBF
Hardware				
1	11	E1 to E3, E5, E8 to E10, E12, E14 to E16	Test points, turret, 0.064" mounting hole diameter, PCB 0.062" thickness	Mill-Max, 2308-2-00-80-00-00-07-0
2	5	E4, E6, E7, E11, E13	Test points, turret, 0.094" mounting hole diameter, PCB 0.062" thickness	Mill-Max, 2501-2-00-80-00-00-07-0
3	1	JP1	Connector, HDR, male, 1 × 3, 2 mm, vertical, straight, THT	Würth Elektronik, 62000311121
4	1	JP2	Connector, HDR, male, 1 × 4, 2 mm, vertical, straight, THT	Würth Elektronik, 62000411121
5	4	MP1 to MP4	Standoff, nylon, snap-on, 0.50"	Keystone, 8833
6	2	XJP1, XJP2	Connectors, shunt, female, 2 position, 2 mm	Würth Elektronik, 60800213421

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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