



ORSO/ORT82G5-B1

Evaluation Board

User Manual

JP4

Schematic page 3

A 7-pin serial connector used for configuration.

Serial Connector	
Pin 1	GND
Pin 2	NC
Pin 3	PROGRMN
Pin 4	DONE
Pin 5	D0
Pin 6	CCLK
Pin 7	VDD

JP6

Schematic page 3

JP6 is an 8-pin JTAG connector. It is physically similar to **JP4**; an arrow indicates pin 1.

JTAG Connector	
Pin 1	GND
Pin 2	INIT_N
Pin 3	RD_CFG_N
Pin 4	TDO
Pin 5	TCK
Pin 6	TMS
Pin 7	TDI
Pin 8	VDD

Header Connections

Standard 0.100 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords (such as Pomona Electronics #5948 www.pomonelectronics.com).

D17 & D18

Schematic page 3

These LEDs indicate the status of configuration to the FPGA. When D17 is illuminated this indicates the successful completion of configuration. When D18 illuminates this indicates that the programming was aborted or reinitialized.

JP1 & JP2

Schematic page 2

This is a *standard* header. Pin one is at the bottom left. Pin numbers increment from left to right. The even pins on this header correspond to general I/O pins. The odd pins are connected to ground .

JP3

Schematic page 2

This is a standard header (utilizing the even pins only) as described above. This header connects to 16-LEDs. When a jumper cable is used, output from the ORSO/ORT82G5 can drive these LEDs to display a pattern from JP1 and JP2.

JP35

Schematic pages 4

This is a 3 by 1 header that provides differential input/output from the ORSO/ORT82G5 primary clock spines. The first pin connects to the true side of the pair. Ground is connected to the middle column. The third pin is connected to the complement side of the pair.

J39, 40, 41

Schematic page 6

These 96-pin headers fit with the 860 bus to communicate to a Windriver (www.windriver.com) MPC860 development board.

JP32

Schematic page 5

This jumper selects the data 0 bit between the 860 bus communications and the 7-pin serial connector (**J1**). Jumping pins 2 and 3 selects the serial communication. Jumping pins 1 and 2 selects the 860 bus.

J52 and J53

Schematic page 4

These SMA connectors provide differential input to the PLL clocks.

PLL clocks	
J52	PLL_CLK0C
J53	PLL_CLK0T

JP36

Schematic page 4

This 2x2 header allows connection of ac coupling for J52 and J53. Adding a jumper between pins 1 and 2 or pins 3 and 4 removes the ac coupling capacitor.

PB1, PB2, PB3

Schematic page 3

These push button switches assert/de-assert the logic levels on the FPGA PRGMN, PRESET, and the SERDES reset. Depressing the button drives a logic level “0” to the device.

JP7

Schematic page 3

The 1x2 header enables the de-bounce IC for push-buttons PB1, 2, & 3. Connecting a jumper enables the circuitry.

JP9

Schematic page 3

This 1x3 header is connects PB3 to the SERDES reset or can connect the reset pin to GND.

JP12, JP13, JP14, JP15, JP16

Schematic page 5

These are 2X10 reference voltage headers are used to connect the specified voltage reference pins used by the FPGA IO pins.

JP19, 20, 21, 22,23

Schematic page 8

These jumpers select the input for the VddI/O voltage. Jumper connections are as follows.

1	2	1.5V
3	4	2.5V
5	6	3.3V

JP8

Schematic page 3

This 2x4 header is used to drive the correct levels to the device Mode pins. When left without jumpers to the even (2,4,6,8) pins the device is driven to “1”. No jumpers is “1111” for slave serial programming mode.

J51

Schematic page 9

This banana jack is connected to the ground plane of the board.

JP25, 30, 28, 26, 31

Schematic page 9

These 3-pin headers select the source of the SERDES power supplies. When a jumper is placed between Pin 1 and 2 the source of the supply comes from the on-board power supply. When the jumper is between P2 and 3 this selects the source from the adjacent banana jacks to be connected to an external supply.

JP24, 27, 29

Schematic page 9

These 3-pin headers select the source of the device (3.3V, 2.5V, and 1.5V) power supplies. When no jumpers are used the source of the supply comes from the on-board power supply. When the jumper is between P1 and 2 this selects the source from the adjacent banana jacks to be connected to an external supply.

J50

Schematic page 9

This banana jack connects to 5VDC supply.

JP5

Schematic page 3

JP5 is a ten-pin header for additional dedicated signals from the ORSO/ORT82G5. One column of the header (pins 2,4,6, etc) is connected to ground.

J82			
Pin 1	LVDS_R	Pin 2	GND
Pin 3	RCLK	Pin 4	GND
Pin 5	DOUT	Pin 6	GND
Pin 7	LDC	Pin 8	GND
Pin 9	HDC	Pin 10	GND

JP17, 18

Schematic page 5

These headers are the chip select controls. The default is selected when no jumpers are present.

JP10

Schematic page 4

This connector interconnects test points for the SERDES for characterization only. It is not populated for general use. This connector type is an Amp Z-Pack 2mm header. A cable similar to one from W. L. Gore (<http://www.wlgore.com/>) P/N 2MMA3193-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe signals or connect to other test devices.

JP10									
Pin A1	GND	Pin B1	RBC0	Pin C1	GND	Pin D1	RBC1	Pin E1	GND
Pin A2	WD_SYNC	Pin B2	GND	Pin C2	GND	Pin D2	GND	Pin E2	BYTE_SYNC
Pin A3	GND	Pin B3	GND	Pin C3	GND	Pin D3	GND	Pin E3	GND
Pin A4	GND	Pin B4	GND	Pin C4	GND	Pin D4	GND	Pin E4	XCK

JP11

Schematic page 4

This connector interconnects test points for the SERDES for characterization only. It is not populated for general use. This connector type is an Amp Z-Pack 2mm header. A cable similar to one from W. L. Gore (<http://www.wlgore.com/>) P/N 2MMA3192-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe signals or connect to other test devices.

JP11									
Pin A1	GND	Pin B1	LDIO0	Pin C1	GND	Pin D1	LDIO1	Pin E1	GND
Pin A2	LDIO2	Pin B2	GND	Pin C2	GND	Pin D2	GND	Pin E2	LDIO3
Pin A3	GND	Pin B3	LDIO4	Pin C3	GND	Pin D3	LDIO5	Pin E3	GND
Pin A4	LDIO6	Pin B4	GND	Pin C4	GND	Pin D4	GND	Pin E4	LDIO7
Pin A5	GND	Pin B5	LDIO8	Pin C5	GND	Pin D5	LDIO9	Pin E5	GND

J26

Schematic page 4

This test point is used to observe the CV (code violation) signal from the SERDES.

SERDES Reference Clocks

Schematic page 4

These SMA connectors connect to the reference clock pins of the SERDES. These pins receive a direct differential reference clock

J13	REFCLKA_N	J14	REFCLKA_P
J22	REFCLKB_N	J23	REFCLKB_P

SERDES Channels

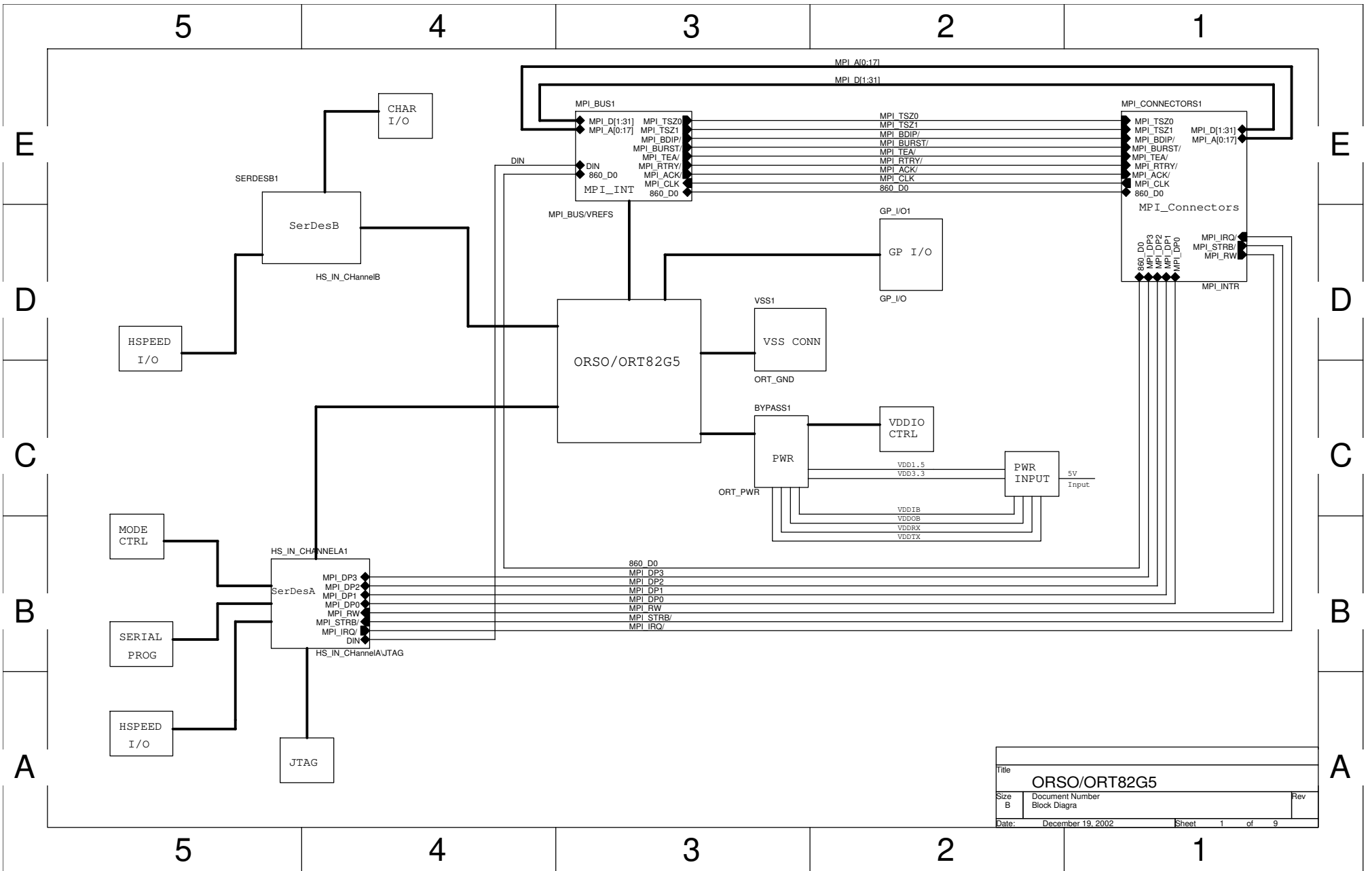
Schematic page 4

These SMA connectors connect to the SERDES Tx and Rx channels of Quad B of the SERDES. These pins receive a direct differential data.

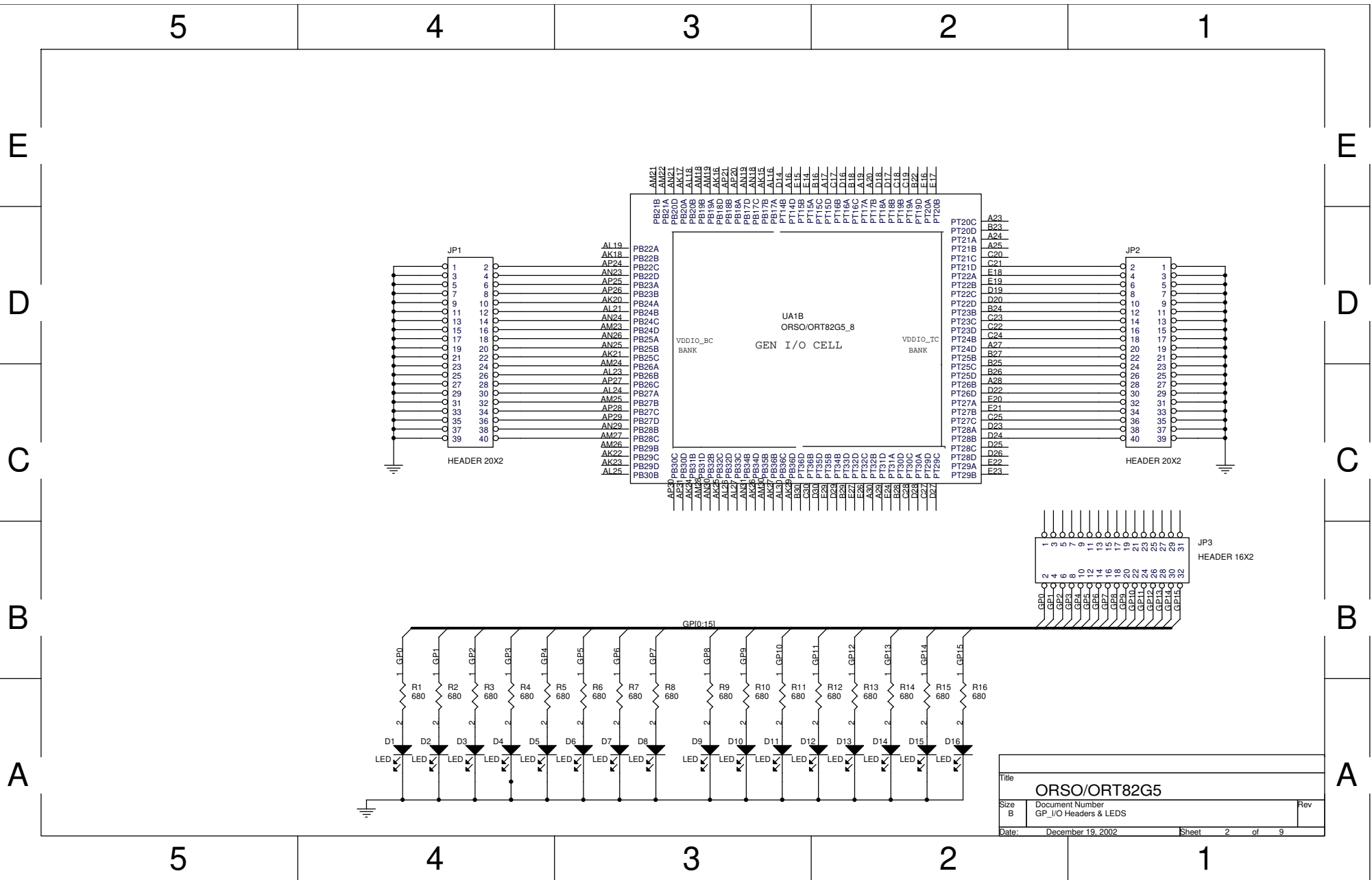
J19	INN_BA	J24	OUTN_BA
J20	INP_BA	J25	OUTP_BA
J27	INN_BB	J29	OUTN_BB
J28	INP_BB	J30	OUTP_BB
J31	INN_BC	J33	OUTN_BC
J32	INP_BC	J34	OUTP_BC
J35	INN_BD	J37	OUTN_BD
J36	INP_BD	J38	OUTP_BD

JP33 & JP34
Schematic page 3

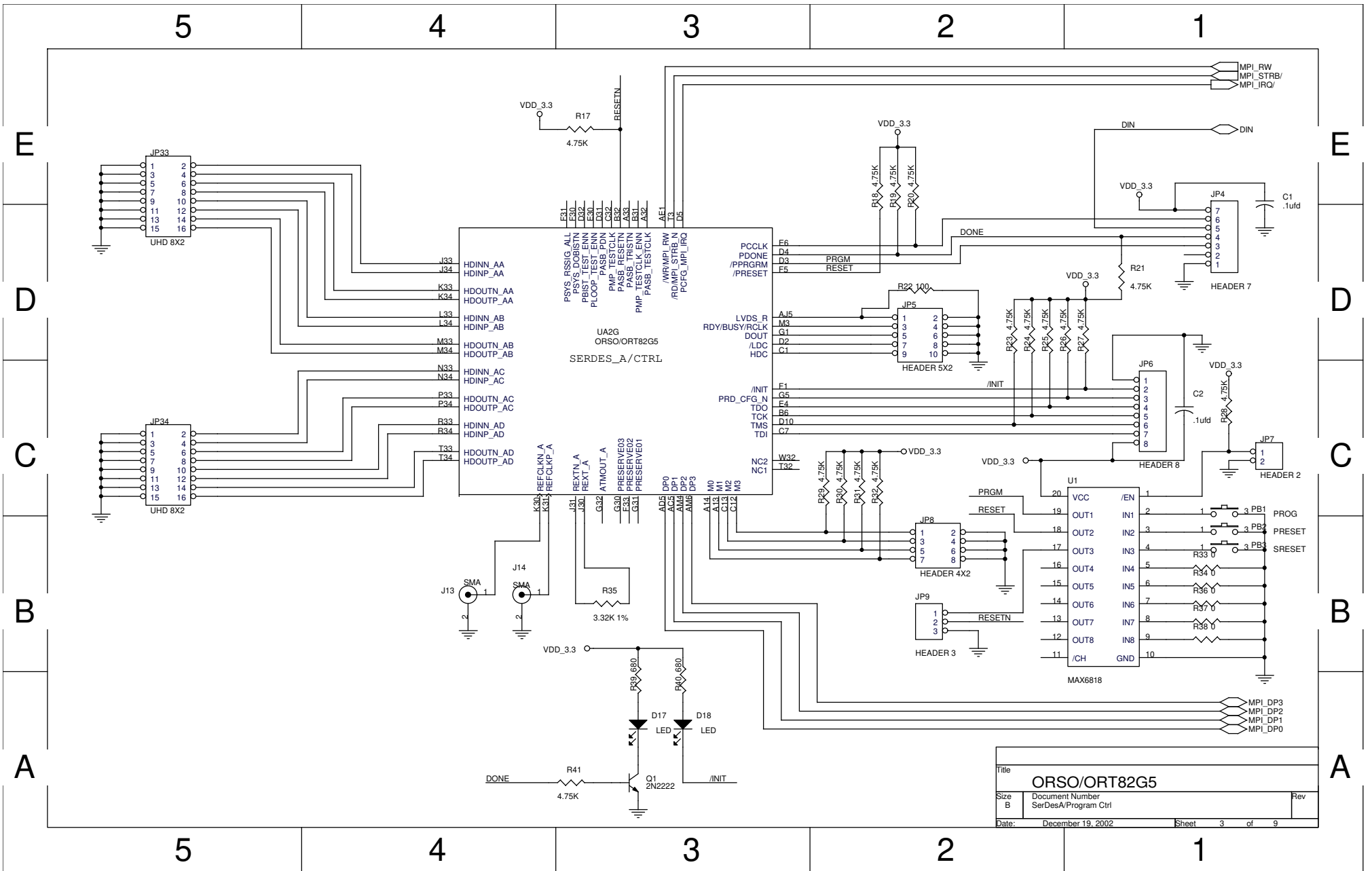
JP33 and JP34 are unpopulated connections for the SERDES channel A.



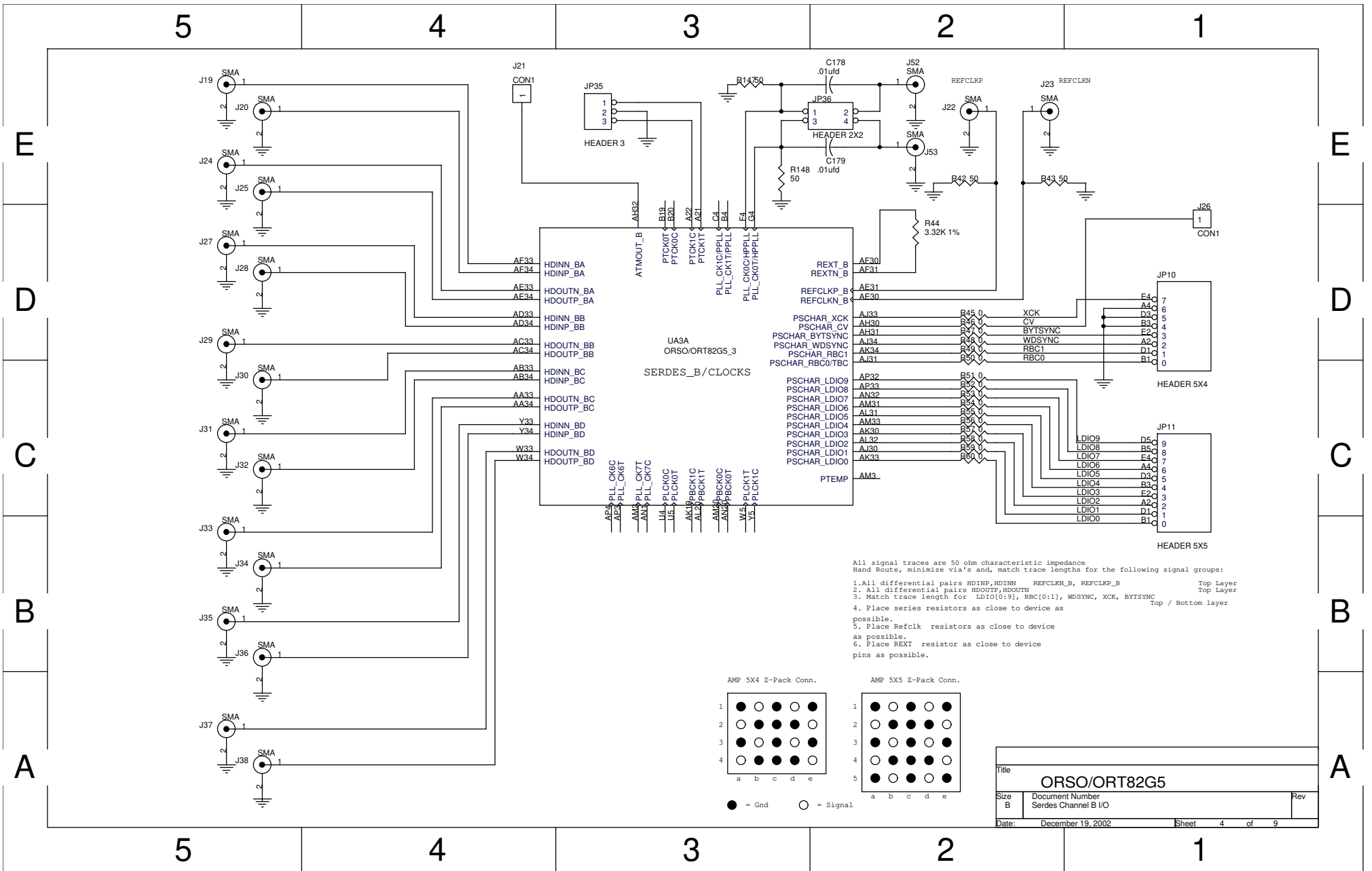
Title		
ORSO/ORT82G5		
Size	Document Number	Rev
B	Block Diagram	
Date:	December 19, 2002	Sheet 1 of 9



Title		ORSO/ORT82G5	
Size	Document Number	Rev	
B	GP_I/O Headers & LEDS		
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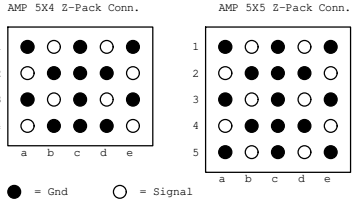


Title		ORSO/ORT82G5	
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B			
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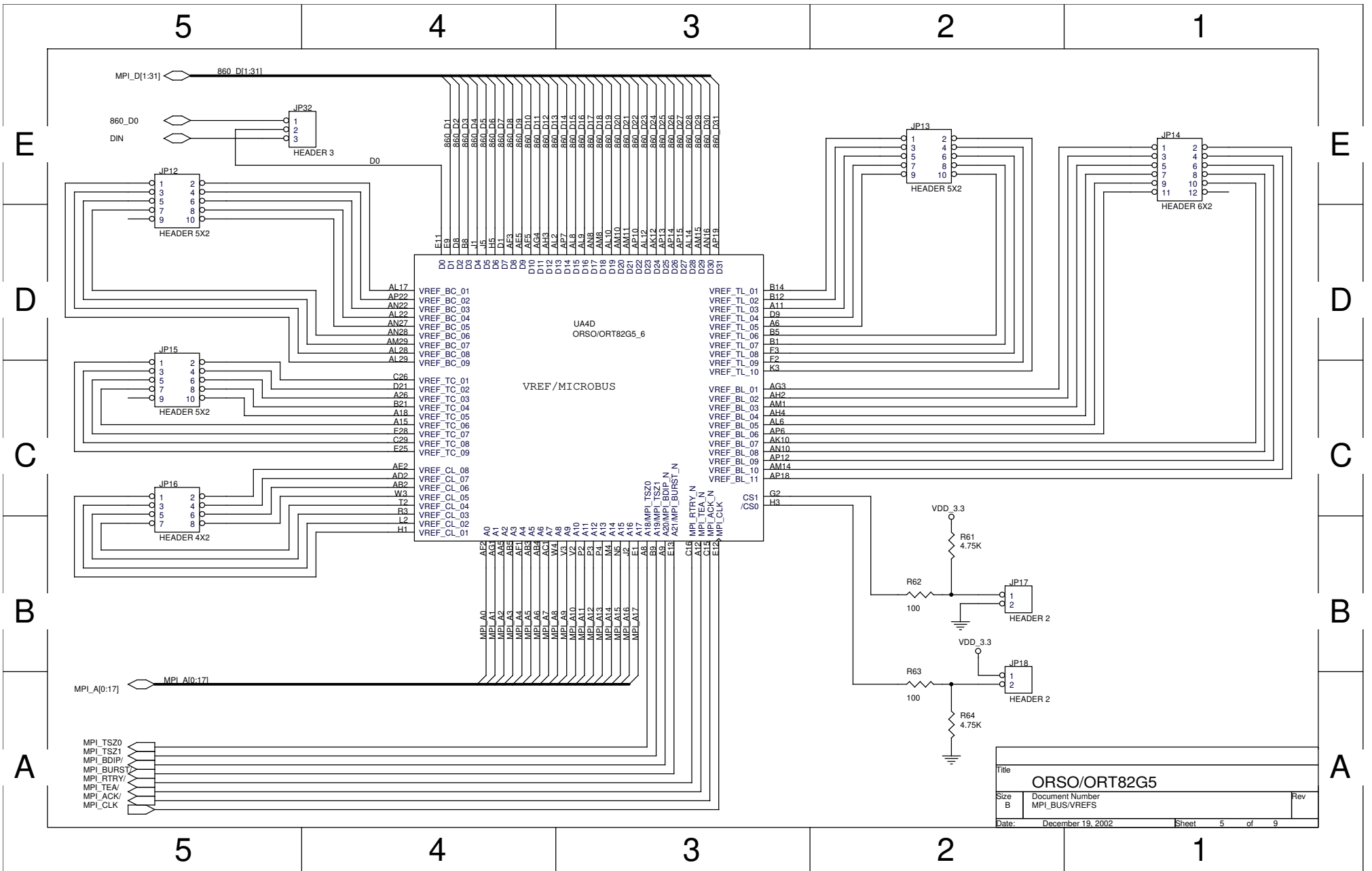


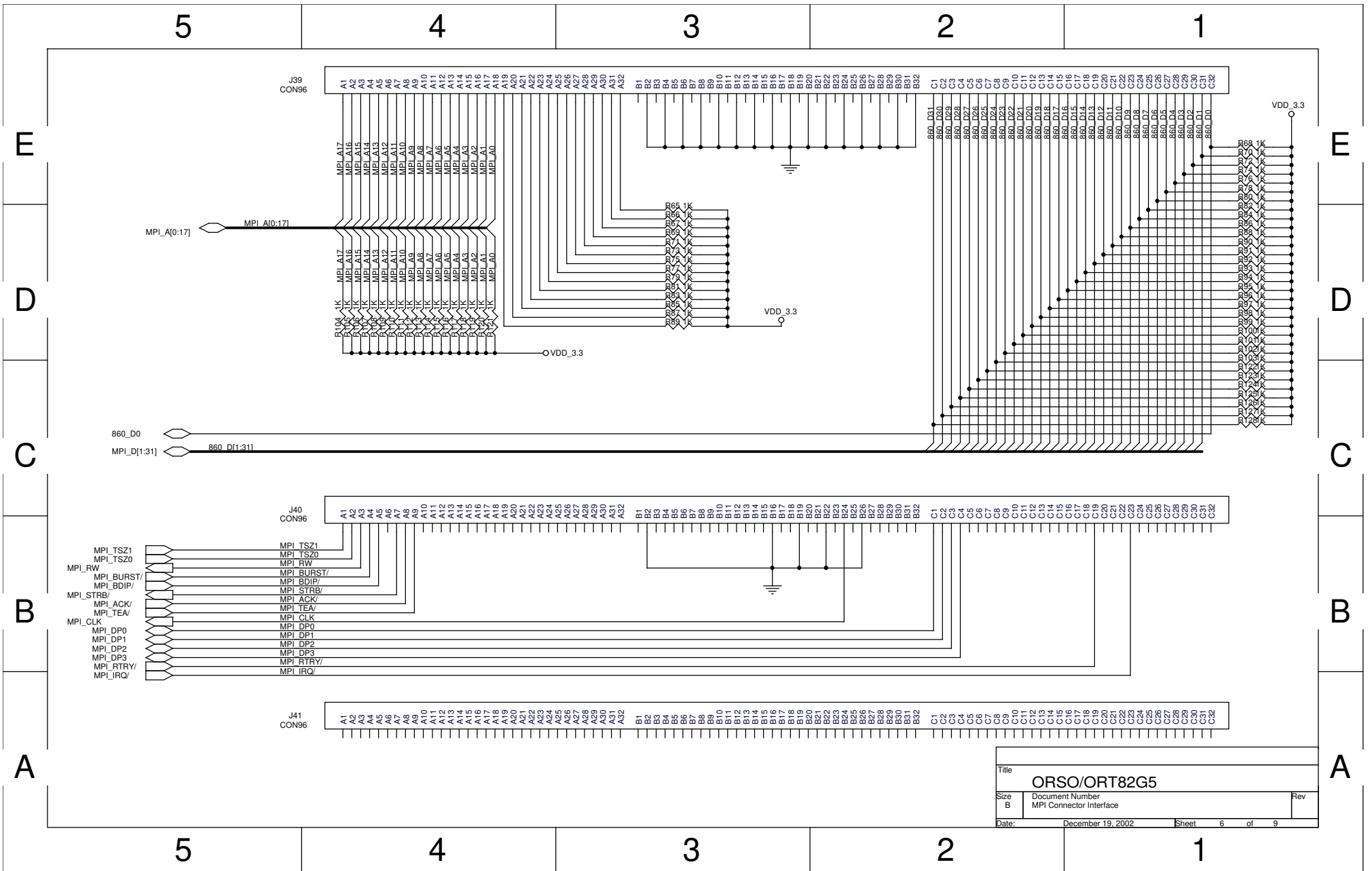
All signal traces are 50 ohm characteristic impedance
 Hand Route, minimize via's and, match trace lengths for the following signal groups:

1. All differential pairs HDINP, HDINN REFCLKN_B, REFCLKP_B Top Layer
2. All differential pairs HDOUTP, HDOUTN Top Layer
3. Match trace length for LDIO[0:9], RBC[0:1], WDSYNC, XCK, BYTSYNC Top / Bottom Layer
4. Place series resistors as close to device as possible.
5. Place Refclk resistors as close to device as possible.
6. Place REXT resistor as close to device pins as possible.

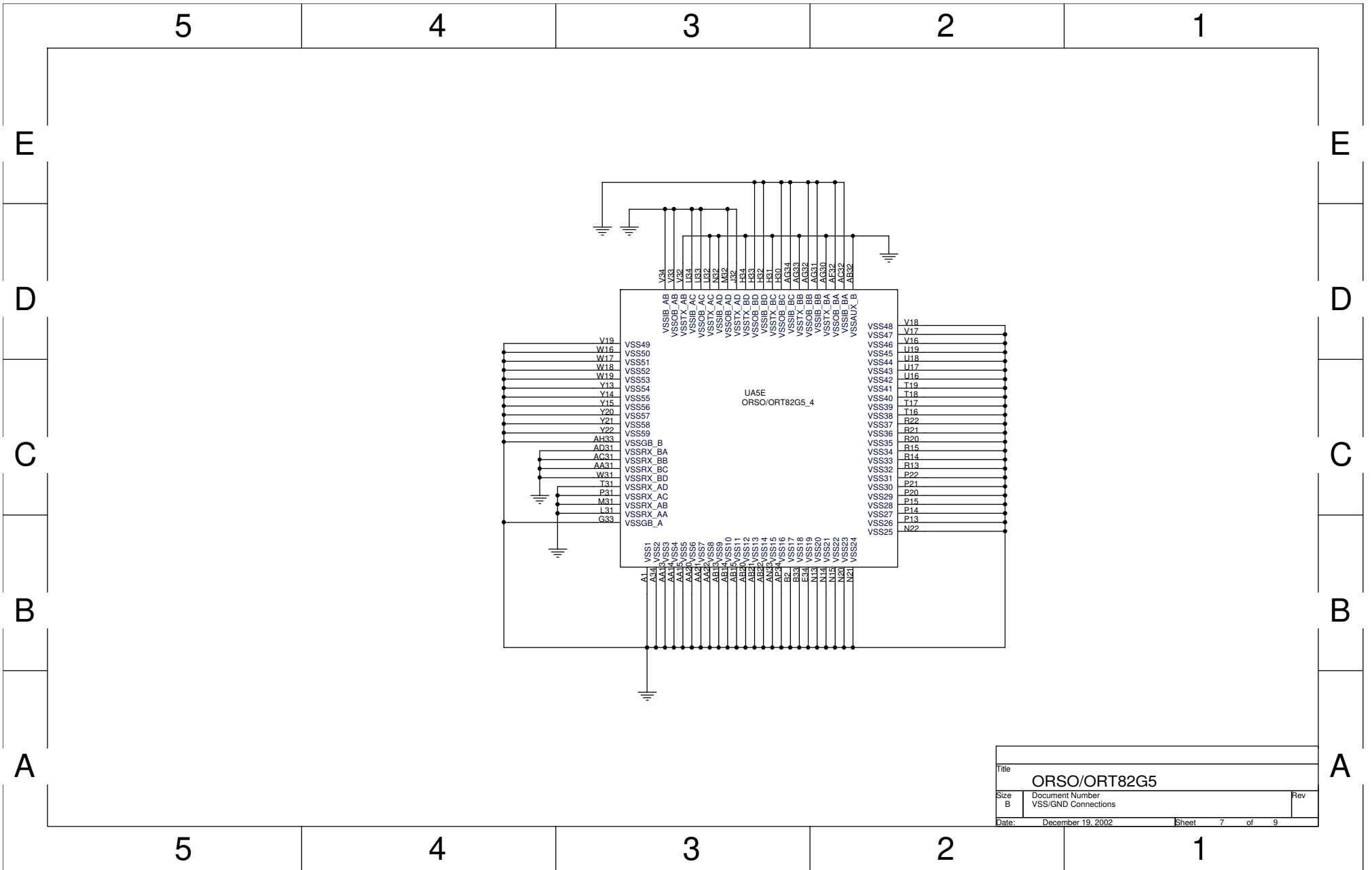


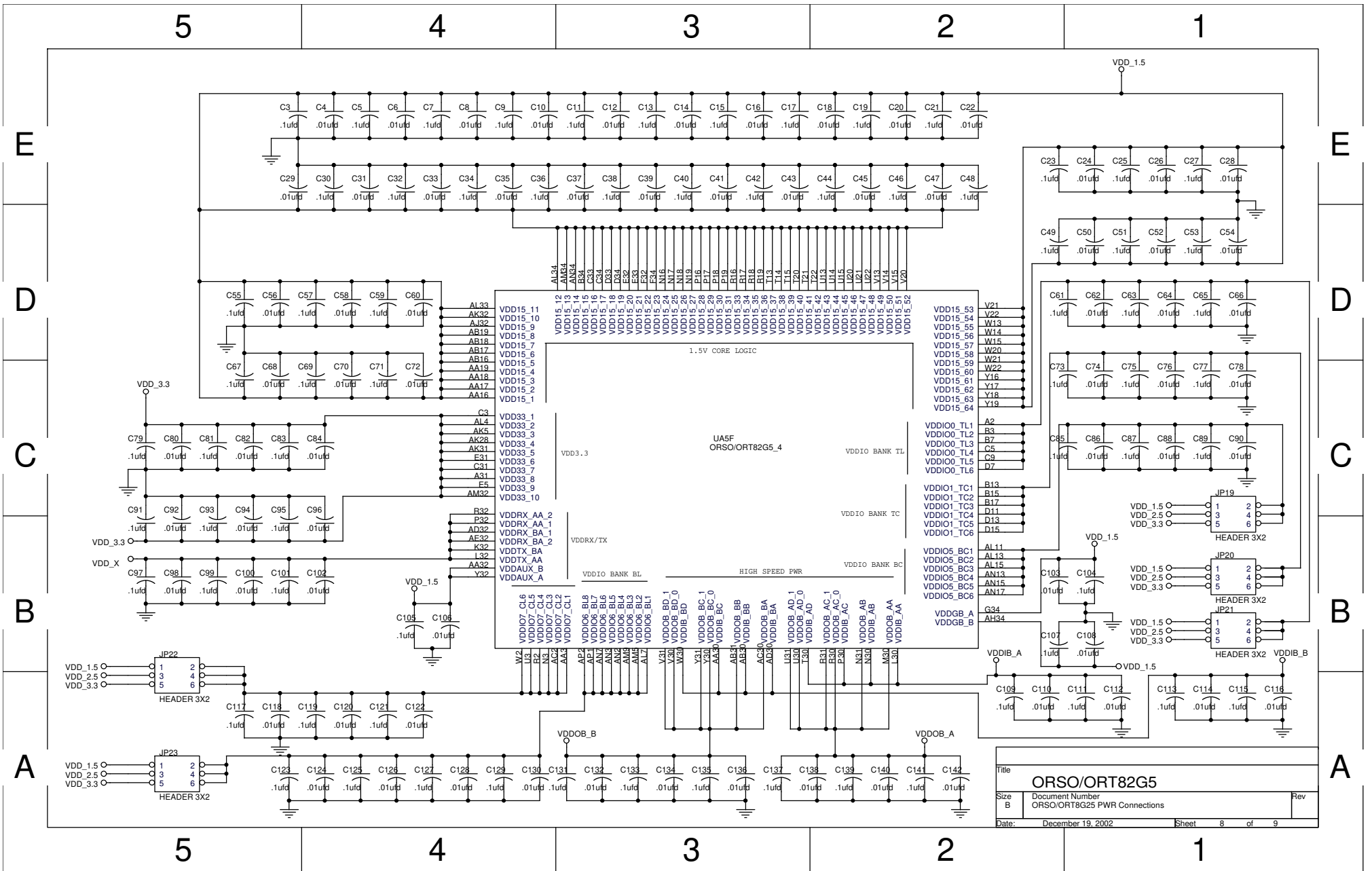
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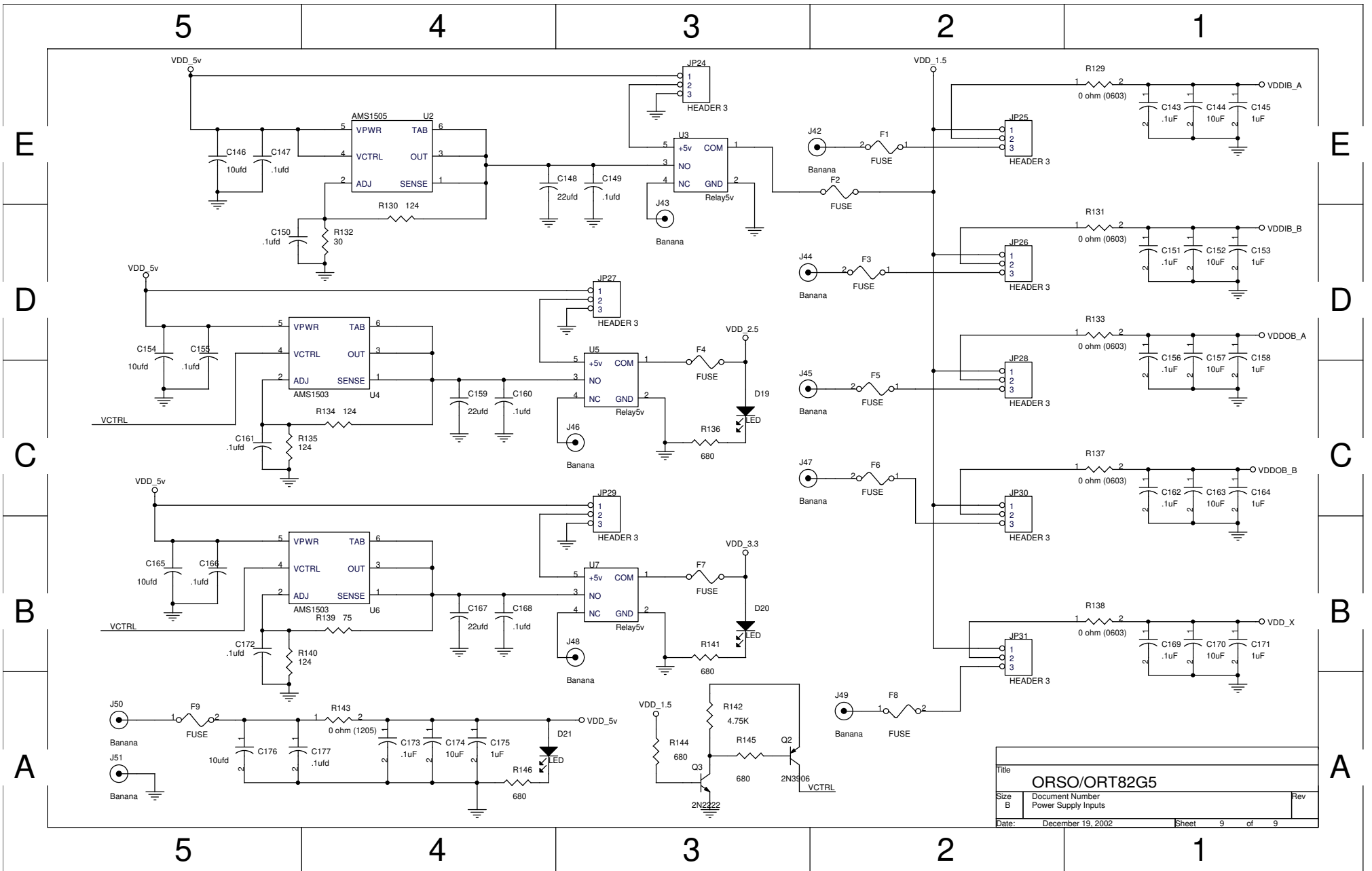


Title		ORSO/ORT82G5	
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B	MPI Connector Interface		
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B			
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B	Power Supply Inputs	
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