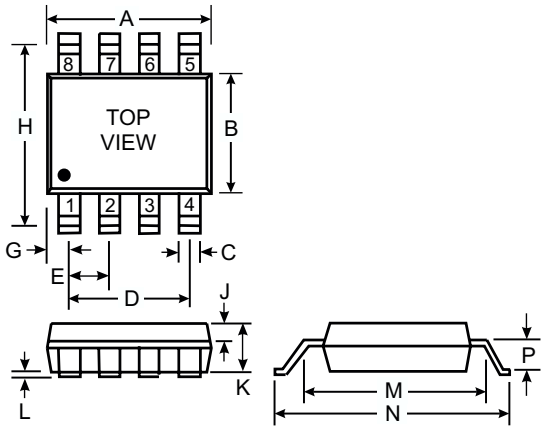
DI9435

SINGLE P-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

- High Cell Density DMOS Technology
- Low On-State Resistance
- High Power and Current Capability
- Fast Switching Speed
- High Transient Tolerance



SO-8		
Dim	**Min**	**Max**
A	3.94	4.19
B	3.20	3.40
C	0.381	0.495
D	2.67	3.05
E	0.89	1.02
G	0.527	0.679
J	0.41 Nominal	
K	0.94	1.09
L	0.025	0.152
M	4.37	4.62
N	4.39	4.70
P	0.939 Nominal	
All Dimensions in mm		

Mechanical Data

- SO-8 Plastic Case
- Terminal Connections: See Outline Drawing and Internal Circuit Diagram above

Maximum Ratings 25°C unless otherwise specified

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current	Continuous (Note 1a) Pulsed	I_D	±5.3 ±20	A
Maximum Power Dissipation	Note 1a Note 1b Note 1c	P_d	2.5 1.2 1.0	W
Operating and Storage Temperature Range		T_j, T_{STG}	-55 to +150	°C

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	Note 1a	$R_{\Theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case	Note 1	$R_{\Theta JC}$	25	°C/W

Notes: 1. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance ($R_{\Theta JC}$ + $R_{\Theta CA}$) where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\Theta JC}$ in this instance is 25°C/W but is dependent on the specific circuit board thermal design.

1a. With 1 in² of 2 oz. copper mounting pad $R_{\Theta JA}$ = 50°C\W.

1b. With 0.04 in² of 2 oz. copper mounting pad $R_{\Theta JA}$ = 105°C\W.

1c. With 0.006 in² of 2 oz. copper mounting pad $R_{\Theta JA}$ = 125°C\W.

Electrical Characteristics (continued) 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	V_{GS} = 0V, I_D = -25 µA
Zero Gate Voltage Drain Current T_j = 70°C	I_{DSS}	—	—	-1.0 -5.0	µA	VDS = -24V. V_{GS} = 0V V_{DS} = -15V. V_{GS} = 0V
Gate-Body Leakage, Forward	I_{GSSF}	—	—	100	nA	V_{GS} = 20V, V_{DS} = 0V
Gate-Body Leakage, Reverse	I_{GSSR}	—	—	-100	nA	V_{GS} = -20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage T_j = 125°C	$V_{GS(th)}$	-1.0 -0.7	-1.4 -1.0	—	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance T_j = 125°C	$R_{DS\ (ON)}$	—	0.038 0.054 0.046 0.064	0.05 0.10 0.07 0.09	Ω	V_{GS} = -10V, I_D = -5.3A V_{GS} = -10V, I_D = -5.3A V_{GS} = -6.0V, I_D = -4.7A V_{GS} = -4.5V, I_D = -4.2A
On-State Drain Current	$I_{D(ON)}$	-20 -5.0	—	—	A	V_{GS} = -10V, V_{DS} = -5.0V V_{GS} = -4.5V, V_{DS} = -5.0V
Forward Transconductance	g_{FS}	—	10	—	ṁ	V_{DS} = -15V, I_D = -5.3A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	—	950	—	pF	V_{DS} = -15V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{OSS}	—	610	—	pF	
Reverse Transfer Capacitance	C_{RSS}	—	220	—	pF	
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	$t_{D(ON)}$	—	10	30	ns	V_{DD} = -15V, I_D = -1.0A V_{GEN} = -10V, R_{GEN} = 6.0Ω
Turn-On Rise Time	t_r	—	18	60	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	80	120	ns	
Turn-Off Fall Time	t_f	—	45	100	ns	
Total Gate Charge	Q_g	—	29	40	nC	V_{DS} = -15V. I_D = -5.3A. V_{GS} = -10V
Gate-Source Charge	Q_{gs}	—	3.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	9.0	—	nC	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Max Continuous Drain-Source Diode Forward Current	I_S	—	—	-1.9	A	
Drain-Source Diode Forward Voltage	V_{SD}	—	-0.85	-1.3	V	V_{GS} = 0V, I_S = -5.3A (Note 2)
Reverse Recovery Time	t_{rr}	—	—	100	ns	V_{GS} = 0V, I_F = -5.3A, dI_F/dt = 100A/µs

Notes: 2. Pulse Test: Pulse width ≤ 300µs, duty cycle = ≤ 2.0%.

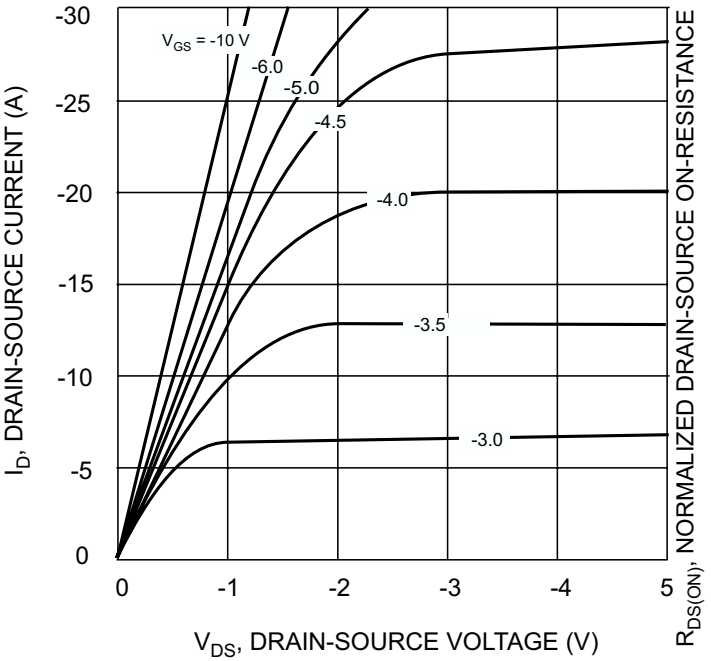


Fig. 1, On-Region Characteristics

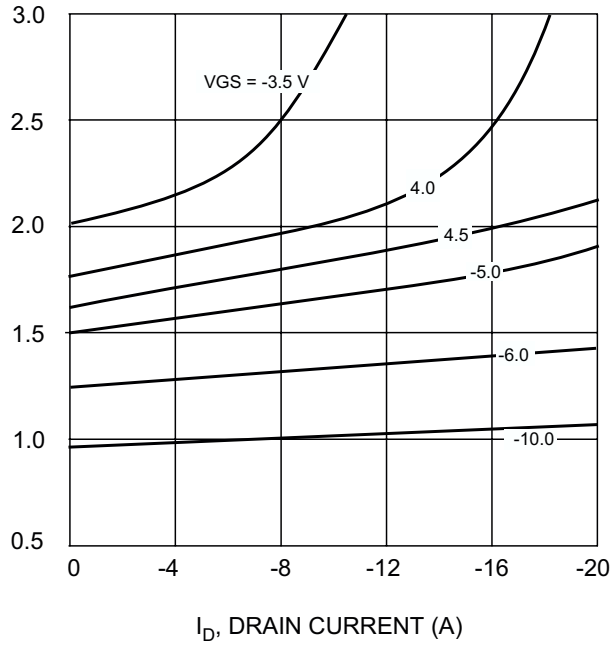


Fig. 2, On-Resistance vs Gate Voltage & Drain Current

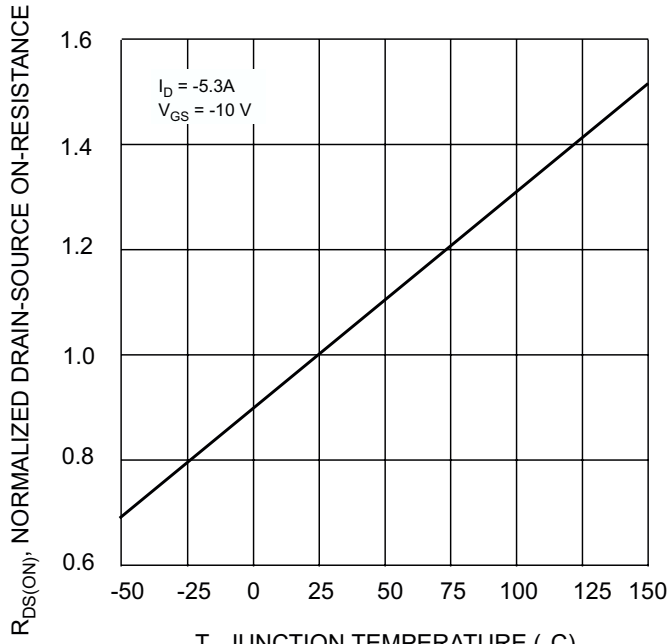


Fig. 3, On-Resistance vs Junction Temperature

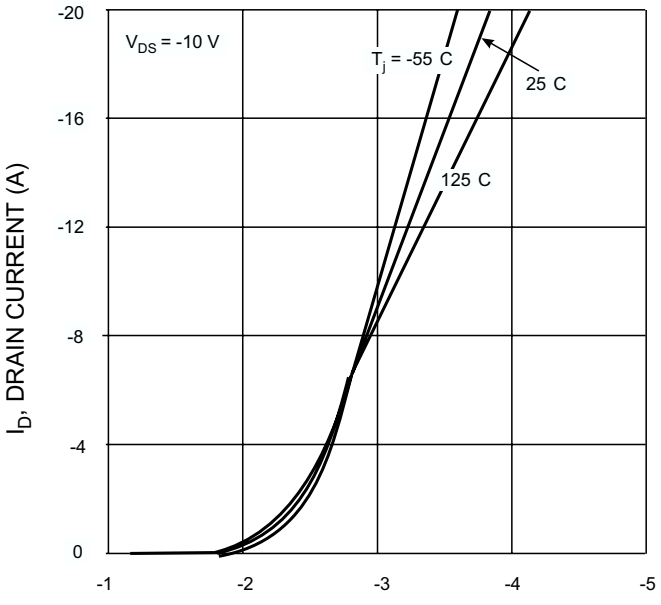


Fig. 4, Transfer Characteristics

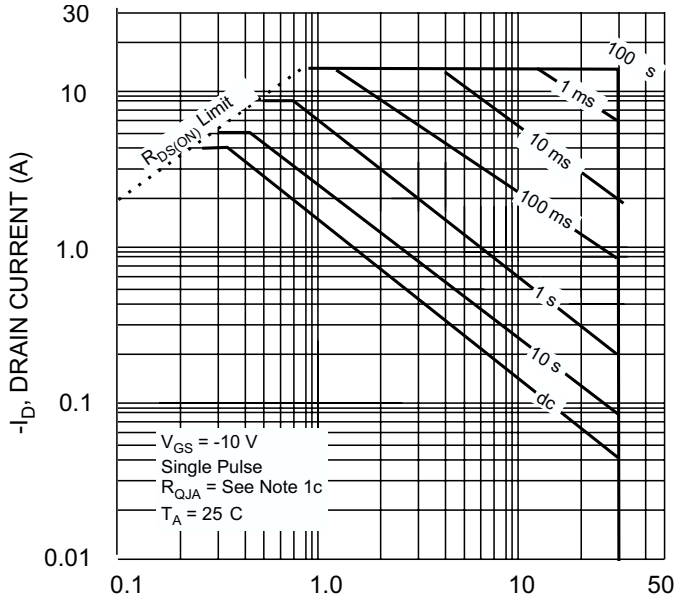


Fig. 5, Maximum Safe Operating Area

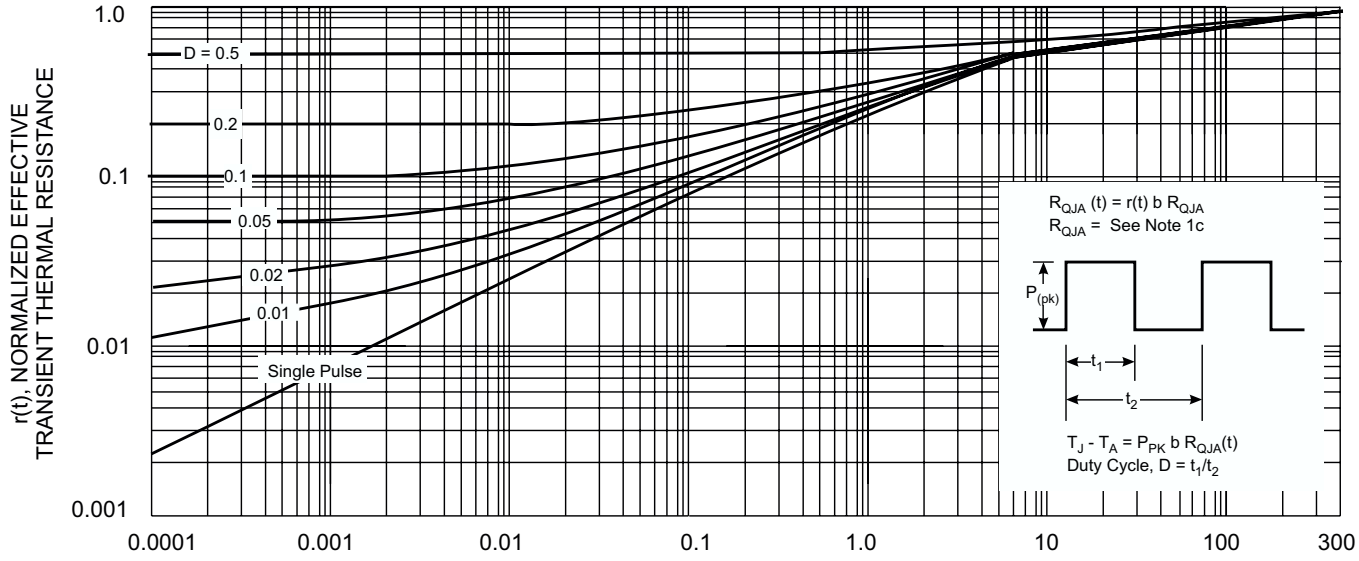


Fig. 6, Typical Normalized Transient Thermal Impedance Curves

Remark: Thermal characterization performed under conditions of Note 1c. Better thermal design such as shown in Notes 1a and 1b or 1d will offer lower $R_{\Theta JA}$ values and allow junction to reach thermal equilibrium sooner.