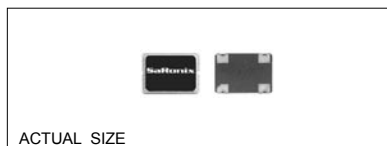


Technical Data

S1800 / S1803 / S1850 Series



Description

The 5V S1800, S1850 and 3.3V S1803 are crystal-controlled, low-current oscillators providing precise rise and fall times to drive high speed CMOS and TTL loads. The sub-miniature, very low profile leadless ceramic packages have gold-plated contact pads, ideal for today's pick-and-place SMT environments. The S1850 is a high output load version available to 80 MHz.

Applications & Features

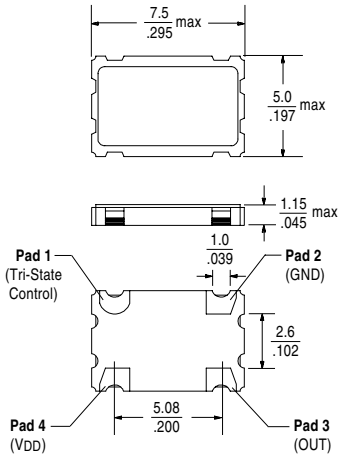
- Sub-miniature, 1.1 mm high ceramic package ideal for SMT applications
- 10µA max standby mode on S1800 and S1803
- Tight Stability, low power, and low profile ideal for 802.11 applications
- Available as 3.3V and 5V versions LVCMOS, HCMOS, TTL compatible
- Perfect for PC's; notebook, palmtop computers; portable applications; PCMCIA cards; disc drives. Anywhere small size, low power, surface mountability are a priority
- Available on tape & reel; 16mm tape, 1000pcs per reel

Frequency Range:	1.5440 MHz to 80 MHz		
Frequency Stability:	±20, ±25, ±50, ±100 ppm over all conditions; calibration, tolerance, operating temperature, input voltage change, load change, shock and vibration and aging*		
	*Aging (1 Year @ 25°C average ambient temperature)		
Temperature Range:	Operating: -10 to +70°C or -40 to +85°C Storage: -55 to +125°C		
Supply Voltage:	+5.0V ±10%, 3.3V ±10%		
Supply Current:	S1800	S1803	S1850
1.544 to 32 MHz:	25mA max	15mA max	27mA max
32+ to 50 MHz:	35mA max	25mA max	35mA max
50+ to 80 MHz:	n/a	40mA max	75mA max
Output disabled (Standby):	10µA max	10µA max	n/a
Output:	Symmetry: 45/55% max @ 50% V _{DD} , 40/60% max @ 1.5V on S1800 & 1850		
	Rise & Fall Times: S1800: 10ns max, 20% to 80% V _{DD} S1803: 7ns max, (to 50MHz), 5ns (>50 MHz), 20% to 80% V _{DD} S1850: 7ns max, 20% to 80% V _{DD}		
	Logic 0: 10% V _{DD} max		
	Logic 1: 90% V _{DD} min		
	Load: S1800/S1803: 15pF max, 10 LSTTL S1850: 50 pF max 1.544 to 50 MHz, 10 TTL 30 pF max 50+ to 70 MHz, 10 TTL 20 pF max 70+ to 80 MHz (HCMOS), 10 TTL		
	Accumulated Jitter: 5ps RMS (1-sigma) max in 20,000 adjacent periods		
	Phase Jitter: 1.5ps RMS (1-sigma) max in 10kHz ~ 20MHz freq. band		
	Total Jitter: 50ps max peak-to-peak in 100,000 random periods		
Mechanical:	Shock: MIL-STD-883, Method 2002, Condition B		
	Solderability: MIL-STD-883, Method 2003		
	Vibration: MIL-STD-883, Method 2007, Condition A		
	Solvent Resistance: MIL-STD-202, Method 215		
	Terminal Strength: MIL-STD-883, Method 2004, Condition D		
	Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition I or J		
Environmental:	Thermal Shock: MIL-STD-883, Method 1011, Condition A		
	Moisture Resistance: MIL-STD-883, Method 1004		

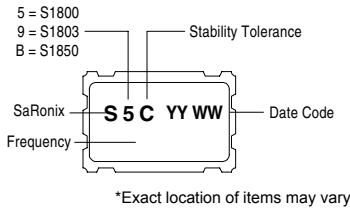
Technical Data

S1800 / S1803 / S1850 Series

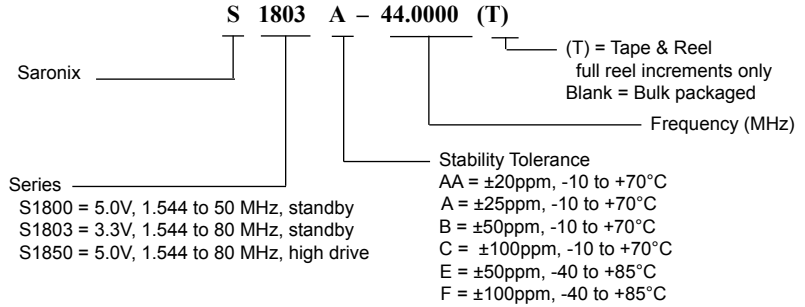
Package Details



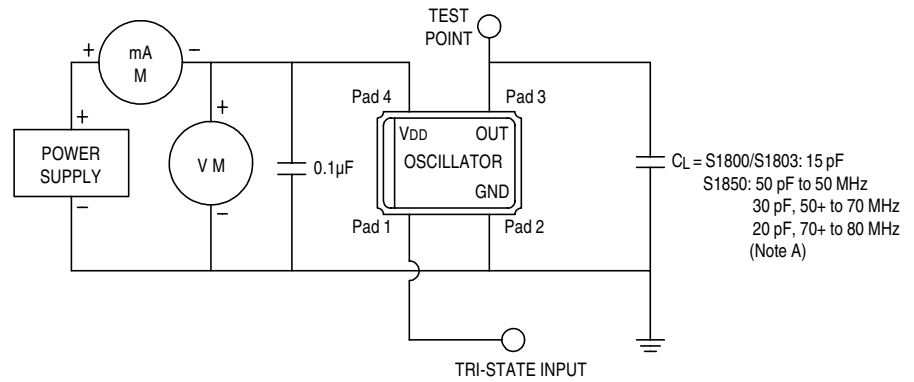
Marking Format*



Part Numbering Guide

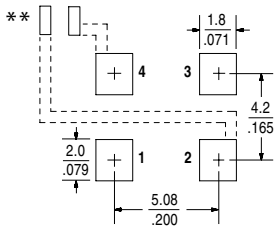


Test Circuit



Note A: CL includes probe and fixture capacitance

Recommended Land Pattern



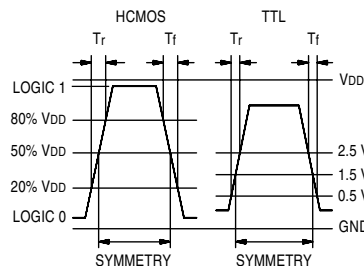
** External high frequency power supply decoupling required.

Scale: None (Dimensions in $\frac{\text{mm}}{\text{inches}}$)

Tri-State Control Characteristics (low power stand-by for S1800/S1803)

	S1850	S1800/S1803
Output Oscillation (V_{in}):	≥ 2.2V or N/C	≥ 2.2V or N/C
Output High Impedance (V_{IN}):	≤ 0.8V or GND	≤ 0.8V or GND
Disable Output Delay:	≤ 100ns	≤ 100ns (to Stand-by mode)
Enable Output Delay:	≤ 100ns	≤ 10ms (from Stand-by mode)
Internal Pullup Resistance:	≥ 50kΩ	≥ 50kΩ

Output Waveform



Solder Reflow Guide

