

MediaClock™ MPEG Clock Generator with VCXO

Features

- Integrated phase-locked loop (PLL)
- Low jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation

Benefits

- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Large ± 150 -ppm range, better linearity
- Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24212-1	1	13.5 MHz/27 MHz (selectable)	27 MHz
CY24212-2	2	13.5 MHz/27 MHz (selectable)	Two copies of 27 MHz
CY24212-3	2	27 MHz	27 MHz/27.027 MHz (-1 ppm)
CY24212-5	2	27 MHz	27 MHz/27.027 MHz (0 ppm)

Logic Block Diagram

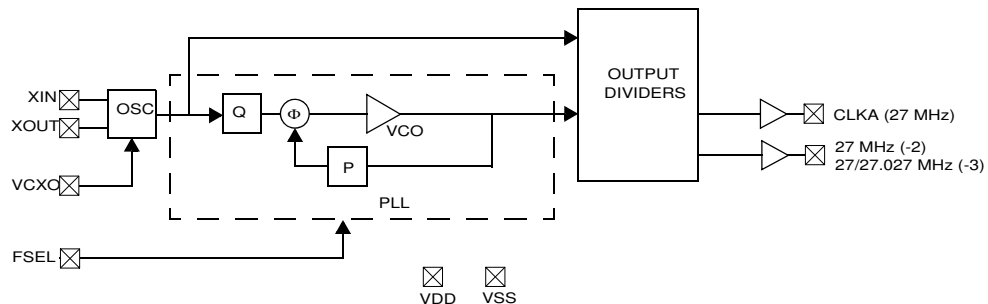


Table 1. CY24212 (-1, -2) Frequency Select Option

FSEL	Reference	CLKA/CLKB
0	13.5 MHz	27 MHz
1	27 MHz	27 MHz

Table 2. CY24212 (-3, -5) Frequency Select Option

FSEL	Reference	CLKA	CLKB
0	27 MHz	27 MHz	27 MHz
1	27 MHz	27 MHz	27.027 MHz

Pin Configurations

Figure 1. CY24212, 8-pin SOIC

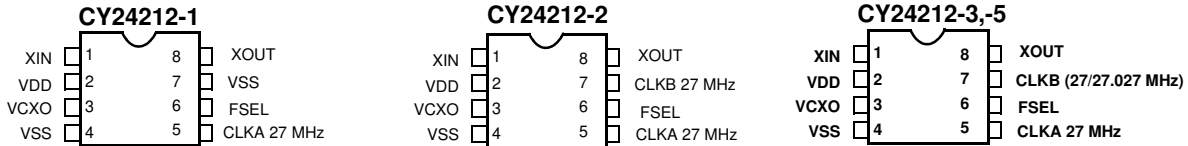


Table 3. Pin Definition

Name	Pin Number	Description
XIN	1	Reference Input.
VDD	2	Voltage Supply.
VCXO	3	Input Analog Control for VCXO.
VSS	4	Ground.
CLKA	5	27-MHz Clock Output.
FSEL (-1,-2)	6	Input Frequency Select, Weak Internal Pull up. FSEL = 0, XIN = 13.5 MHz FSEL = 1, XIN = 27 MHz
FSEL (-3,-5)	6	Output Frequency Select, Weak Internal Pull up. FSEL = 0, CLKA = 27 MHz, CLKB = 27 MHz FSEL = 1, CLKA = 27 MHz, CLKB = 27.027 MHz
VSS (-1)	7	Ground.
CLKB (-2)	7	27 MHz.
CLKB (-3,-5)	7	27 MHz/27.027 MHz.
XOUT ^[1]	8	Reference Output.

Pullable Crystal Specifications

Parameter	Name	Min	Typ.	Max	Unit
CR _{load}	Crystal Load Capacitance		14		pF
C0/C1				240	
ESR	Equivalent Series Resistance		35	50	Ω
T _o	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT _s	Stability over Temperature and Aging			± 50	ppm

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V _{DD}	Supply Voltage	-0.5	7.0	V
T _S	Storage Temperature ^[2]	-65	125	°C
T _J	Junction Temperature		125	°C
	Digital Inputs	V _{SS} - 0.3	V _{DD} + 0.3	V
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V _{DD}	Operating Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	0		70	°C
C _{LOAD}	Max. Load Capacitance			15	pF
f _{REF}	Reference Frequency	13.5		27	MHz

Notes

1. Float XOUT if XIN is externally driven.
2. Rated for ten years.

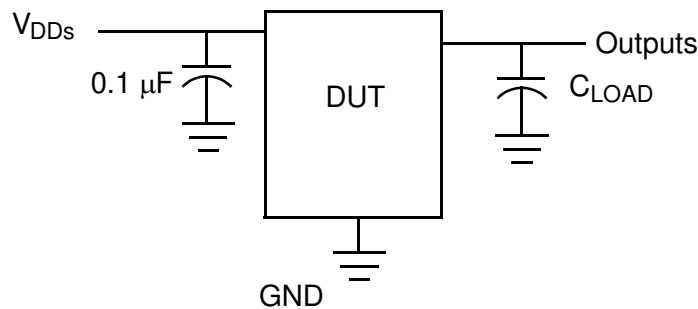
DC Electrical Specifications

Parameter	Name	Description	Min	Typ	Max	Unit
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5, V _{DD} = 3.3V (source)	12	24		mA
I _{OL}	Output Low Current	V _{OL} = 0.5, V _{DD} = 3.3V (sink)	12	24		mA
C _{IN}	Input Capacitance				7	pF
I _{IH}	Input High Current	V _{IH} = V _{DD}	-	5	10	μA
I _{IL}	Input Low Current	V _{IL} = 0V	-	-	50	μA
f _{ΔXO}	VCXO Pullability Range		±150			ppm
V _{VCXO}	VCXO Input Range		0		V _{DD}	V
I _{DD}	Supply Current	Sum of Core and Output Current			35	mA
V _{IH}	Input High Voltage	CMOS levels, 70% of V _{DD}	0.7			V _{DD}
V _{IL}	Input Low Voltage	CMOS levels, 30% of V _{DD}			0.3	V _{DD}
R _{UP}	Pull up resistor on inputs	V _{DD} = 3.14 to 3.47V, measured V _{IN} = 0V		100	150	kΩ

AC Electrical Specifications (V_{DD} = 3.3V)

Parameter ^[3]	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in <i>Figure 2</i> , 50% of V _{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V _{DD} , C _{LOAD} = 15 pF. See <i>Figure 3</i> .	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V _{DD} , C _{LOAD} = 15 pF. See <i>Figure 3</i> .	0.8	1.4		V/ns
t ₉	Clock Jitter	Peak-to-peak period jitter		300		ps
t ₁₀	PLL Lock Time				3	ms

Test and Measurement Setup



Note
3. Not 100% tested.

Voltage and Timing Definitions

Figure 2. Duty Cycle Definition

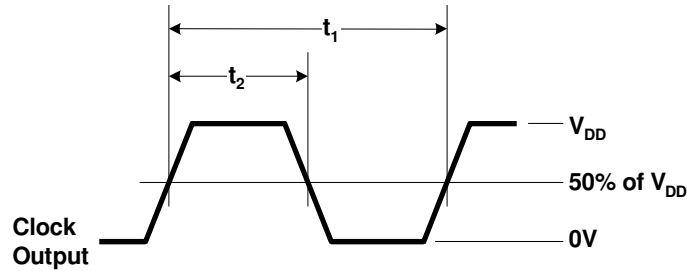
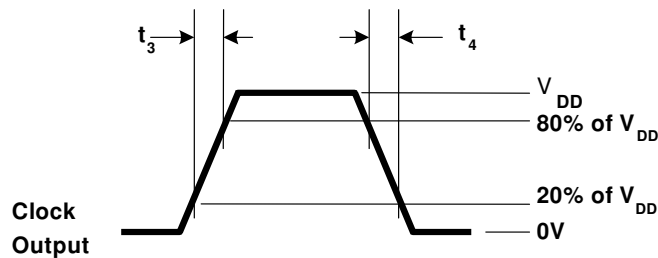


Figure 3. $ER = (0.6 \times V_{DD}) / t_3$, $EF = (0.6 \times V_{DD}) / t_4$



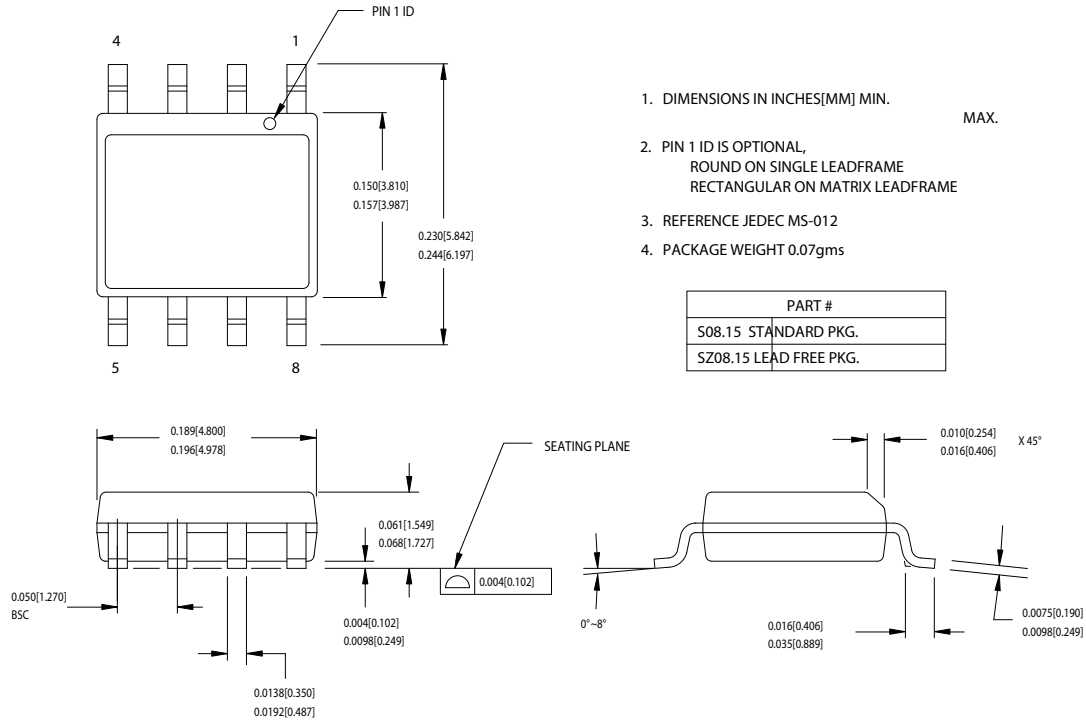
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY24212SC-1 ^[4]	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-1T ^[4]	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-2 ^[4]	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-2T ^[4]	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-3 ^[4]	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-3T ^[4]	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212SC-5 ^[4]	S8	8-Pin SOIC	Commercial	3.3V
CY24212SC-5T ^[4]	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
Pb-free				
CY24212SXC-5 ^[4]	S8	8-Pin SOIC	Commercial	3.3V
CY24212SXC-5T ^[4]	S8	8-Pin SOIC -Tape and Reel	Commercial	3.3V
CY24212KSXC-5	S8	8-Pin SOIC	Commercial	3.3V

Note
4. Not recommended for new designs.

Package Drawing and Dimensions

Figure 4. 8-lead (150-Mil) SOIC S8



1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

51-85066-°C

Document History Page

Document Title: CY24212 MediaClock™ MPEG Clock Generator with VCXO Document Number: 38-07402				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	117089	09/09/02	CKN	New Data Sheet
*A	120888	12/06/02	CKN	Added -3
*B	123064	02/19/03	CKN	Added -5
*C	345540	See ECN	RGL	Added Pb-free for -5 part
*D	2447126	See ECN	AESA	Updated template. Added Note "Not recommended for new designs." Added part number CY24212KSXC-5 in ordering information table.

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