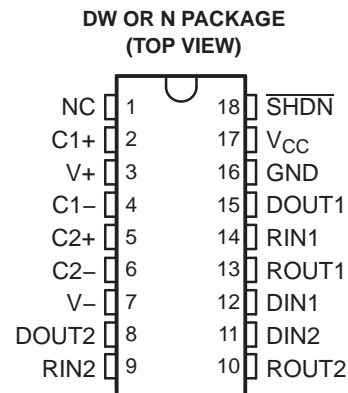


## FEATURES

- ESD Protection for RS-232 Bus Pins
  - $\pm 15$ -kV Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates at 5-V  $V_{CC}$  Supply
- Operates up to 200 kbit/s
- Low Supply Current in Shutdown Mode . . . 2  $\mu$ A Typical
- External Capacitors . . .  $4 \times 0.1 \mu$ F
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II



## APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

## DESCRIPTION/ORDERING INFORMATION

The TRS222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. This device operates at data signaling rates up to 200 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate. By using shutdown ( $\overline{\text{SHDN}}$ ), all receivers can be disabled.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	TRS222CN	TRS222CN
	SOIC – DW	Tube of 20	TRS222CDW	TRS222C
		Reel of 1000	TRS222CDWR	
–40°C to 85°C	PDIP – N	Tube of 20	TRS222IN	TRS222IN
	SOIC – DW	Tube of 20	TRS222IDW	TRS222I
		Reel of 1000	TRS222IDWR	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**FUNCTION TABLES**

**Each Driver<sup>(1)</sup>**

INPUT DIN	OUTPUT DOUT
L	H
H	L

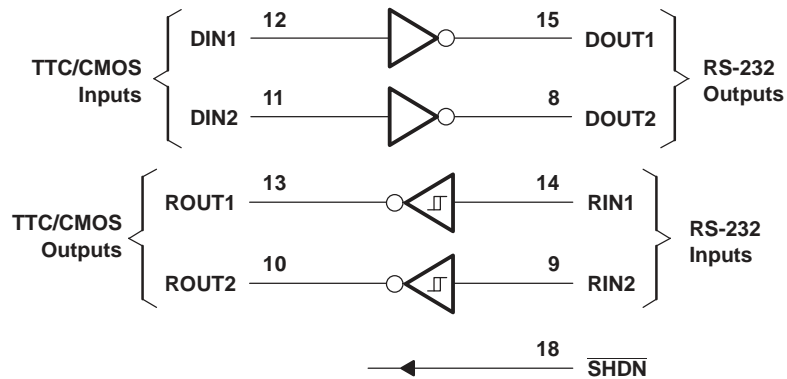
(1) H = high level, L = low level

**Each Receiver<sup>(1)</sup>**

INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

(1) H = high level, L = low level,  
Open = input disconnected or  
connected driver off

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	−0.3	6	V
V <sub>I</sub>	Input voltage range	Drivers	V <sub>CC</sub> − 0.3	V
		Receivers	±30	
V <sub>O</sub>	Output voltage range	Drivers	±15	V
		Receivers	−0.3 V <sub>CC</sub> + 0.3	
D <sub>OUT</sub>	Short-circuit duration	Continuous		
$\theta_{JA}$	Package thermal impedance <sup>(3)(4)</sup>	DW package	58	°C/W
		N package	TBD	
T <sub>J</sub>	Operating virtual junction temperature	150		°C
T <sub>stg</sub>	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network GND.

(3) Maximum power dissipation is a function of T<sub>J(max)</sub>,  $\theta_{JA}$ , and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> − T<sub>A</sub>)/ $\theta_{JA}$ . Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

See [Figure 4](#)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	Driver high-level input voltage	DIN			V
	Shutdown high-level input voltage	SHDN			
V <sub>IL</sub>	Driver and control low-level input voltage	DIN			V
	Shutdown low-level input voltage	SHDN			
V <sub>I</sub>	Driver input voltage	0	5.5		V
	Receiver input voltage	−30	30		
T <sub>A</sub>	Operating free-air temperature	TRS222C			°C
		TRS222I			

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

## Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = 5 V,	SHDN = V <sub>CC</sub>	No load	4	10	mA
				3 k $\Omega$ on both inputs	15		
	Shutdown supply current				2	50	$\mu$ A
SHDN	Shutdown input leakage current				±1		$\mu$ A

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

## DRIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	DOUT at R <sub>L</sub> = 3 k $\Omega$ to GND, DIN = GND	5	8		V
V <sub>OL</sub>	Low-level output voltage	DOUT at R <sub>L</sub> = 3 k $\Omega$ to GND, DIN = V <sub>CC</sub>	–5	–8		V
I <sub>IH</sub>	Driver high-level input current	DIN = V <sub>CC</sub>		5	40	$\mu$ A
	Control high-level input current	$\overline{\text{SHDN}}$ = V <sub>CC</sub>		0.01	1	
I <sub>IL</sub>	Driver low-level input current	DIN = 0 V		–5	–40	$\mu$ A
	Control low-level input current	$\overline{\text{SHDN}}$ = 0 V		–0.01	–1	
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V	$\pm 7$	$\pm 22$		mA
I <sub>off</sub>	Output leakage current	V <sub>CC</sub> = 5.5 V, $\overline{\text{SHDN}}$ = GND, V <sub>O</sub> = $\pm 10$ V		$\pm 0.01$	$\pm 10$	$\mu$ A
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = $\pm 2$ V	300	10 M		$\Omega$

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

(2) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
	Data rate	C <sub>L</sub> = 1000 pF, R <sub>L</sub> = 3 k $\Omega$ , One DO <sub>UT</sub> switching, See <a href="#">Figure 1</a>	200			kbit/s
t <sub>PLH(D)</sub>	Propagation delay time, low- to high-level output	See <a href="#">Figure 1</a>		1.5	3.5	$\mu$ s
t <sub>PHL(D)</sub>	Propagation delay time, high- to low-level output	See <a href="#">Figure 1</a>		1.3	3.5	$\mu$ s
t <sub>PHL(D)</sub> – t <sub>PLH(D)</sub>	Driver (+ to –) propagation delay difference			300		ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 k $\Omega$ to 7 k $\Omega$ , See <a href="#">Figure 2</a>		300		ns
SR(tr)	Slew rate, transition region (see <a href="#">Figure 1</a> )	C <sub>L</sub> = 50 pF to 2500 pF, V <sub>CC</sub> = 5 V, R <sub>L</sub> = 3 k $\Omega$ to 7 k $\Omega$	6	12	30	V/ $\mu$ s
t <sub>ET</sub>	Driver output enable time (after $\overline{\text{SHDN}}$ goes high)			250		$\mu$ s
t <sub>DT</sub>	Driver output disable time (after $\overline{\text{SHDN}}$ goes low)			300		ns

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

(2) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## RECEIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 4](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –1 mA	3.5	V <sub>CC</sub> – 0.2		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OH</sub> = 3.2 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 5 V		1.7	2.4	V
V <sub>IT–</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 5 V	0.8	1.3		V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )		0.2	0.5	1	V
r <sub>i</sub>	Input resistance	V <sub>i</sub> = $\pm 3$ V to $\pm 25$ V	3	5	7	k $\Omega$

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

(2) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 3](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
t <sub>PLH(R)</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF		0.6	1	$\mu$ s
t <sub>PHL(R)</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF		0.5	1	$\mu$ s
t <sub>PHL(R)</sub> – t <sub>PLH(R)</sub>	Receiver (+ to –) propagation delay difference			100		ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>			100		ns

(1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

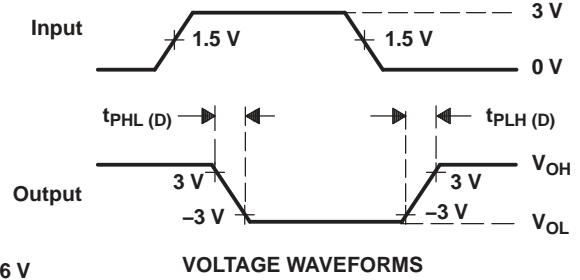
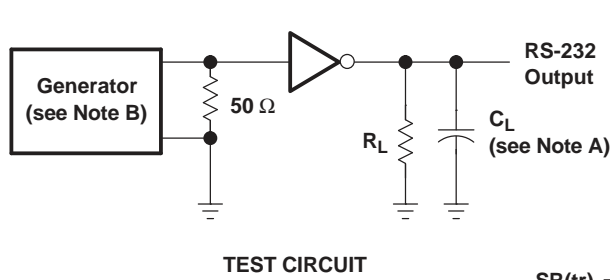
(2) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## ESD Protection

PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	Human-Body Model	$\pm 15$	kV

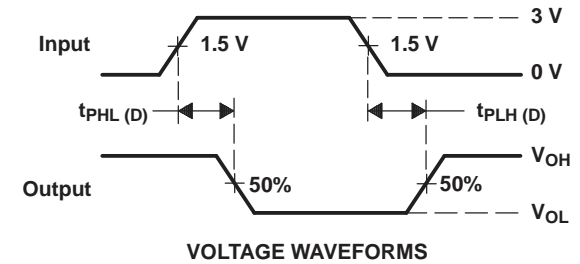
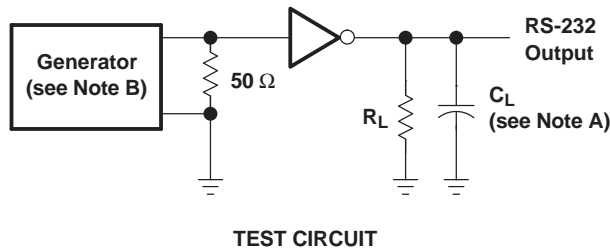
PARAMETER MEASUREMENT INFORMATION



$$SR(tr) = \frac{6\text{ V}}{t_{PHL(D)} \text{ or } t_{PLH(D)}}$$

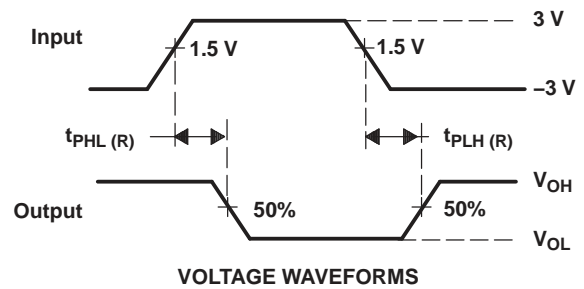
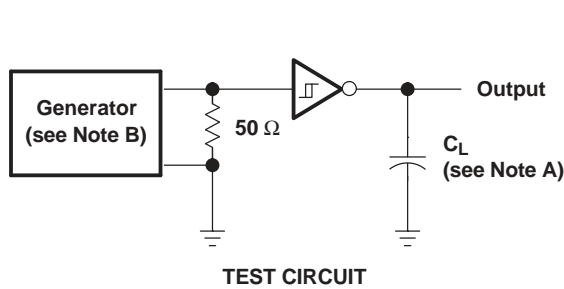
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 1. Driver Slew Rate



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

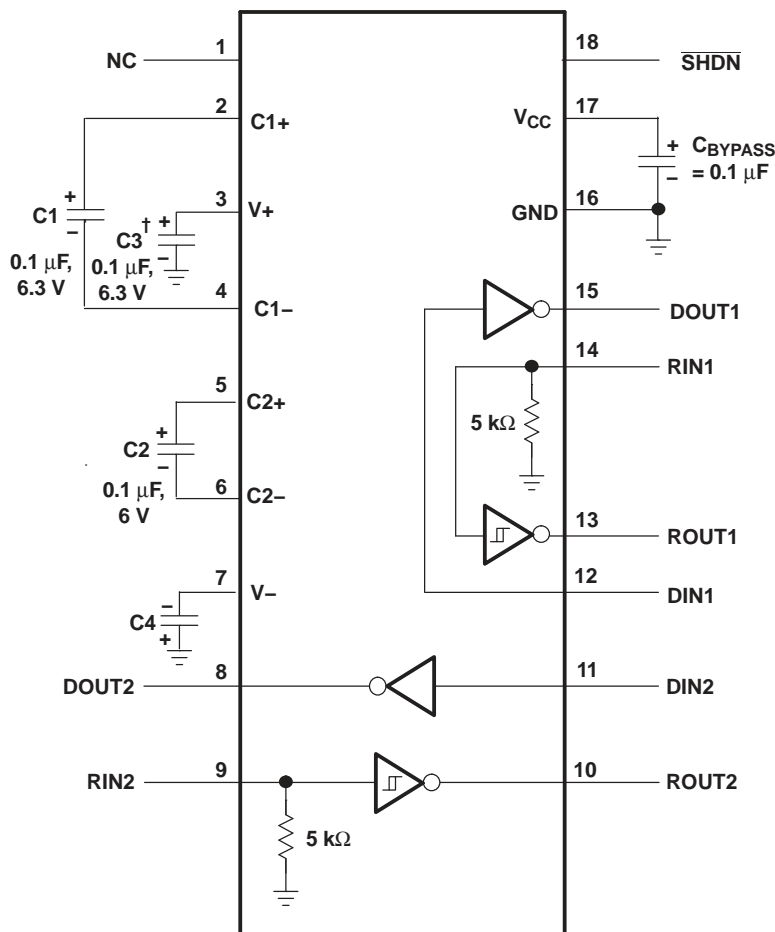
Figure 2. Driver Pulse Skew



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 3. Receiver Propagation Delay Times

**APPLICATION INFORMATION**



† C3 can be connected to V<sub>CC</sub> or GND.

- A. Resistor values shown are nominal
- B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**Figure 4. Typical Operating Circuit and Capacitor Values**

## APPLICATION INFORMATION (continued)

### Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The TRS222 requires 0.1- $\mu\text{F}$  capacitors, although capacitors up to 10  $\mu\text{F}$  can be used without harm. Ceramic dielectrics are suggested for the 0.1- $\mu\text{F}$  capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2 $\times$ ) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V–.

Use larger capacitors (up to 10  $\mu\text{F}$ ) to reduce the output impedance at V+ and V–.

Bypass  $V_{CC}$  to ground with at least 0.1  $\mu\text{F}$ . In applications sensitive to power-supply noise generated by the charge pumps, decouple  $V_{CC}$  to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

### Electrostatic Discharge (ESD) Protection

TI TRS222 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of  $\pm 15$  kV when powered down.

### ESD Test Conditions

ESD testing stringently is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

### Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k $\Omega$  resistor.

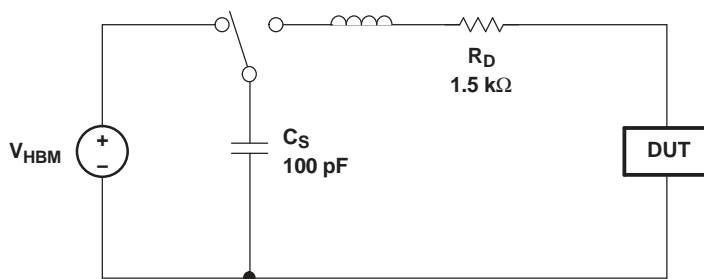
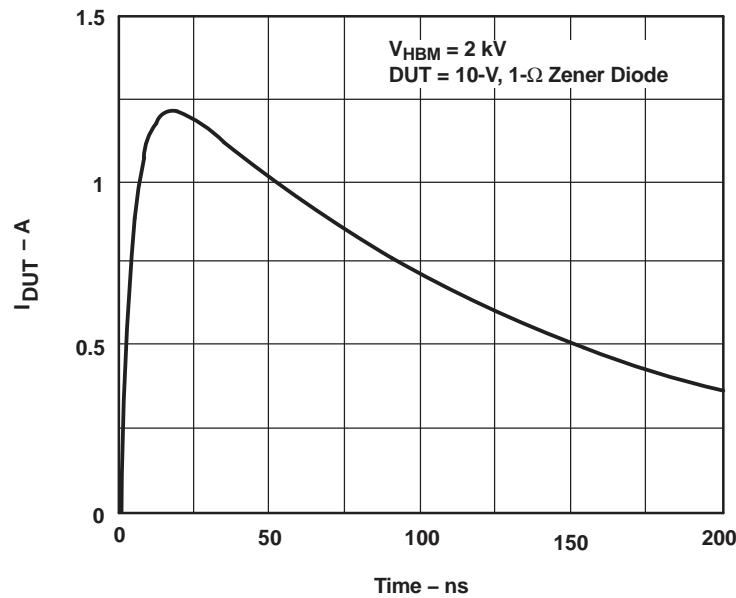


Figure 5. HBM ESD Test Circuit



**APPLICATION INFORMATION (continued)**



**Figure 6. Typical HBM Current Waveform**

**Machine Model (MM)**

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TRS222CDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222CN	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS222CNE4	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS222IDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRS222IN	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TRS222INE4	ACTIVE	PDIP	N	18	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

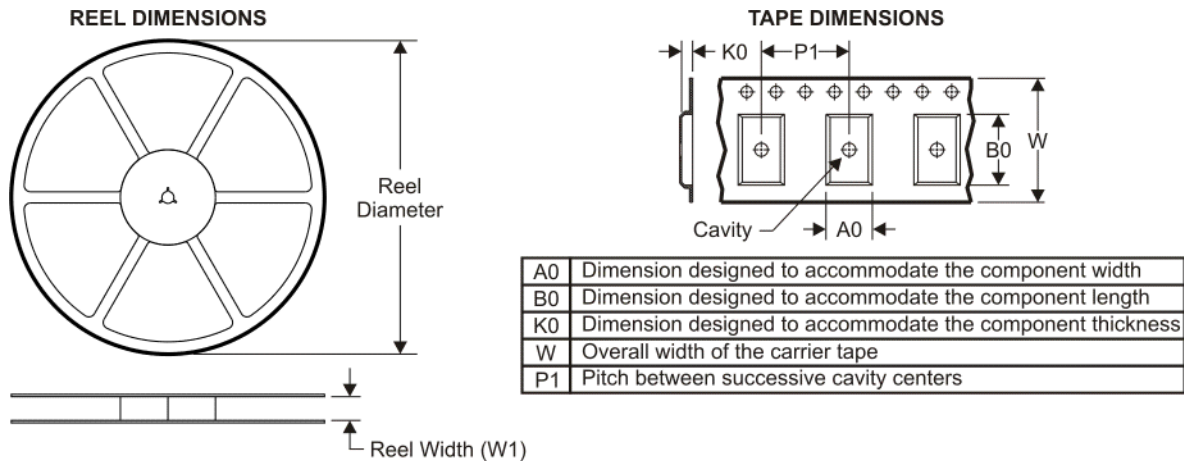
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

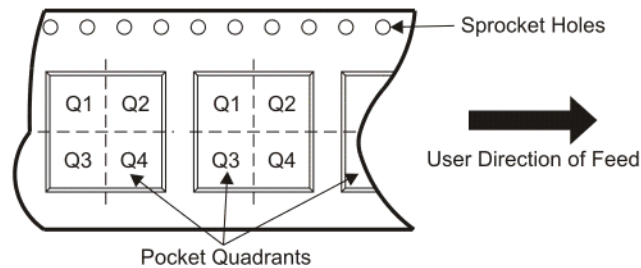
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS222CDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
TRS222IDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

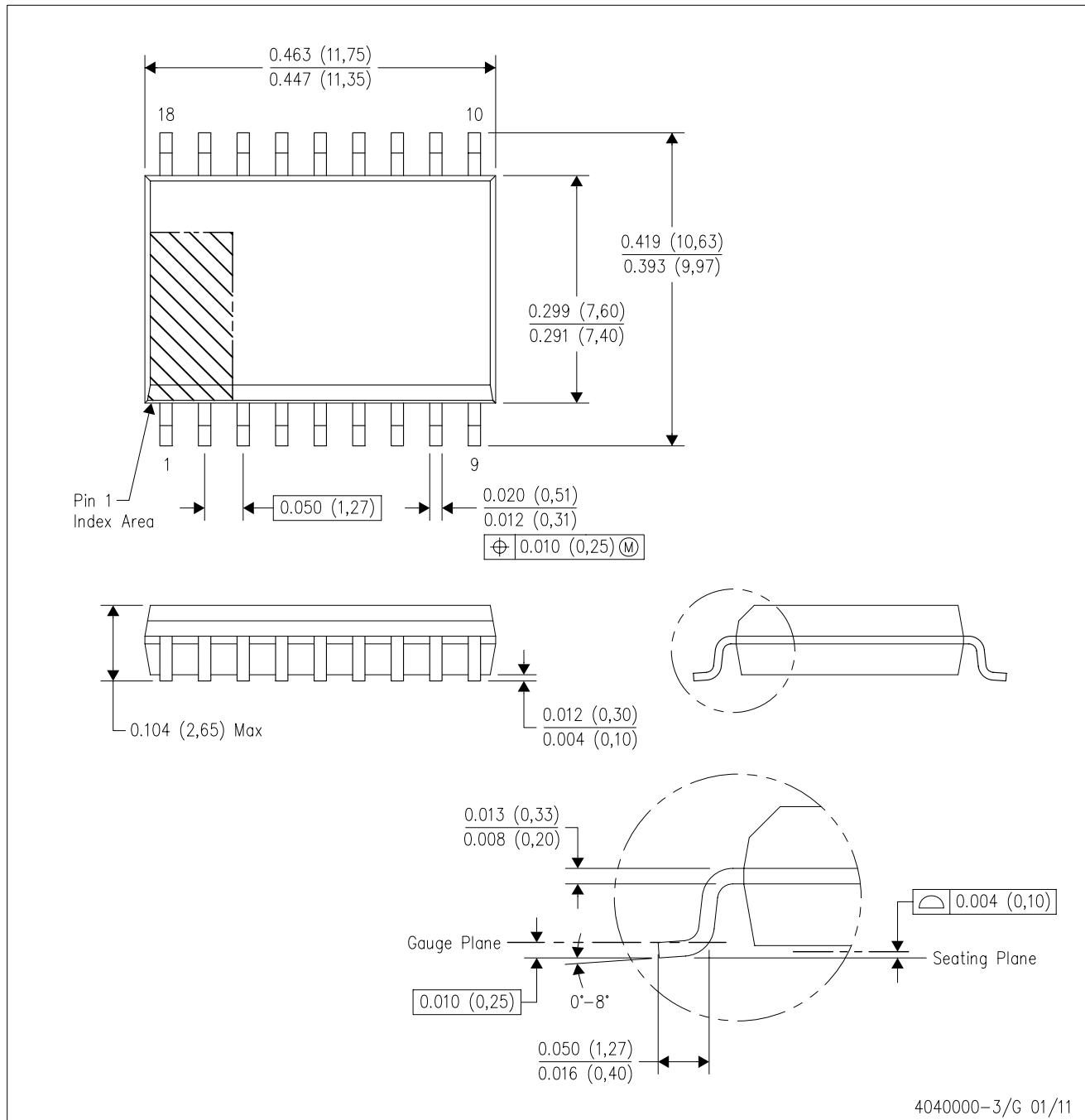
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS222CDWR	SOIC	DW	18	2000	370.0	355.0	55.0
TRS222IDWR	SOIC	DW	18	2000	370.0	355.0	55.0

DW (R-PDSO-G18)

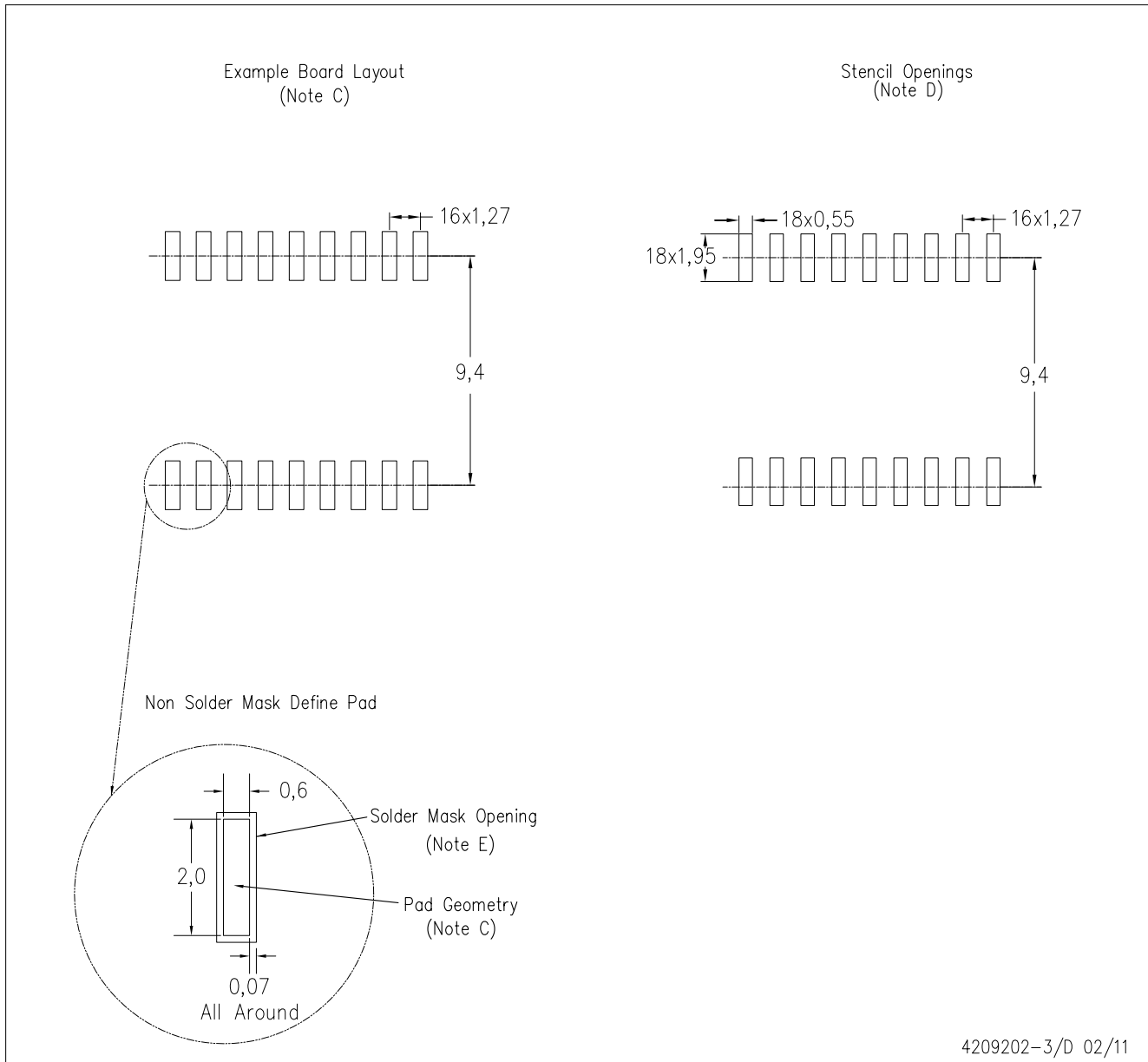
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AB.

DW (R-PDSO-G18)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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