Am29C861A/Am29C863A

High Performance CMOS Bus Transceivers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-speed CMOS bidirectional bus transceivers**
  - T-R delay = 4 ns typical
- **Low standby power**
- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military
- **200-mV typical hysteresis on data input ports**
- **Proprietary edge-rate controlled outputs dramatically reduce undershoots, overshoots, and ground bounce**
- **Power-up/down disable circuit provides for glitch-free power supply sequencing**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **Minimal speed degradation with multiple outputs switching**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C861A and Am29C863A CMOS Bus Transceivers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. The Am29C861A is a 10-bit bidirectional transceiver; the Am29C863A is a 9-bit transceiver with NORed output enables for maximum control flexibility. Each device features data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C861A and Am29C863A are produced with AMD's exclusive CS11SA CMOS process, and features a typical propagation delay of 4 ns, as well as an output current drive of 48 mA.

The Am29C861A and Am29C863A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce), undershoots and overshoots. By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuitry which utilizes n-channel pull-up transistors (eliminating the parasitic diode to V_{CC}) provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C861A and Am29C863A are available in the standard package options: DIPs, PLCCs, and SOICs.

* For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

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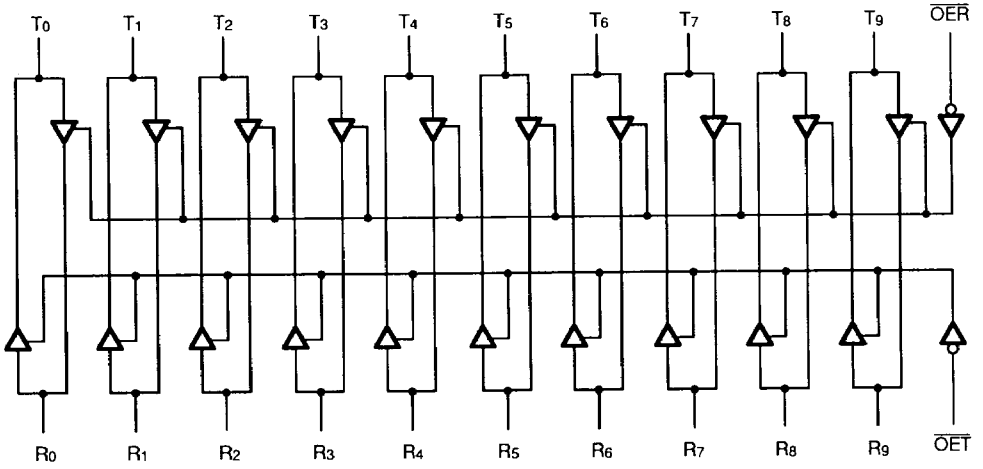
BLOCK DIAGRAMS

Am29C861A



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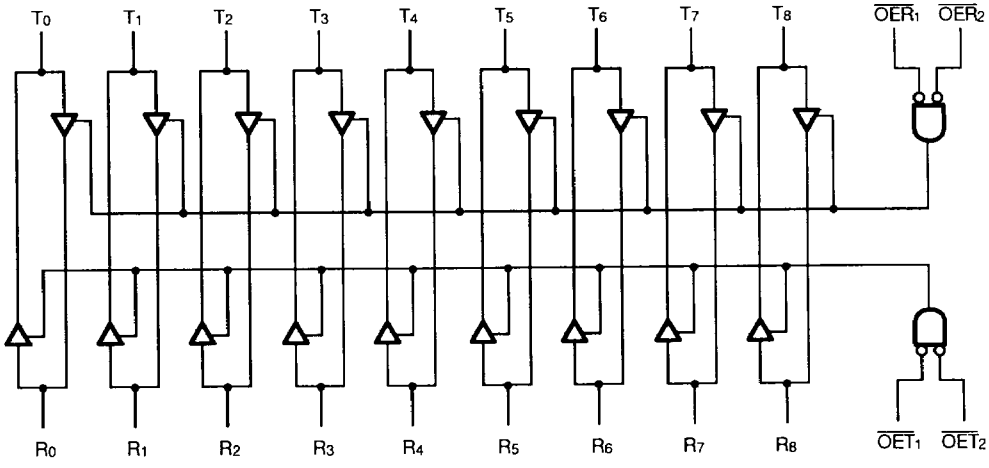

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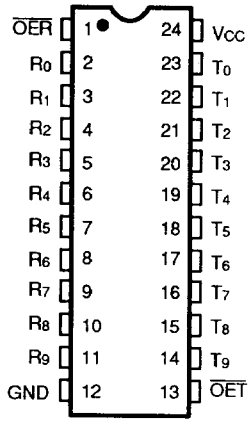
CONNECTION DIAGRAMS
Top View
Am29C861A

DIP*



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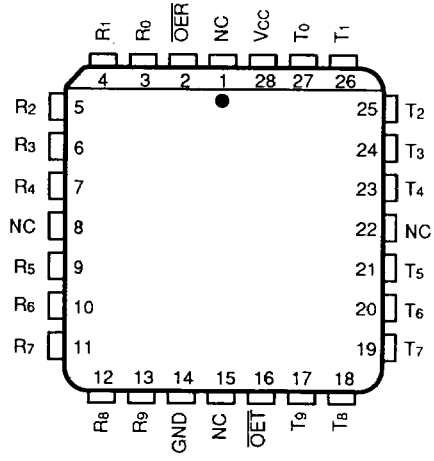
PLCC



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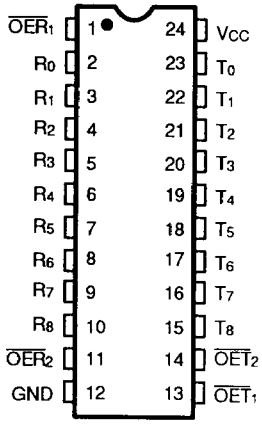
DIP*



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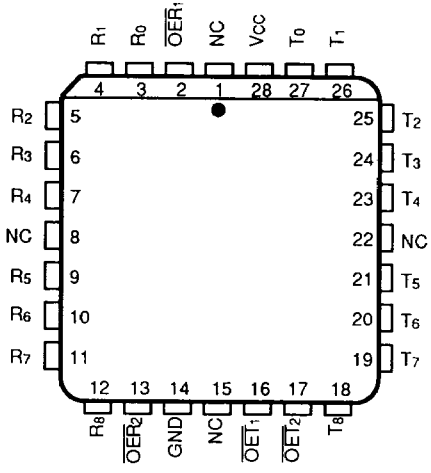
PLCC



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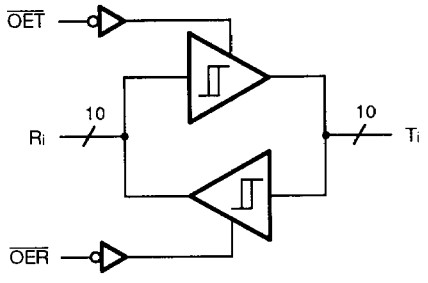
*Also available in 24-Pin Small Outline Package; pinout identical to DIPs.

Note:
Pin 1 is marked for orientation

LOGIC SYMBOLS

Am29C861A



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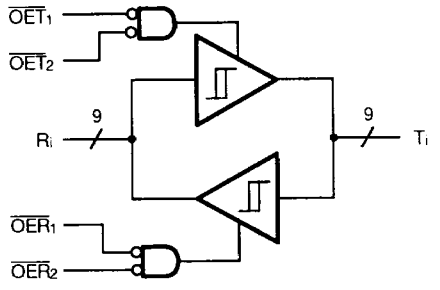

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FUNCTION TABLES

Am29C861A

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	Function
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

Am29C863A

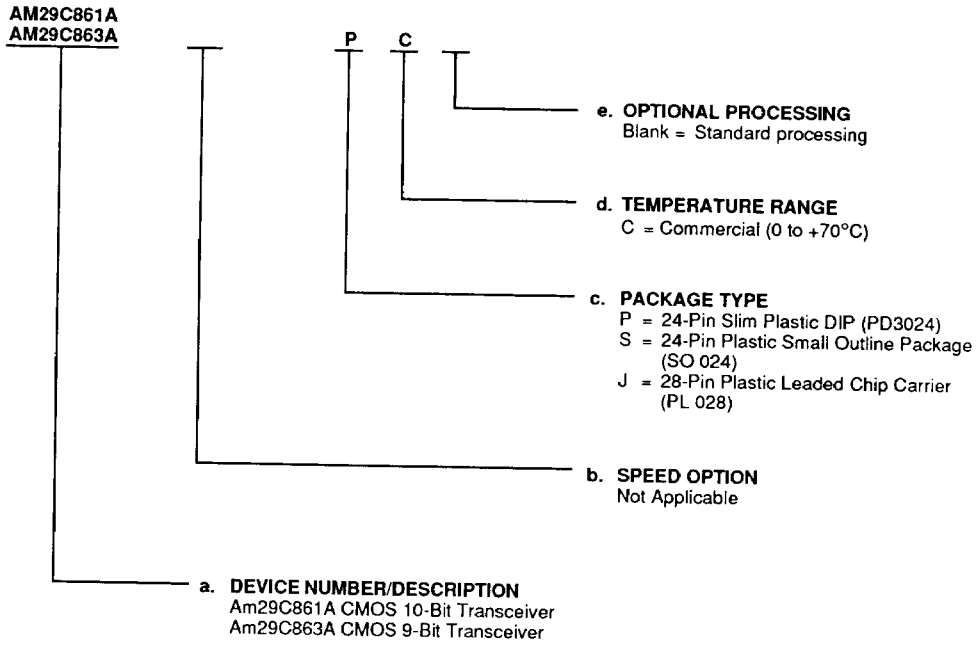
Inputs						Outputs		
$\overline{OET}_1$	$\overline{OET}_2$	$\overline{OER}_1$	$\overline{OER}_2$	R_i	T_i	R_i	T_i	Function
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H = HIGH NC = Not Applicable
L = LOW Z = High Impedance
X = Don't Care

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C861A	PC, SC, JC
AM29C863A	

Valid Combinations

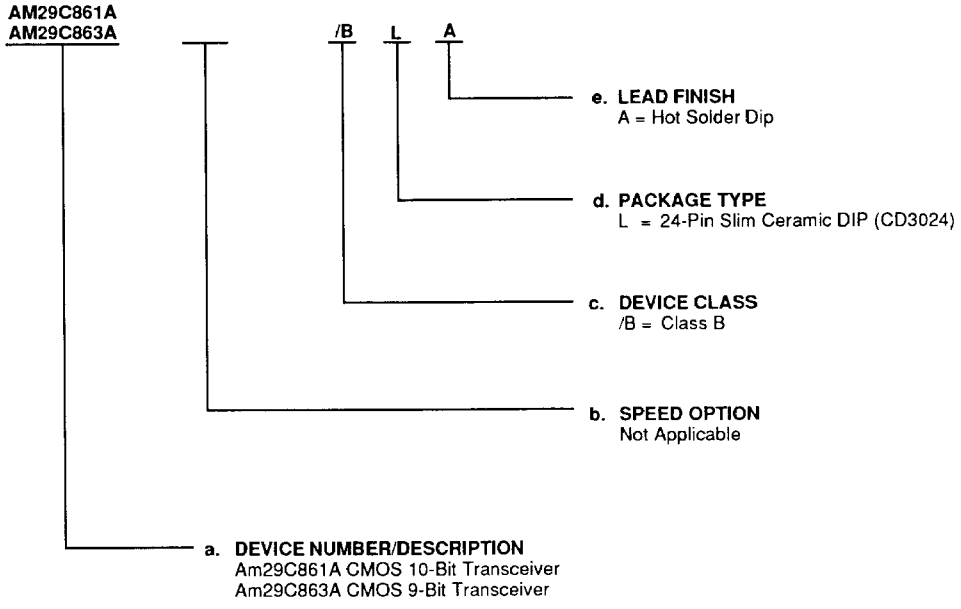
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29C861A	/BLA
AM29C863A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C861A Only

$\overline{OER}$

Output Enable Receive (Input, Active Low)

When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$

Output Enable Transmit (Input, Active Low)

When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are output).

R_i

Receive Port (Input/Output)

R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i

Transmit Port (Input/Output)

T_i are the10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Am29C863A Only

$\overline{OER_i}$

Output Enables Receive (Input, Active Low)

When both $\overline{OER_1}$ and $\overline{OER_2}$ are LOW while $\overline{OET_1}$ or $\overline{OET_2}$ (or both) are HIGH, the device is in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET_i}$

Output Enables Transmit (Input, Active Low)

When both $\overline{OET_1}$ and $\overline{OET_2}$ are LOW while $\overline{OER_1}$ or $\overline{OER_2}$ (or both) are HIGH, the device is in the Transmit mode (R_i are inputs, T_i are outputs).

R_i

Receive Port (Input/Output)

R_i are the 9-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i

Transmit Port (Input/Output)

T_i are the 9-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature		−65 to +150°C
Supply Voltage to Ground Potential Continuous		−0.5 V to +7.0 V
DC Output Voltage		−0.5 V to +6.0 V
DC Input Voltage		−0.5 V to +6.0 V
DC Output Diode Current:	Into Output	+ 50 mA
	Out of Output	− 50 mA
DC Input Diode Current:	Into Input	+ 20 mA
	Out of Input	− 20 mA
DC Output Current:	Into Output	+ 100 mA
	Out of Output	− 100 mA

Total DC Ground Current ($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)

Total DC V_{CC} Current ($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Military (M) Devices

Ambient Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32 mA			0.5	V
			COM'L, I_{OL} = 48 mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V Input Only	V_{IN} = 0 V			−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V Input Only	V_{IN} = 5.5 V			5	µA
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 5.5 V			10	µA
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0 V			−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/ Bit
				$\overline{OER_1}$, $\overline{OER_2}$ $\overline{OET_1}$, $\overline{OET_2}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)	Outputs Open			275	µA/ MHz/ Bit
			Outputs Loaded			400	

Notes:

1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output should be shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ≤ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capacitive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Am29C861A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	2	7	2	8	ns
t_{PHL}			2	8	2	9	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	10	2	11	ns
t_{ZL}			2	12.5	2	13.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		1.5	9	1.5	10	ns
t_{LZ}			1.5	10	1.5	11	ns

Am29C863A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	2	7	2	8	ns
t_{PHL}			2	8	2	9	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	10.5	2	11.5	ns
t_{ZL}			2	12.5	2	13.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		1.5	10	1.5	11	ns
t_{LZ}			1.5	11	1.5	12	ns

* See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified (Note 2)

Am29C861A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	C_L = 300 pF, R_1 = 500 Ω, R_2 = 500 Ω	2	14.5	2	15.5	ns
t_{PHL}			2	15.5	2	16.5	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	16.5	2	17.5	ns
t_{ZL}			2	20.5	2	21.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 5 pF, R_1 = 500 Ω, R_2 = 500 Ω	1.5	7	1.5	8	ns
t_{LZ}			1.5	8.5	1.5	9.5	ns

Am29C863A

Parameter Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i (Note 1)	C_L = 300 pF, R_1 = 500 Ω, R_2 = 500 Ω	2	14.5	2	15.5	ns
t_{PHL}			2	15.5	2	16.5	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i		2	16.5	2	17.5	ns
t_{ZL}			2	20.5	2	21.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 5 pF, R_1 = 500 Ω, R_2 = 500 Ω	1.5	7	1.5	8	ns
t_{LZ}			1.5	8.5	1.5	9.5	ns

* See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
2. These parameters are guaranteed by characterization but not production tested.