A Product Line of
Diodes Incorporated

PI3A412

0.4Ω, 3.3V, Quad SPDT Analog Switch

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.4Ω (+2.7V Supply)
- Wide VCC Range: +1.6V to +4.2V
- 1.8V Logic Control Tolerable
- Rail-to-Rail switching throughout Signal Range
- Fast Switching Speed: 20ns TYP. at 3.3V
- High Off Isolation: -65dB
- Crosstalk Rejection: -65dB
- Extended Industrial Temperature Range: –40°C to 85°C
- 3kV HBM ESD protection
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging: (Pb-free & Green)
  - 16-contact TQFN (ZH), 3.0mm x 3.0mm

Applications

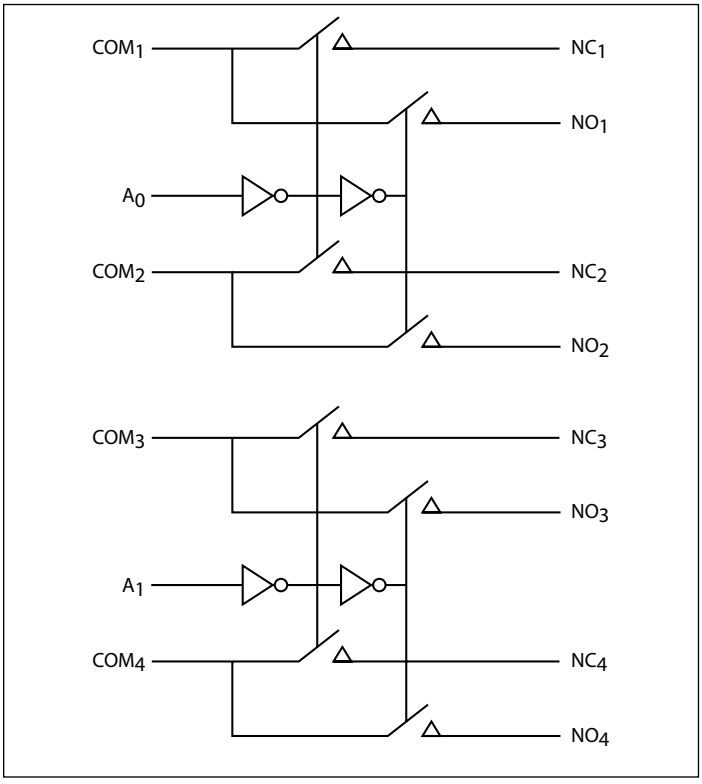
- Cell Phones
- PDAs
- Portable Instrumentation
- Battery Powered Communications
- Computer Peripherals
- Audio & Video Signal Routing
- PCMCIA Cards
- Modems
- Hard Drives
- JTAG Testing

Description

The PI3A412 is a quad single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, +1.6V to +4.2V, the switch has an On-Resistance of 0.4Ω at 2.7V.

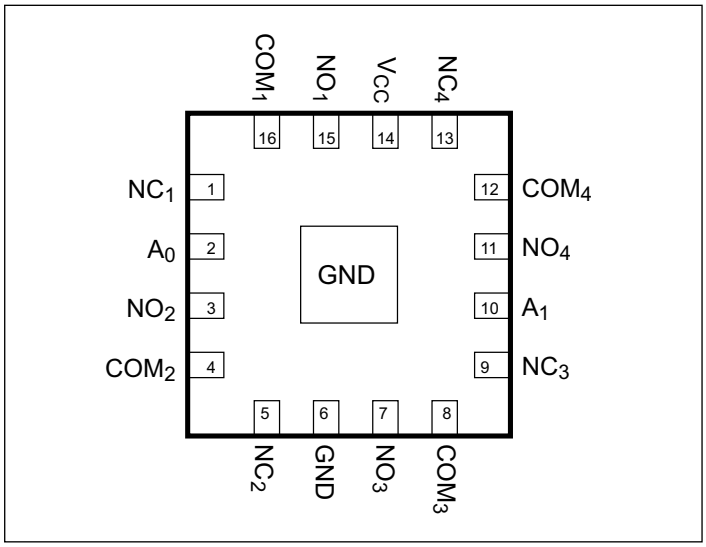
Control inputs, Ax, tolerates input drive signals up to 5V, independent of supply voltage.

Block Diagram



Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration



Pin Description

Pin #	Pin Name	Description
4, 8, 12, 16	COM_X	Common Output / Data Port
1, 5, 9, 13	NC_X	Data Port (normally connect)
3, 7, 11, 15	NO_X	Data Port (normally open)
2, 10	A_0, A_1	Logic Input Control
6	GND	Ground
14	V_{CC}	Positive Power Supply

Notes :

1. X = 1, 2, 3, or 4

Function Tables

A_0	Function
0	NC_X Connected to COM_X
1	NO_X Connected to COM_X

A_1	Function
0	NC_Y Connected to COM_Y
1	NO_Y Connected to COM_Y

Notes :

1. X = 1 or 2
2. Y = 3 or 4

Absolute Maximum Ratings

Voltages Referenced to GND
V_{CC} ..... 1.5V to +4.6V
V_{NOx}, V_{NCx}, V_{COMx}, V_{Ax} (1) .....–0.5V to V_+ +0.3V
or 30mA, whichever occurs first
Current (any terminal)..... ±400mA
Peak Current, V_{NC+} V_{NO}
(Pulsed at 1ms, 10% duty cycle)..... ±500mA

Thermal Information

Continuous Power Dissipation
16-pin Thin QFN (derate 7.1mW/ºC above +70ºC)..... 0.5W
Storage Temperature .....–65ºC to +150ºC
Lead Temperature (soldering, 10s) ..... +300ºC

Note 1: Signals on NC, NO, COM, or A exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +3.3V Supply

(V_{CC} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.3V, V_{IL} = 0.5V) (T_A = –40°C to +85°C)

Symbol	Parameter	Conditions	Min.(1)	Typ.(2)	Max.(1)	Units
V_{ANALOG}	Analog Signal Range(3)		0		V_{CC}	V
R_{ON}	On Resistance	V_{CC} = 2.7V, I_{COM} = 100mA, V_{IN} = +1.5V		0.4	0.6	Ω
ΔR_{ON}	On-Resistance Match Between Channels(4)			0.08	0.09	
$R_{FLAT(ON)}$	On-Resistance Flatness(5)	V_{CC} = 2.7V, I_{COMx} = 100mA, V_{IN} = 0.8V, 2.0V		0.1	0.15	
I_{NC} (off) or I_{NO} (off)	Off Leakage Current(6)	V_{CC} = 3.6V, V_{NO} or V_{NC} = 0.3V, 3.3V	-400		400	nA
$I_{COMx\ (on)}$	On Leakage Current(6)	V_{CC} = 3.6V, V_{COMx}= 0.3V, 3.3V	-400		400	

Notes:
1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are T_A = 25°C, V_{CC} = 3.3V unless otherwise specified.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ match between channels
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.

Electrical Specifications - Single +4.2V Supply

(V_{CC} = +4.2V, GND = 0V, V_{IH} = 1.6V, V_{IL} = 0.7V) (T_A = –40°C to +85°C)

Symbol	Parameter	Conditions	Min.(1)	Typ.(2)	Max.(1)	Units
V_{ANALOG}	Analog Signal Range(3)		0		V_{CC}	V
R_{ON}	On Resistance	V_{CC} = 4.0V, I_{COMx} = 100mA, V_{IN} = +1.5V		0.4	0.6	Ω
ΔR_{ON}	On-Resistance Match Between Channels(4)			0.08	0.09	
$R_{FLAT(ON)}$	On-Resistance Flatness(5)	V_{CC} = 4.0V, I_{COMx} = 100mA, V_{IN} = 0.8V, 2.0V		0.1	0.15	
I_{NC} (off) or I_{NO} (off)	Off Leakage Current(6)	V_{CC} = 4.2V, V_{NO} or V_{NC} = 0.3V, 3.3V	-500		500	nA
I_{COMx} (on)	On Leakage Current(6)	V_{CC} = 4.2V, V_{COMx} = 0.3V, 3.3V	-500		500	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are T_A = 25°C, V_{CC} = 4.2V unless otherwise specified.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ match between channels
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.

Electrical Specifications - Single +4.2V Supply

(V_{CC} = +4.2V, GND = 0V, V_{IH} = 1.6V, V_{IL} = 0.7V) (T_A = –40°C to +85°C)

Parameter	Description	Test Conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
Logic Input						
V_{IH}	Input High Voltage	Guaranteed logic High Level	1.6			V
V_{IL}	Input Low Voltage	Guaranteed logic Low Level			0.7	
I_{AH}	Input Current with Voltage High	V_A = 1.4V, all others = 0.5V	–1		1	µA
I_{AL}	Input Current with Voltage Low	V_A = 0.5V, all other = 1.4V	–1		1	
Dynamic						
t_{ON}	Turn-On Time	V_{CC} = 4.2V, V_{COM} = 2.0V, Figure 1 & 2		20	25	ns
t_{OFF}	Turn-Off Time			12	15	
t_{BBM}	Break-Before-Make	V_{IN} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 3	1	12	15	
Q	Charge Injection(3)	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4		100		pC
O_{IRR}	Off Isolation(4)	R_L = 50Ω, f = 100kHz, Figure 5		-65		dB
X_{TALK}	Cross Talk(5)	R_L = 50Ω, f = 100kHz, Figure 6		-65		
f_{3db}	3dB Bandwidth	See Test Circuit Figure 9		40		MHz
$C_{NC(OFF)}$	Off Capacitance	f = 1 MHz, Figure 7		50		pF
$C_{NO(OFF)}$	Off Capacitance			50		
C_{ON}	On Capacitance	f = 1 MHz, Figure 8		135		
Supply						
V_{CC}	Power-Supply Range		1.5		4.4	V
I_{CC}	Positve Supply Current	V_{CC} = 4.2V, V_A = 0V or V_{CC}			40	µA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are T_A = 25°C, V_{CC} = 4.2V unless otherwise specified.
3. Guaranteed by design.
4. Off Isolation = $20\log_{10}$ [(V_{NO} or V_{NC}) / V_{COM}]. See Figure 5.
5. Between any two switches. See Figure 6.

Electrical Specifications - Single +3.3V Supply

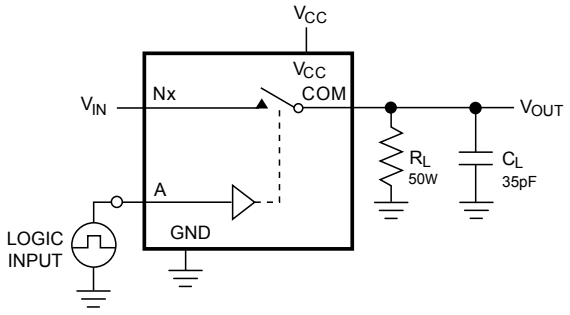
(V_{CC} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.3V, V_{IL} = 0.5V) (T_A = –40°C to +85°C)

Parameters	Description	Test Conditions	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input						
V_{IH}	Input High Voltage	Guaranteed logic High Level	1.3			V
V_{IL}	Input Low Voltage	Guaranteed logic Low Level			0.5	
I_{AH}	Input Current with Voltage High	V_A = 1.4V, all others = 0.5V	–1		1	µA
I_{AL}	Input Current with Voltage Low	V_A = 0.5V, all other = 1.4V	–1		1	
Dynamic						
t_{ON}	Turn-On Time	V_{CC} = 3.3V, V_{COM} = 2.0V, Figure 1 & 2		20	25	ns
t_{OFF}	Turn-Off Time			12	15	
t_{BBM}	Break-Before-Make	V_{IN} = 1.5V, R_L = 50Ω, C_L = 35pF, See Figure 3	1	12	15	
Q	Charge Injection(3)	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4		100		pC
O_{IRR}	Off Isolation(4)	R_L = 50Ω, f = 100kHz, Figure 5		-65		dB
X_{TALK}	Cross Talk(5)	R_L = 50Ω, f = 100kHz, Figure 6		-65		
f_{3db}	3dB Bandwidth	See Test Circiut Figure 9		40		MHz
$C_{NC(OFF)}$	Off Capacitance	f = 1 MHz, Figure 7		50		pF
$C_{NO(OFF)}$	Off Capacitance			50		
C_{ON}	On Capacitance	f = 1 MHz, Figure 8		135		

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are V_{CC} = 3.3V unless otherwise specified.
3. Guaranteed by design.
4. Off Isolation = $20\log_{10}$ [(V_{NO} or V_{NC}) / V_{COM}]. See Figure 5.
5. Between any two switches. See Figure 6.

Test Circuits and Timing Diagrams

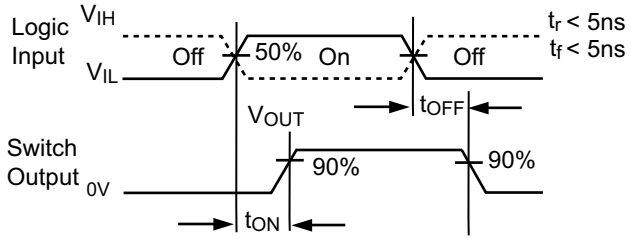


CL INCLUDES FIXTURE AND STRAY CAPACITANCE.

Figure 1. AC Test Circuit

Notes:

Unused N_X inputs must be grounded.



Logic Input Waveforms inverted for
Switches that have opposite logic

Figure 2. AC Waveforms

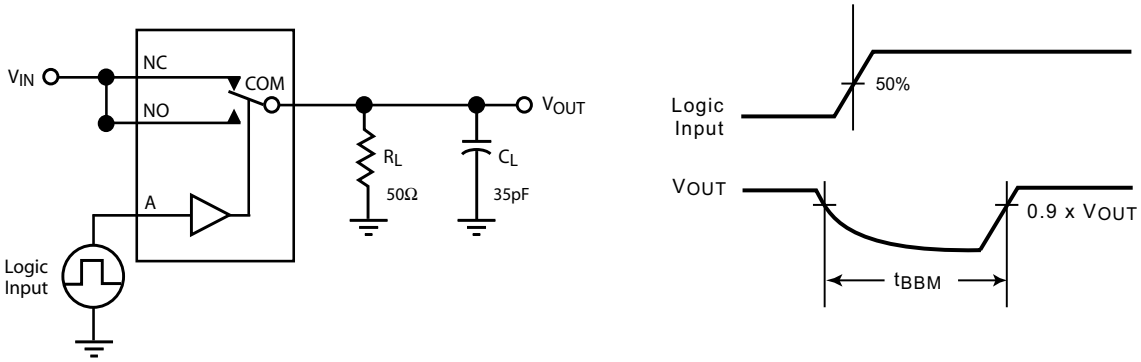


Figure 3. Break Before Make Interval Timing

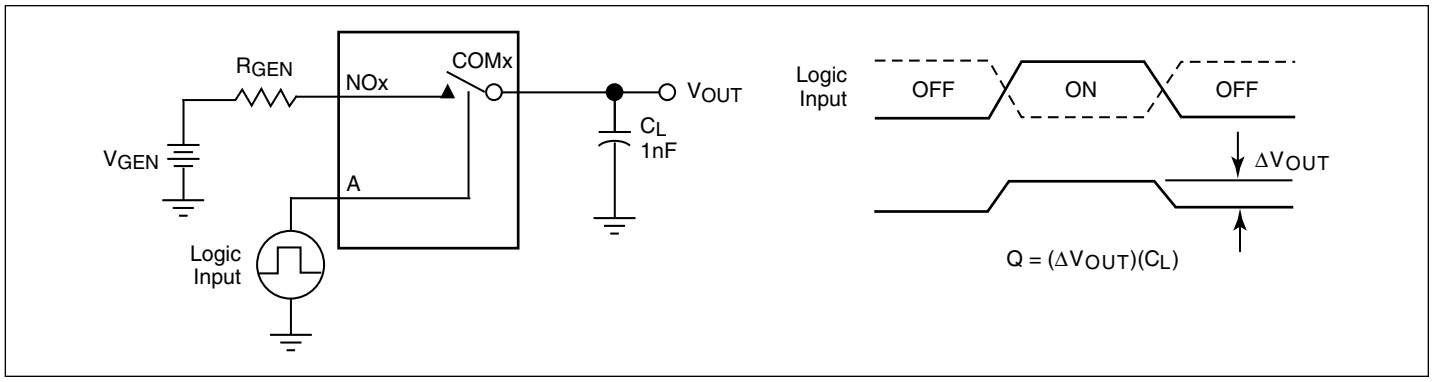


Figure 4. Charge Injection Test

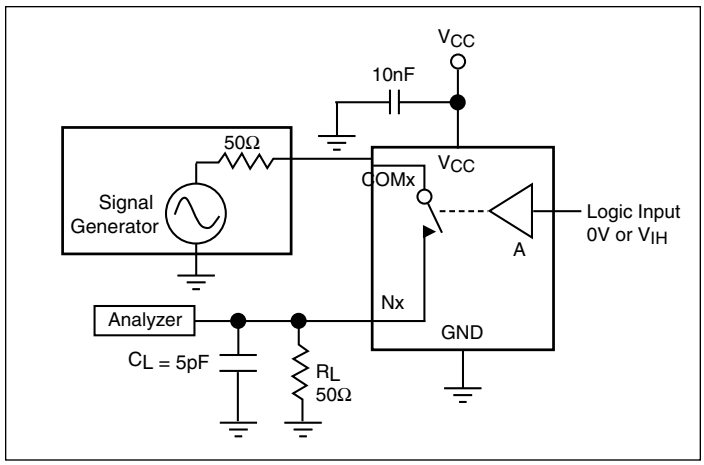


Figure 5. Off Isolation

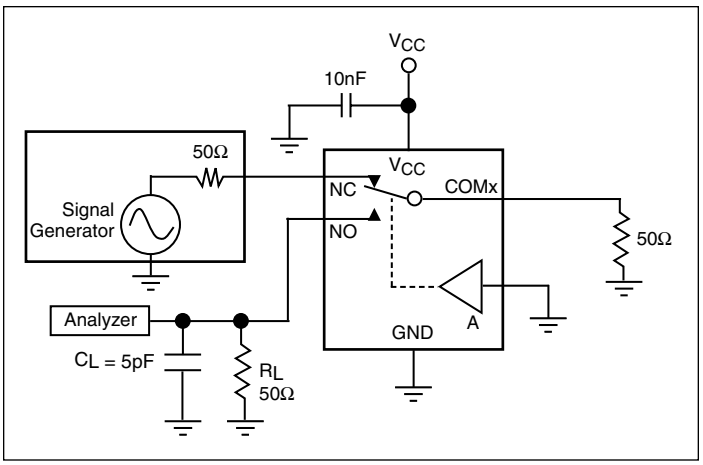


Figure 6. Crosstalk

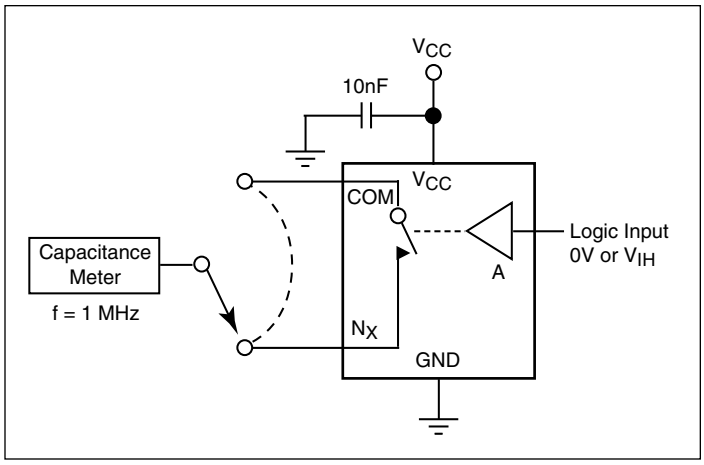


Figure 7. Channel Off Capacitance

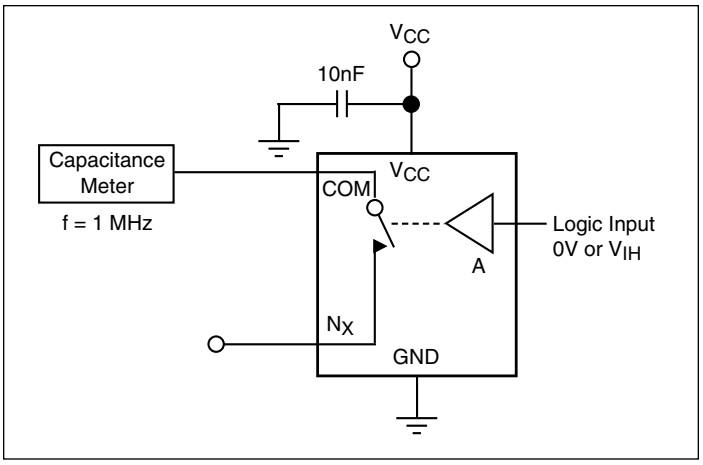


Figure 8. Channel On Capacitance

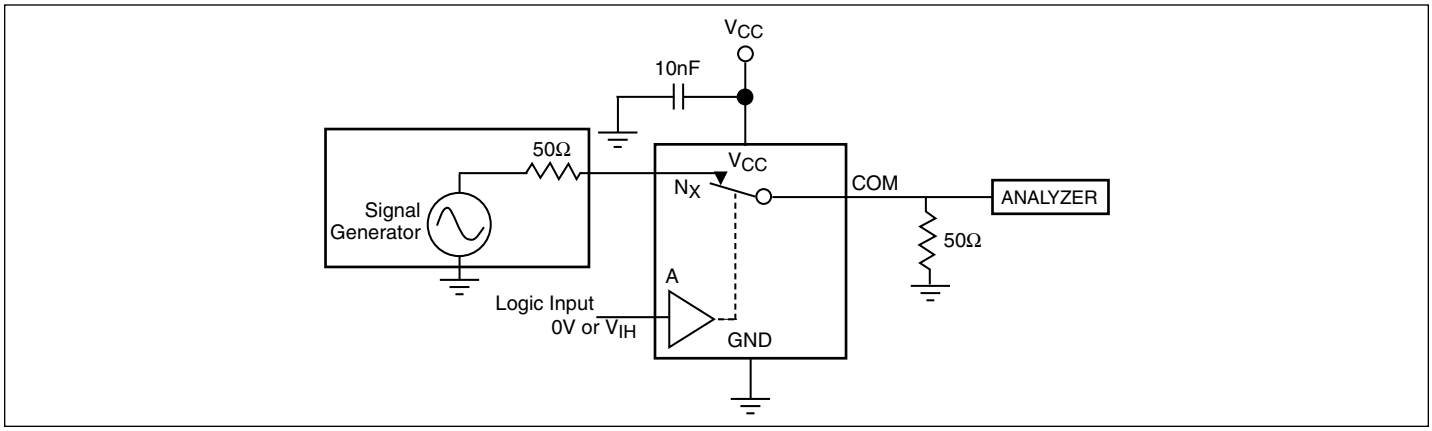
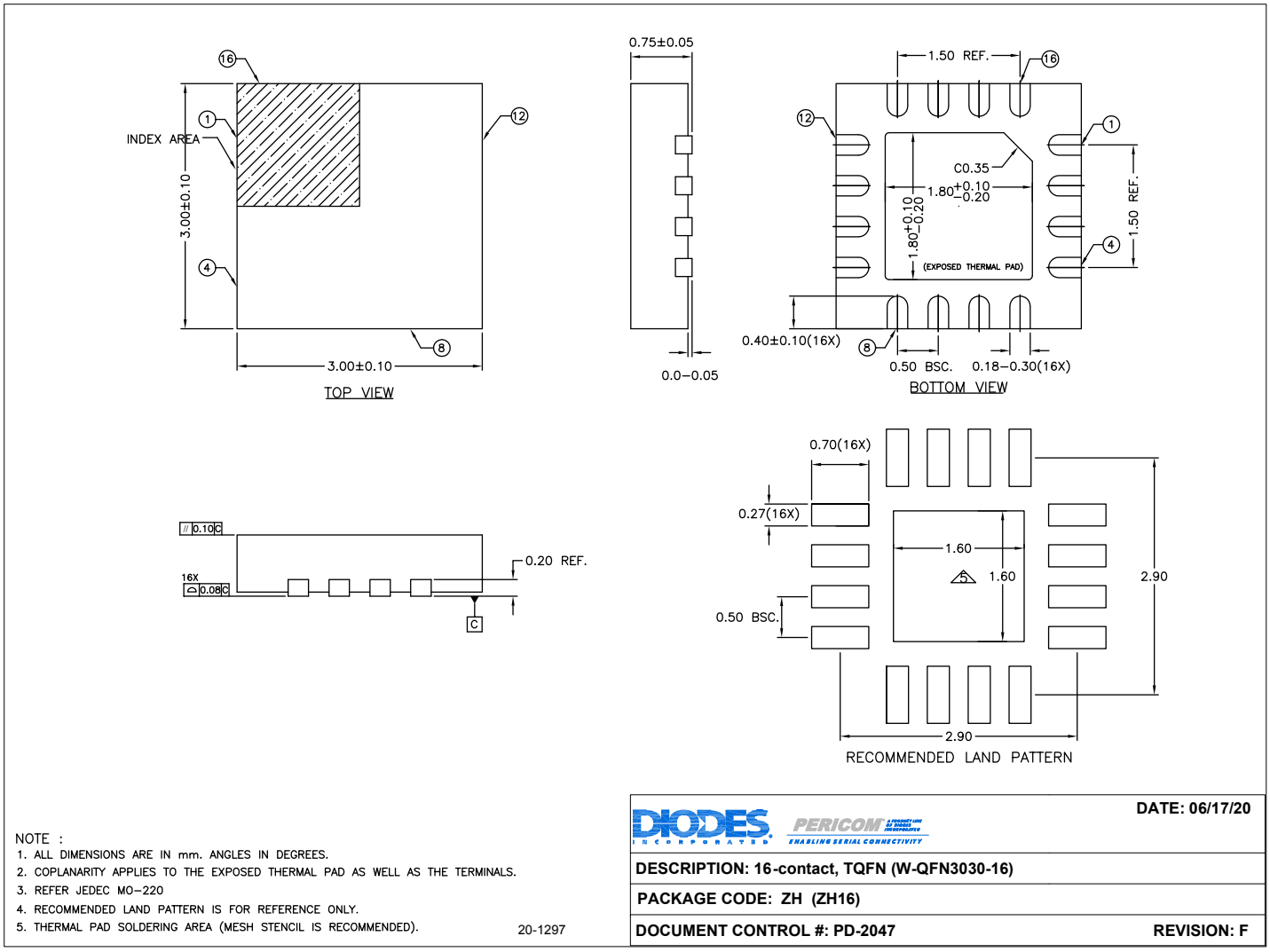


Figure 9. Bandwidth

Part Marking

PI3A412ZHE = A4ZHE
Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above Fab Code means Cu wire

Packaging Mechanical: 16-TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

20-1297

	DATE: 06/17/20
DESCRIPTION: 16-contact, TQFN (W-QFN3030-16)	
PACKAGE CODE: ZH (ZH16)	
DOCUMENT CONTROL #: PD-2047	REVISION: F

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Code	Package Code	Package Description
PI3A412ZHEX	ZH	16-contact, W-QFN3030-16 (TQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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