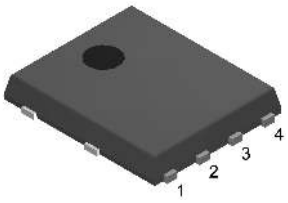
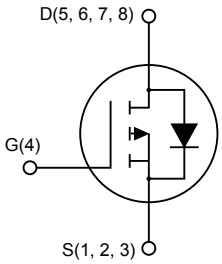
P-channel 40 V, 15.5 mΩ typ., 42 A STripFET F6 DeepGATE Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



AM01475v4

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL42P4LLF6	40 V	18 mΩ	42 A	75 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STL42P4LLF6

Product summary	
Order code	STL42P4LLF6
Marking	42P4LLF6
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	42	A
	Drain current (continuous) at T_C = 100 °C	29	A
I_{DM} (1)(3)	Drain current (pulsed)	168	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	10	A
	Drain current (continuous) at T_{pcb} = 100 °C	7.5	A
I_{DM} (2)(3)	Drain current (pulsed)	40	A
P_{TOT} (1)	Total power dissipation at T_C = 25 °C	75	W
P_{TOT} (2)	Total power dissipation at T_{pcb} = 25 °C	4.8	W
T_{stg}	Storage temperature	-55 to 175	°C
T_J	Maximum junction temperature	175	°C

1. *The value is limited by $R_{thj\text{-}case}$.*
2. *The value is limited by $R_{thj\text{-}pcb}$.*
3. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	2.00	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb, single operation	31.3	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu, steady state.*

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_C = 125 °C			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5 A		15.5	18	mΩ
		V_{GS} = 4.5 V, I_D= 5 A		21	26	

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2850	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Reverse transfer capacitance		-	180	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 10 A, V_{GS} = 4.5 V (see Figure 13. Gate charge test circuit)	-	22	-	nC
Q_{gs}	Gate-source charge		-	9.4	-	nC
Q_{gd}	Gate-drain charge		-	7.3	-	nC
R_g	Gate input resistance	I_D = 0 A, gate DC bias = 0 V, f = 1 MHz, magnitude of alternative signal = 20 mV	-	1.4	-	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Switching times test circuit for resistive load)	-	43	-	ns
t_r	Rise time		-	47	-	ns
$t_{d(off)}$	Turn-off-delay time		-	148	-	ns
t_f	Fall time		-	19	-	ns

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 5 A	-		1.1	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	26		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 32 V, T_J = 150 °C	-	21		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	1.7		A

1. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

Note: For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

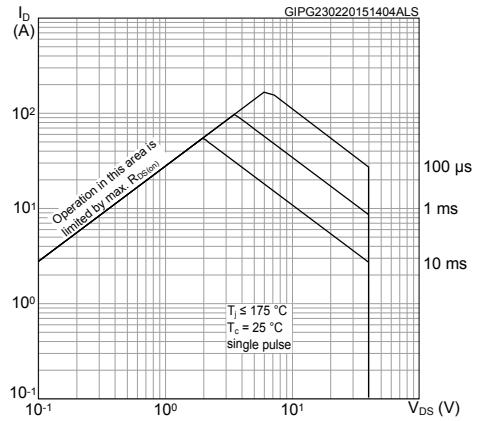


Figure 2. Thermal impedance

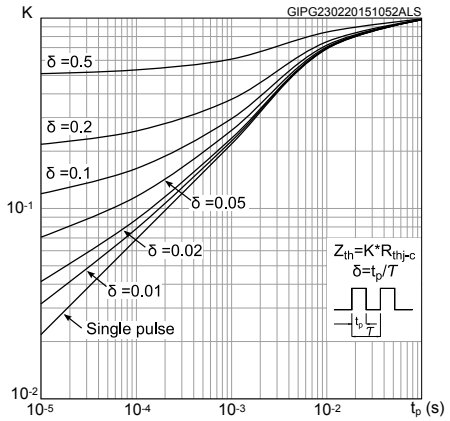


Figure 3. Output characteristics

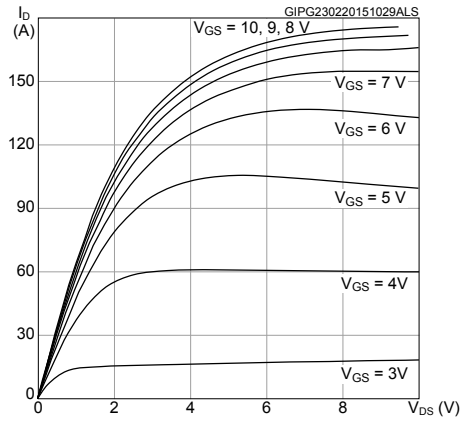


Figure 4. Transfer characteristics

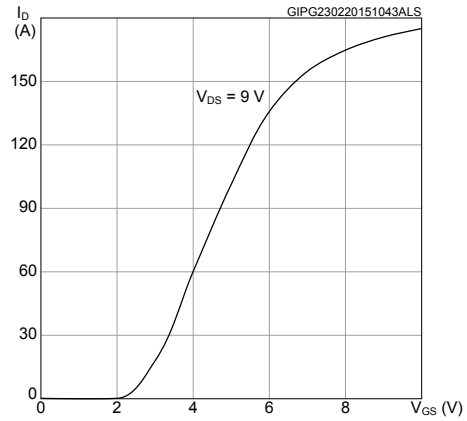


Figure 5. Normalized gate threshold voltage vs temperature

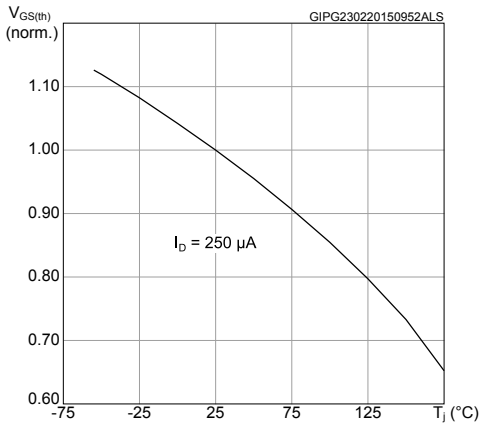


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

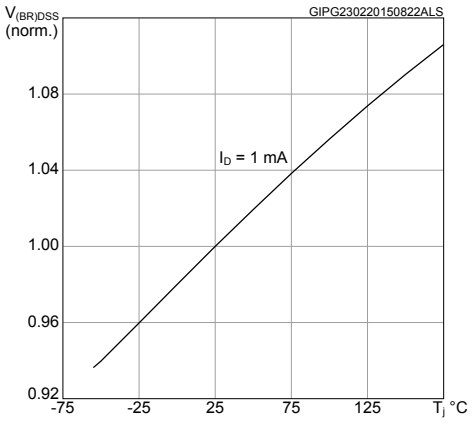


Figure 7. Static drain-source on-resistance

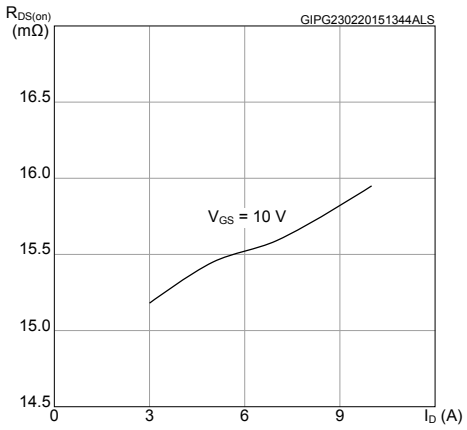


Figure 8. Normalized on-resistance vs. temperature

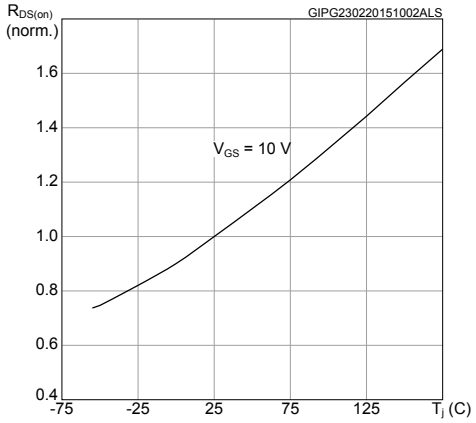


Figure 9. Gate charge vs gate-source voltage

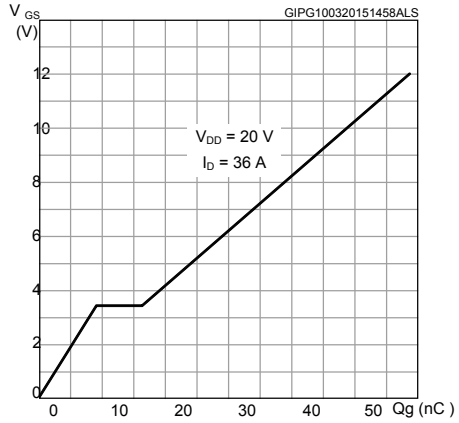


Figure 10. Capacitance variations voltage

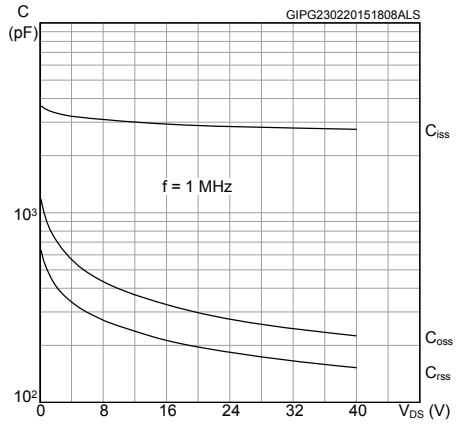
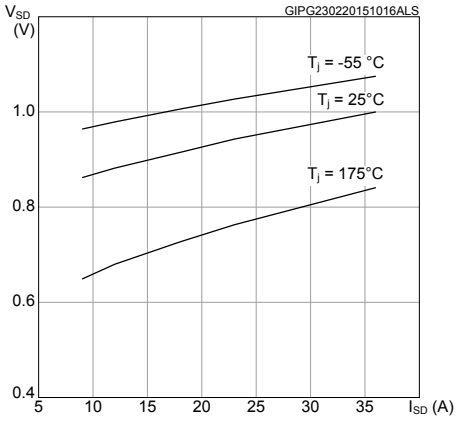


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load

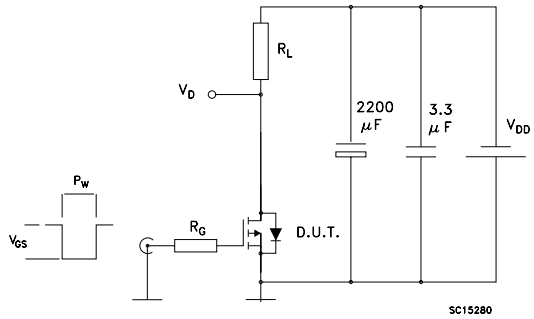


Figure 13. Gate charge test circuit

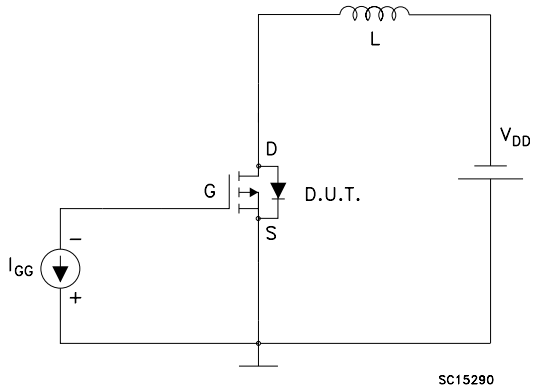
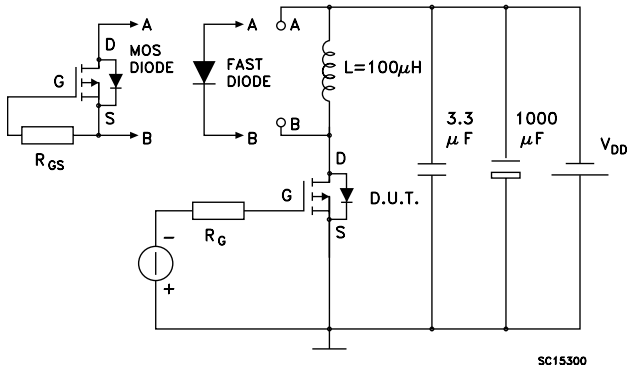


Figure 14. Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 5x6 type R package information

Figure 15. PowerFLAT 5x6 type R package outline

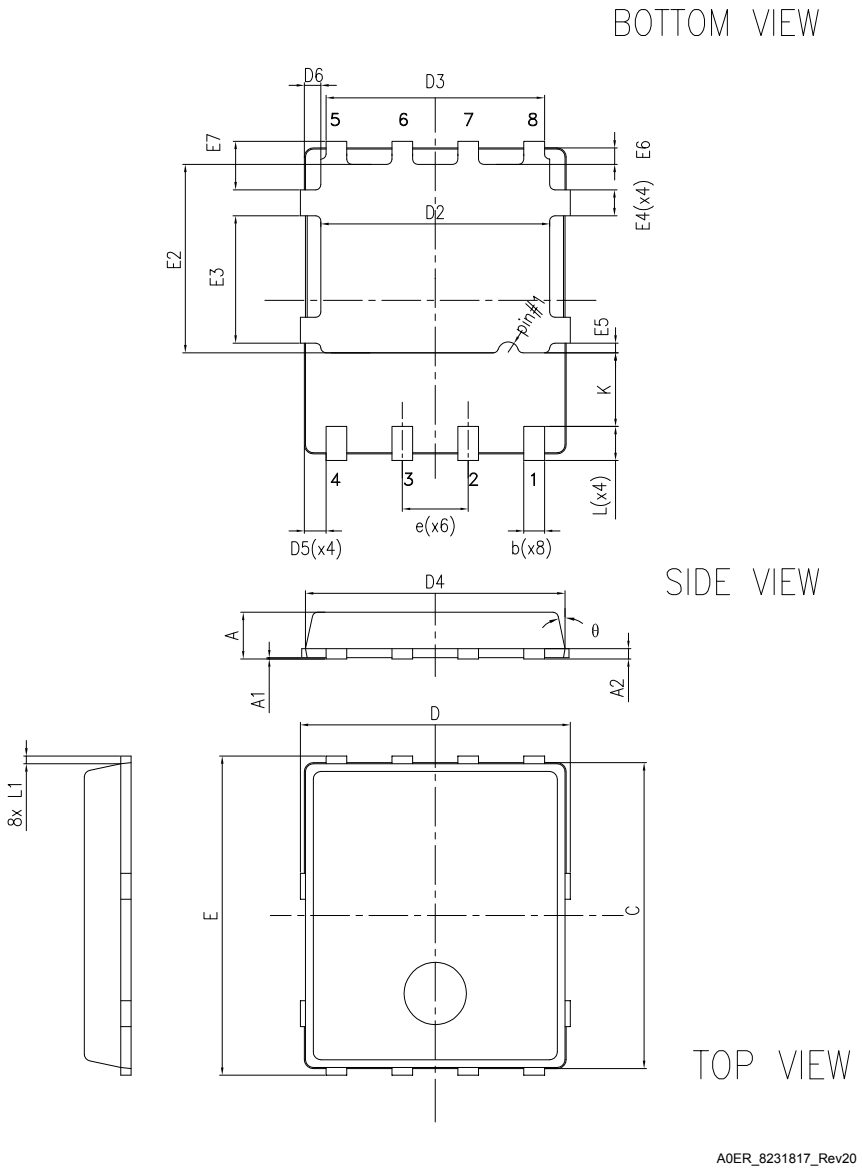


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Table 7. PowerFLAT 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

4.2 PowerFLAT 5x6 type R SUBCON package information

Figure 16. **PowerFLAT 5x6 type R SUBCON package outline**

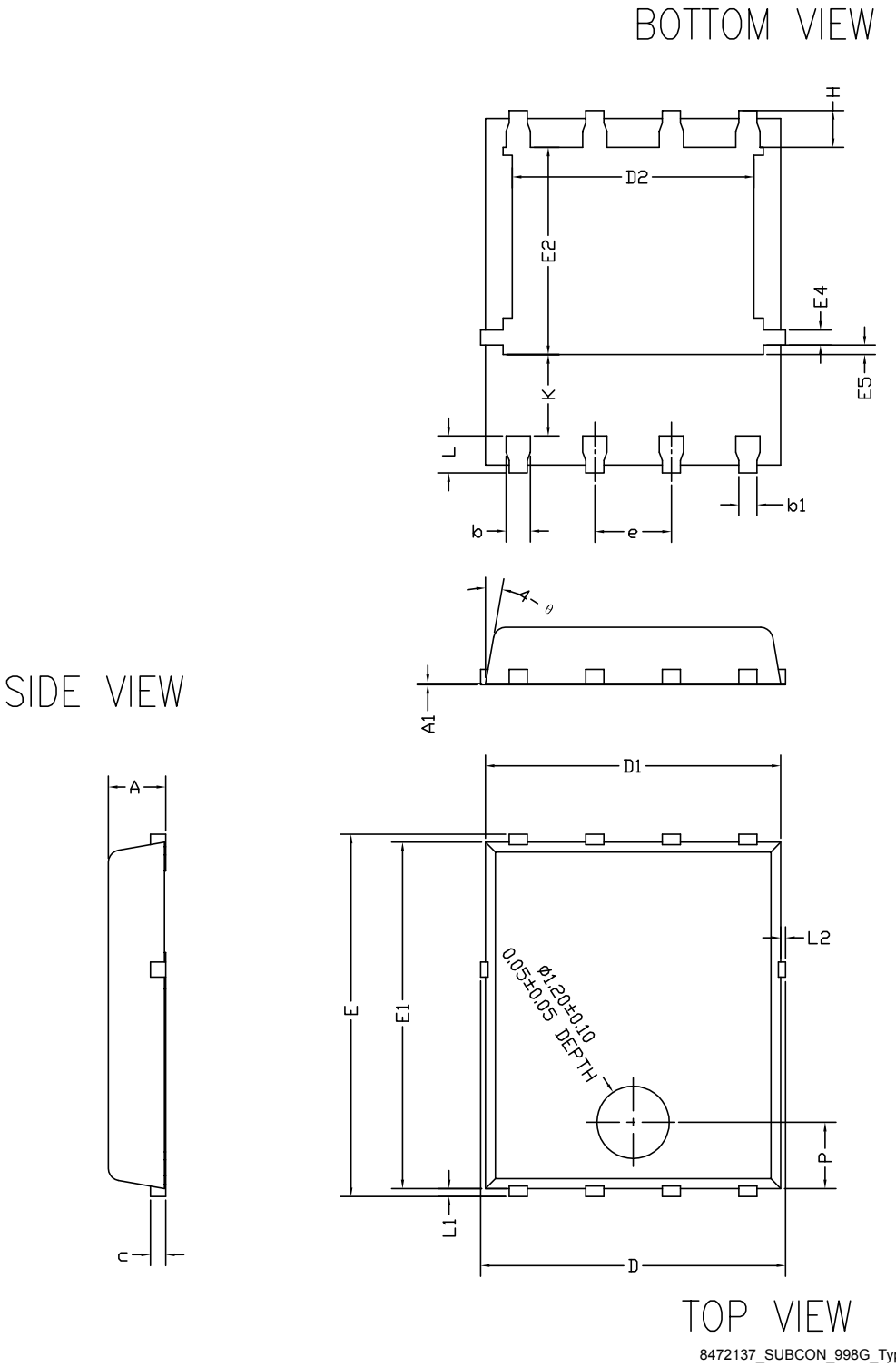
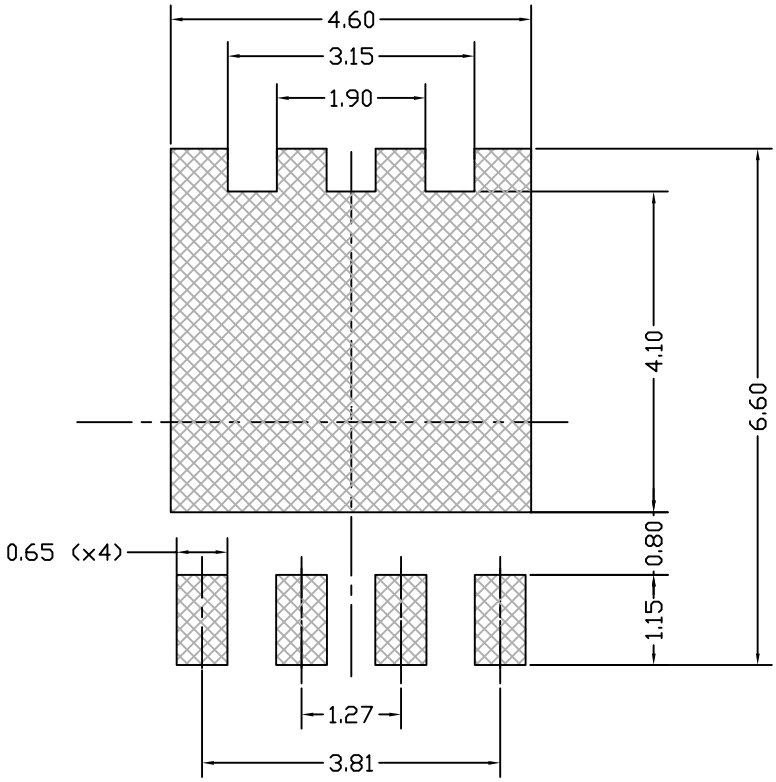


Table 8. PowerFLAT 5x6 type R SUBCON package mechanical data

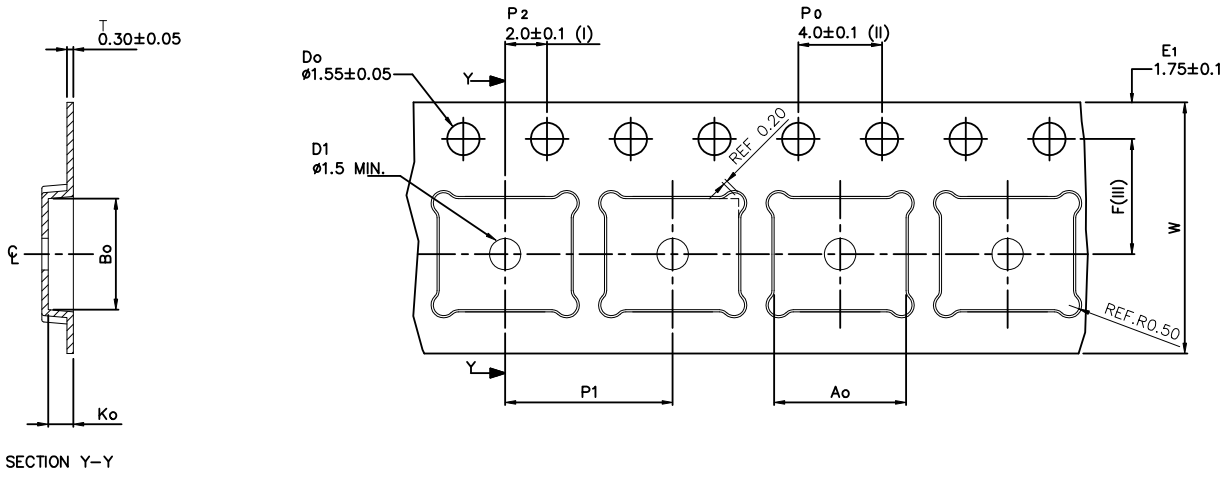
Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1		0.02	
b	0.35	0.40	0.45
b1		0.30	
c	0.21	0.25	0.34
D			5.10
D1	4.80	4.90	5.00
D2	3.91	4.01	4.11
e	1.17	1.27	1.37
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.34	3.44	3.54
E4	0.15	0.25	0.35
E5	0.06	0.16	0.26
H	0.51	0.61	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
L2			0.10
P	1.00	1.10	1.20
θ	8°	10°	12°

Figure 17. **PowerFLAT 5x6 recommended footprint (dimensions are in mm)**



4.3 PowerFLAT 5x6 packing information

Figure 18. PowerFLAT 5x6 tape (dimensions are in mm)



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 19. PowerFLAT 5x6 package orientation in carrier tape

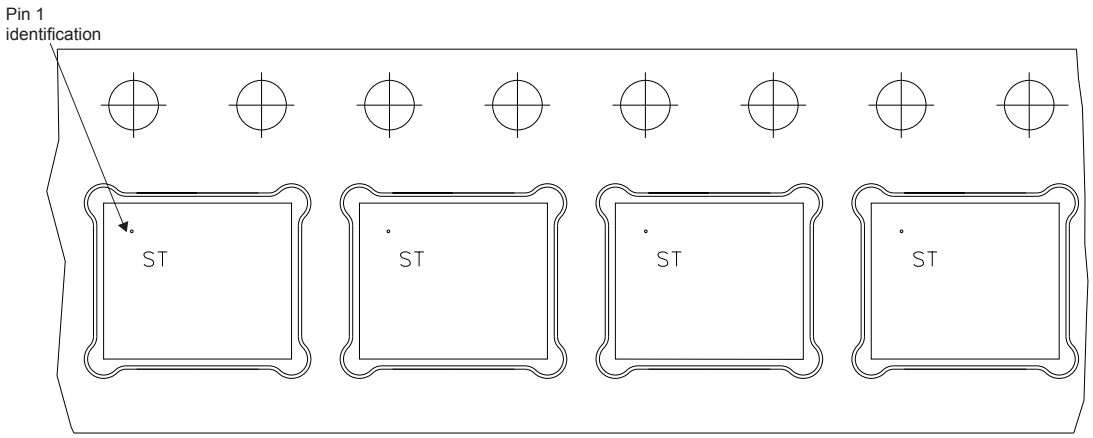
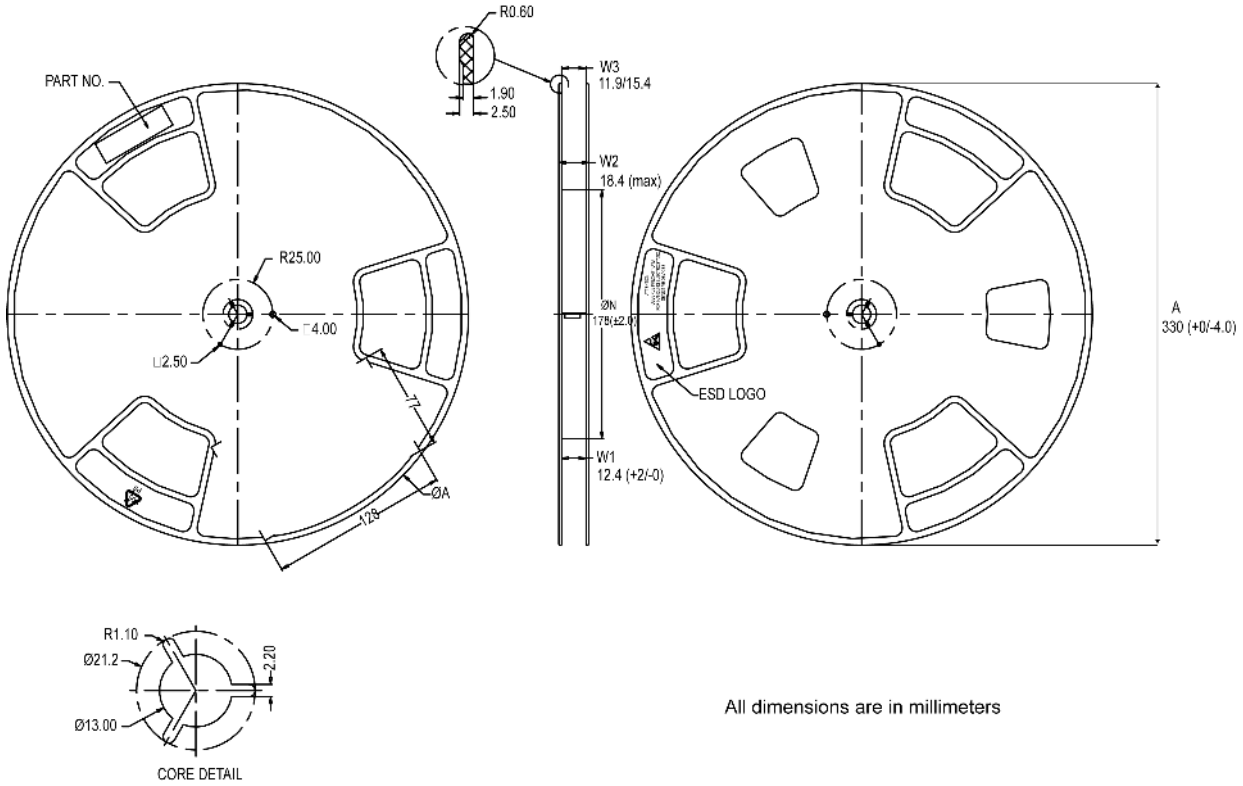


Figure 20. **PowerFLAT 5x6 reel**



Revision history

Table 9. **Document revision history**

Date	Revision	Changes
28-Jan-2014	1	Initial release.
25-Feb-2015	2	Text edits throughout document On cover page, updated title, description and features table Renamed and updated Table 4: Static Updated Table 5: Dynamic Updated Table 6: Switching times Updated Table 7: Source-drain diode Added Section 2.1: Electrical characteristics (curves) Renamed and updated Section 4.1 PowerFLAT™ 5x6 type R package information Renamed and updated Section 5 Packing information
18-Feb-2020	3	Updated Section 4 Package information. Minor text changes.

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