16 W non-isolated auxiliary power supply for outdoor air-conditioner using ICE5BR3995BZ

REF_5BR3995BZ_16W1

About this document

Scope and purpose

This document is a reference design for a 16 W auxiliary power supply for an invertized air-conditioner unit with the latest Infineon fifth-generation fixed-frequency (FF) CoolSET™ ICE5BR3995BZ. The power supply is designed with a universal input compatible with most geographic regions and three non-isolated outputs (12 V/900 mA, 15 V/150 mA and 5 V/300 mA), where 15 V output and 5 V output are supported by a linear regulator from an 18 V source and 8 V source respectively.

Highlights of the auxiliary power supply for the invertized air-conditioner unit are:

- Tightly regulated output voltages, high efficiency under light load and low standby power
- Comprehensive CoolSET™ protection feature
- Auto-restart protection scheme to minimize interruption and enhance end user experience

Intended audience

This document is intended for power supply design engineers who are designing auxiliary power supplies for outdoor air-conditioner units that are efficient, reliable and easy to design.

Table of contents

1 System introduction

With the growing household trend for internet-connected devices, the new generation of home appliances including air-conditioners are equipped with advanced features such as wireless control and monitoring capability, smart sensors and touch screen display. These can transform a static product into an interactive and intelligent home appliance, capable of adapting to the smart-home theme. Infineon has introduced the latest fifth-generation FF CoolSET™ to address this need in an efficient and cost-effective manner.

An auxiliary SMPS is needed to power the various modules and sensors, which typically operate from a stable DC voltage source. The Infineon CoolSET™ (as shown in **Figure 1**) forms the heart of the system, providing the necessary protection and AC-DC conversion from the mains to multiple regulated DC voltages to power the various blocks.

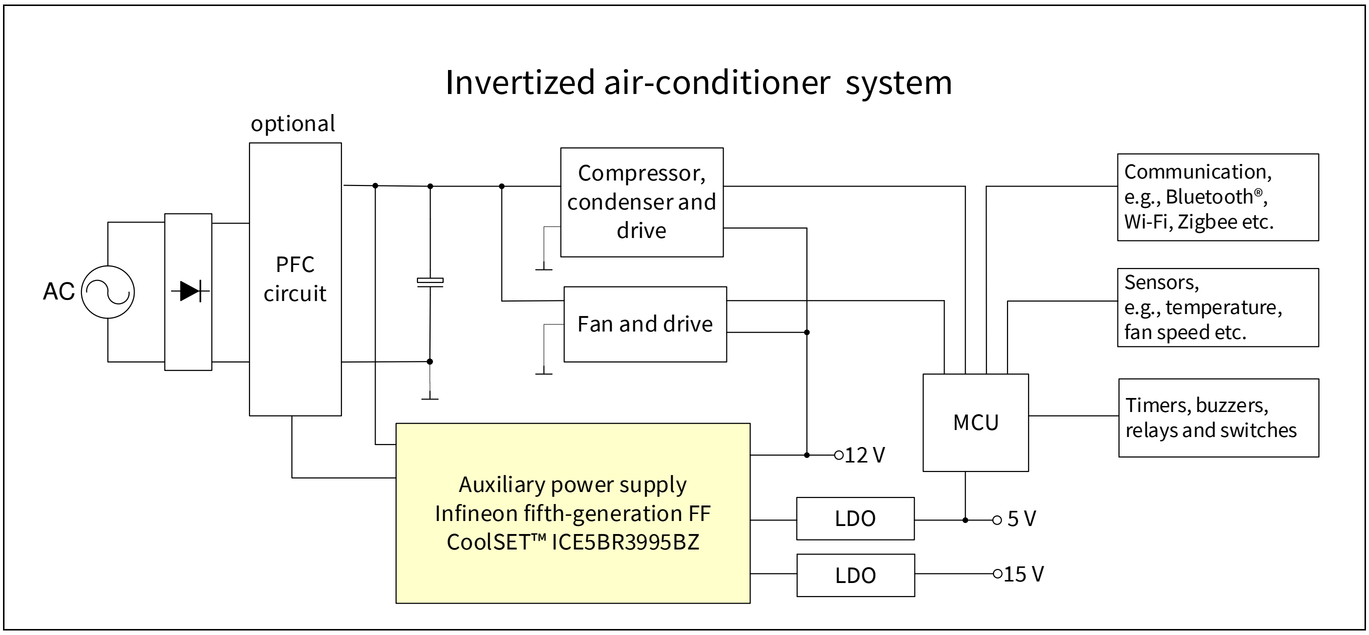


Figure 1 Simplified outdoor air-conditioner unit system block diagram example

Table 1 lists the system requirements for auxiliary power supply for the invertized air-conditioner unit, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for invertized air-conditioner unit power supply	**Infineon solution – ICE5BR3995BZ**
1	High efficiency under light load and low standby power	New FF control and active burst mode (ABM)
2	Robust system and protection features	Comprehensive protection feature CoolSET™ in DIP-7 package
3	Auto-restart protection scheme to minimize interruption and enhance end-user experience	All protections are in auto-restart

1.1 High efficiency under light load and low standby power

During typical air-conditioner operation, the power requirement fluctuates according to various use cases. However, in most cases where room temperature is already stabilized, the indoor and outdoor air-conditioner units will reside in an idle state, in which the loading toward the auxiliary power supply is low. It is crucial that the auxiliary power supply operates as efficiently as possible, because it will be in this particular state for most of the period. Under light-load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency plays a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5BR3995BZ was primarily chosen due to its frequency reduction switching scheme. Compared with a traditional FF flyback, the CoolSET™ reduces its switching frequency from medium to light load, thereby minimizing switching losses. Therefore, an efficiency of more than 80 percent is achievable under 25 percent loading conditions and nominal input voltages.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, the CoolSET™ is a highly integrated device with both a controller and a HV MOSFET integrated into a single, space-saving DIP-7 package. This certainly helps the designer to reduce component count.

1.3 Auto-restart protection scheme to minimize interruption and enhance end-user experience

For an invertized air-conditioner unit, it would be annoying to both the end user and the manufacturer if the system were to halt and latch after protection. Accessibility of the input AC plug may also be difficult; therefore, to minimize interruption, the CoolSET™ implements auto-restart mode for all abnormal protections.

2 Reference board design

This document provides complete design details including specifications, schematics, bill of materials (BOM), PCB layout, and transformer design and construction information. Performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans and so on are also included.

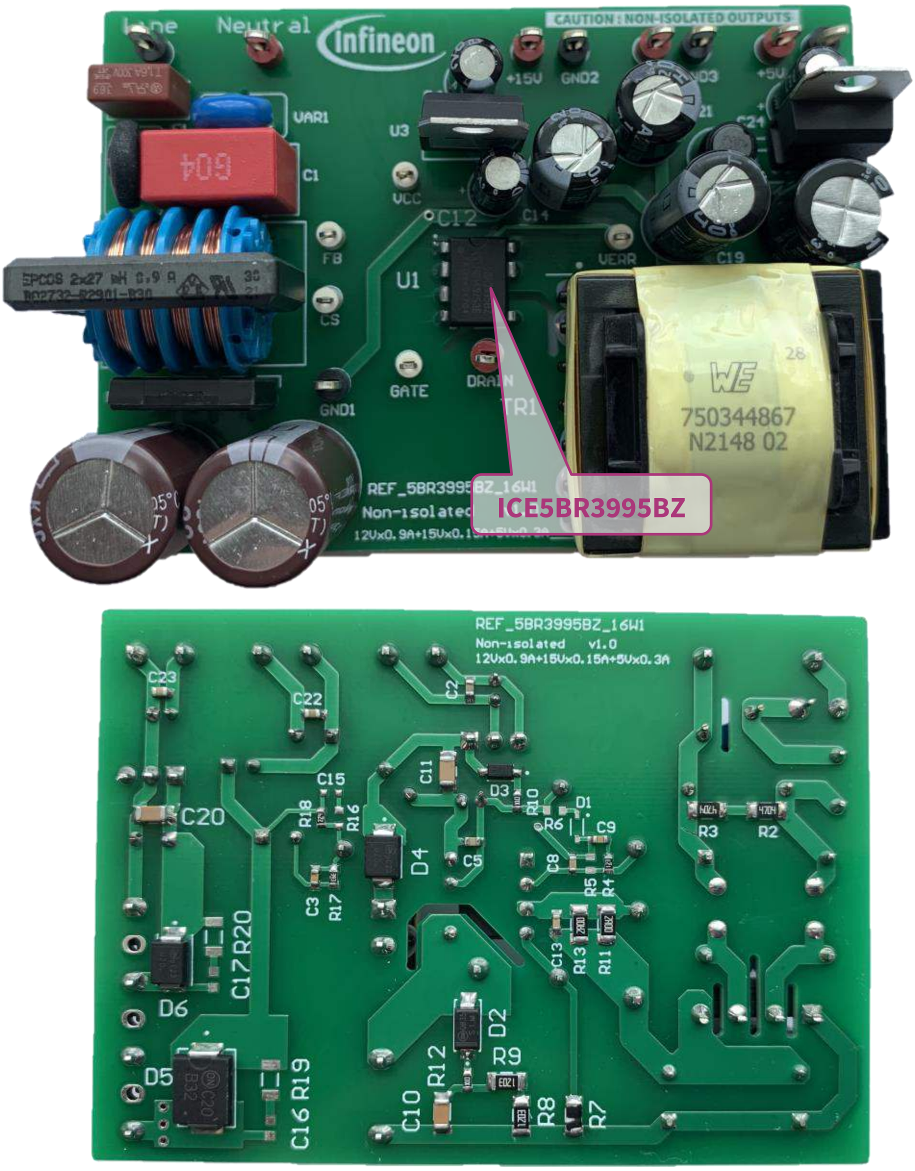


Figure 2 REF_5BR3995BZ_16W1

3 Power supply specifications

The table below shows the minimum acceptance performance of the design at 25°C ambient temperature. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5BR3995BZ_16W1

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	85	–	264	V AC	2 wires (no P.E.)
Frequency	f_{LINE}	47	50/60	64	Hz	
Output						
Output voltage 1	V_{OUT1}	–	12	–	V	±1.5 percent
Output current 1	I_{OUT1}	–	–	0.9	A	
Output voltage ripple 1	$V_{RIPPLE1}$	–	–	60	mV	
Output voltage 2	V_{OUT2}	–	15	–	V	±1 percent
Output current 2	I_{OUT2}	–	–	0.15	A	
Output voltage ripple 2	$V_{RIPPLE2}$	–	–	50	mV	
Output voltage 3	V_{OUT3}	–	5	–	V	±1 percent
Output current 3	I_{OUT3}	–	–	0.3	A	
Output voltage ripple 3	$V_{RIPPLE3}$	–	–	50	mV	
Output power	P_{OUT_Nom}	–	13.35	–	W	
Overcurrent protection (+12 V)	I_{OCP}	–	–	1.3	A	Full load on other outputs
Start-up time	t_{start_up}	–	–	250	ms	
Environmental						
Conducted EMI			10		dB	Margin, CISPR 22 class B
Surge immunity						EN 61000-4-5
Differential mode			±2		kV	
PCBA dimension			80 x 57 x 27		mm^2	L x W x H

4 Circuit diagram

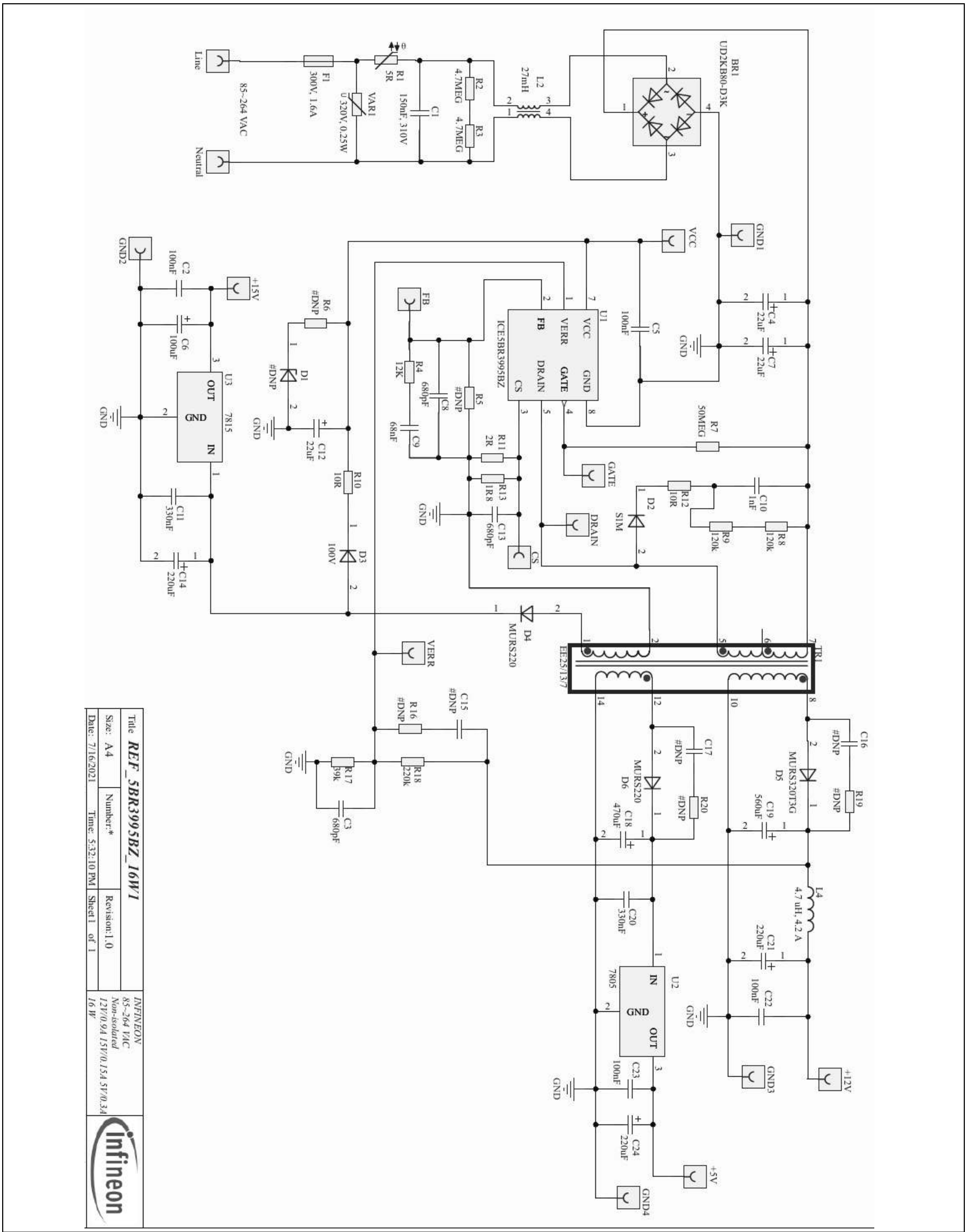


Figure 3 Schematic of REF_5BR3995BZ_16W1

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide **[2]** and calculation tool **[3]**.

5.1 EMI filtering and line rectification

The input of the power supply unit is taken from the AC power grid, which is in the range of 85 V AC ~ 264 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor VAR1, which is connected across the input to absorb excessive energy during line-surge transient. The X-capacitor C1 and common-mode choke (CMC) L2 reduce the EMI noise. R2 and R3 serve as the X-capacitor discharge resistor. Thermistor R1 is in series with line to limit inrush current. The bridge rectifier BR1 rectifies the AC input into DC voltage, filtered by the bulk capacitor C4 and C7.

5.2 Flyback converter power stage

The flyback converter power stage consists of transformer TR1, CoolSET™, secondary rectification diodes D5 and D6, secondary output capacitors C18 and C19 and output filter inductor L4.

When the primary HV MOSFET turns on, energy is stored in the transformer. When it turns off, the stored energy is discharged to the output capacitors and into the output load.

Secondary winding is sandwiched between two layers of primary winding to reduce leakage inductance. This improves efficiency and reduces voltage spikes.

For the output rectification, lower forward voltage and ultrafast recovery diodes can improve efficiency. Capacitor C19 stores the energy needed during output load jumps. LC filter L4/C21 reduces the high-frequency (HF) ripple voltage.

The +15 V output is from the 15 V low dropout (LDO) regulator (U3) with an input of +18 V. +5 V output is from the 5 V LDO regulator (U2) with an input of +8 V. As such, these outputs should not be affected by cross-regulation. However, its input should be maintained within the operating range of the LDO.

5.3 Control of flyback converter through fifth-generation FF CoolSET™ ICE5BR3995BZ

5.3.1 Current sensing

The ICE5BR3995BZ is a current mode controller. The primary peak current is controlled cycle-by-cycle through the current sense (CS) resistors R11 and R13 in the CS pin (pin 3). Transformer saturation can be avoided through peak-current limitation (PCL); therefore, the system is more protected and reliable.

5.3.2 Feedback and compensation network

Resistor R17 and R18 comprises a voltage divider, which is used to sense the V_{OUT} and directly feed back output signal to the error amplifier pin (pin 1) of U1 as the output is non-isolated. A Type II compensation network C8, C9 and R4 is connected between the FB pin (pin 2) and GND pin (pin 8) of the U1 to stabilize the system.

The FB pin of ICE5BR3995BZ is a multifunction pin, which is used to select the entry burst power level (there are three levels available) through the resistor at the FB pin (R5) and also the burst-on/burst-off sense input during ABM.

5.4 Unique features of the fifth-generation FF CoolSET™ ICE5BR3995BZ

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. Pull-up resistors R7 connected to the GATE pin (pin 4) are used to initiate the start-up phase. At first, $I_{VCC\_Charge1}$ is used to charge the V_{CC} capacitor from 0 V to V_{CC_SCP}. This is a protection which reduces the power dissipation of the power MOSFET during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of $I_{VCC\_Charge2}$ will charge the V_{CC} capacitor until the V_{CC_ON} is reached.

After start-up, the IC V_{CC} supply is usually sustained by the auxiliary winding of the transformer, which needs to support the V_{CC} to be above undervoltage lockout (UVLO) voltage (10 V typ.). In this reference board, the V_{CC} supply is tapped from the +18 V winding.

5.4.2 CCM, DCM operation with frequency reduction

ICE5BR3995BZ can be operated in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM) with frequency-reduction features. This reference board is designed to operate in DCM at operating input voltage and load conditions. When the system is operating at high output load, the controller will switch at 65 kHz FF. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented as a function of V_{FB}, as shown in **Figure 4**. Switching frequency will not reduce further once the minimum switching frequency of 28 kHz is reached.

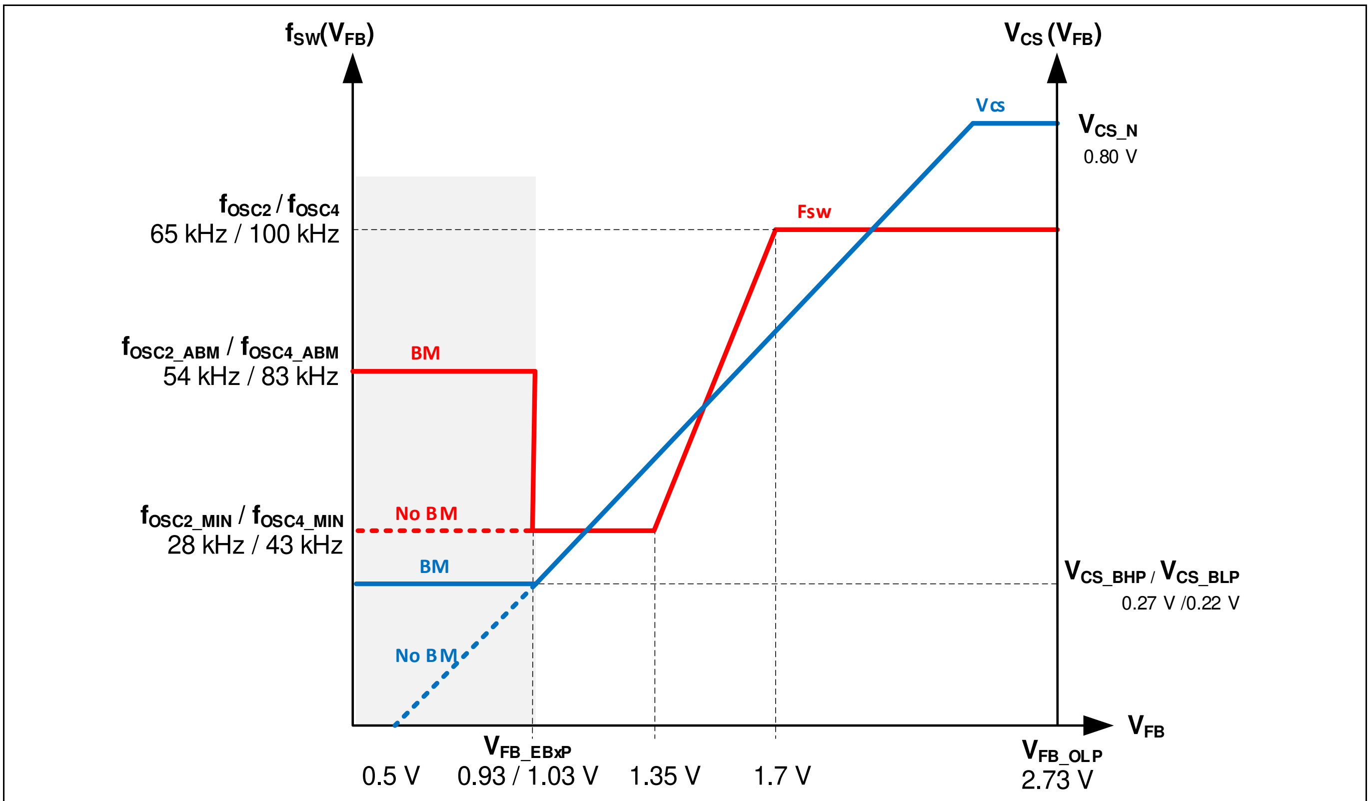


Figure 4 **Frequency reduction curve**

5.4.3 Frequency jittering with modulated gate drive

The ICE5BR3995BZ has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 65 kHz (±4 kHz), and the jitter period is 4 ms.

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5BR3995BZ provides comprehensive protection to ensure the system is operating safely. This includes V_{CC} overvoltage (OV) and undervoltage (UV), overload, overtemperature and V_{CC} short-to-GND. When those faults are found, the system will enter into protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and the failure conditions is shown in the table below.

Table 3 Protection functions of ICE5BR3995BZ

Protection function	Failure condition	Protection mode
V_{CC} OV	V_{VCC} greater than V_{VCC_OVP}	Odd-skip auto-restart
V_{CC} UV	V_{VCC} less than V_{VCCoff}	Auto-restart
Overload	V_{FB} greater than V_{FB_OLP} and lasts for $t_{FB\_OLP\_B}$	Odd-skip auto-restart
Overtemperature	T_J greater than 140°C (40°C hysteresis)	Non-switch auto-restart
V_{CC} short-to-GND (V_{VCC} = 0 V, $R_{startup}$ = 50 MΩ, V_{DRAIN} = 90 V)	V_{VCC} less than V_{CC_SCP}, $I_{VCC\_Charge1}$ ≈ -0.2 mA	Cannot start up

5.5 Clamper circuit

A clamper network consisting of D2, C10 and R8, R9, R12 is used to reduce the switching voltage spikes across the DRAIN of the integrated HV MOSFET of the CoolSET™, which are generated by the leakage inductance of the transformer TR1. This is a dissipative circuit; therefore, R8, R9 and C10 need to be fine-tuned depending on the voltage derating factor and efficiency requirement.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

- The switching power loop needs to be as small as possible (see **Figure 5**). There are three power loops in the reference design; one on the HV side and two on the output side. The HV loop starts from the bulk capacitor C7 positive terminal, primary transformer winding, CoolSET™, CS resistors and back to the C7 negative terminal. The first output side loop (+12 V output) starts at the transformer winding pin 8, output diode D5, output capacitor C19 and back to pin 10 of TR1. The second output loop (+8 V output) starts at the transformer winding (pin 12 of TR1), output diode D6, output capacitor C18 and back to pin 14 of T1. The third output loop (18 V output) starts at the transformer winding (pin 2 of TR1), output diode D4, output capacitor C14 and back to pin 1 of T1.

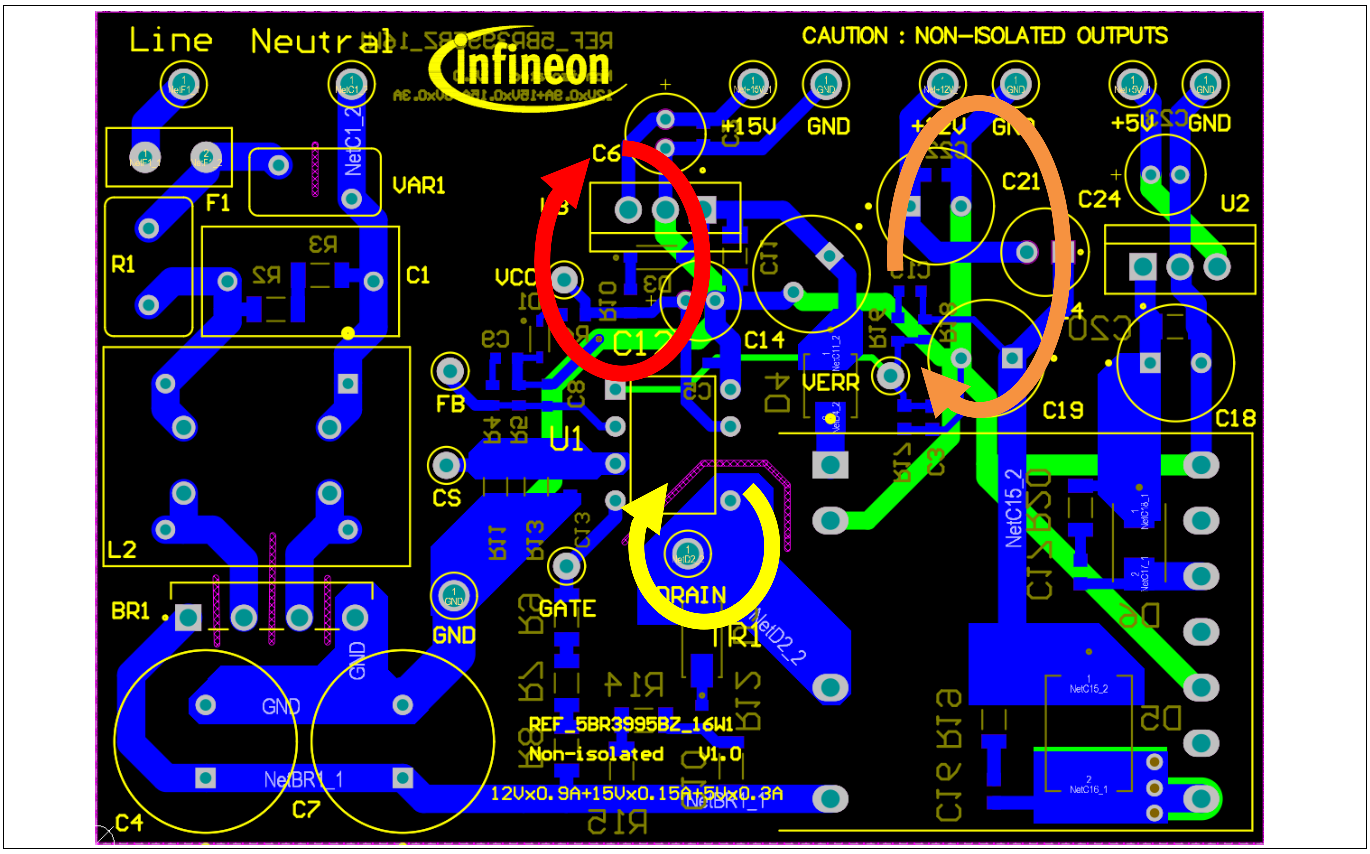


Figure 5 PCB layout tips

- Star-ground connection should be used to reduce HF noise coupling that can affect the functional operation. The ground of the small-signal components should connect directly to the IC ground.
- Separating the HV components and LV components, e.g. clamper circuit, at the top part of the PCB and the other LV components at the lower part of the PCB can reduce the spark-over chance of the high energy surge during a lightning surge test.
- Make the PCB copper pour on the DRAIN pin of the MOSFET act as a heatsink.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve a satisfactory EMI performance.

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding technique is the most common practice to reduce leakage inductance. Winding shield, core shield and whole transformer shield are also some of the techniques used to reduce EMI.
- Input CMC and X-capacitor greatly reduce EMI, but this is costly and impractical especially for low-power applications.
- Short-switching power-loop design in the PCB (as described in section 5.6) can reduce radiated EMI due to the antenna effect.
- An output diode snubber circuit can reduce HF noise.
- Ferrite beads can reduce HF noise, especially on critical nodes such as the DRAIN pin, clamper diode and output diode terminals. There is no ferrite bead used in this design, as this can reduce the efficiency due to additional losses especially on high-current terminals.

6 PCB layout

6.1 Top side

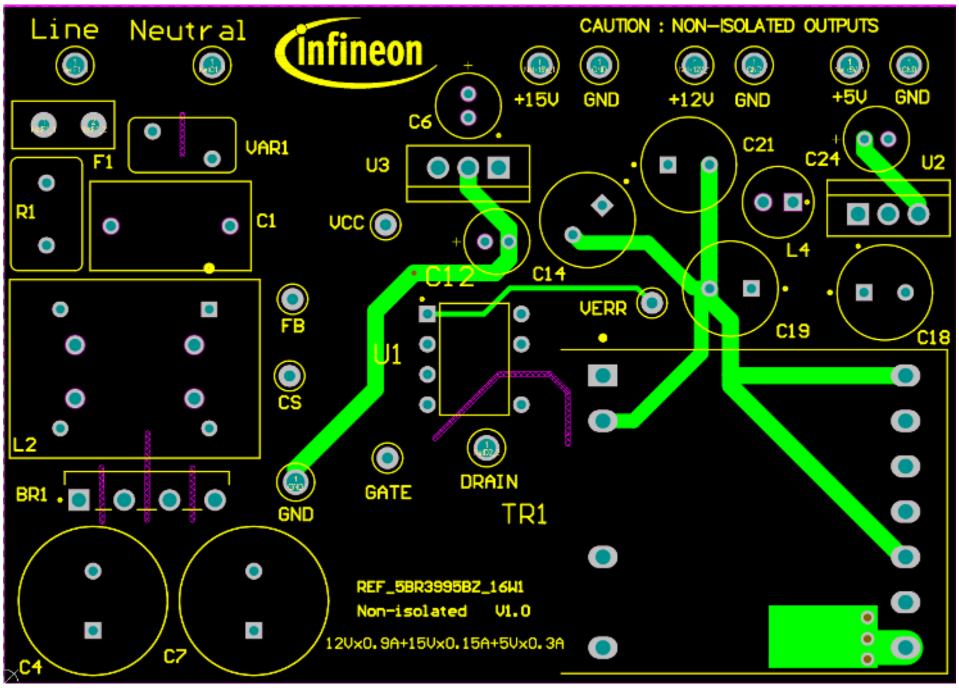


Figure 6 Top-side component legend

6.2 Bottom side

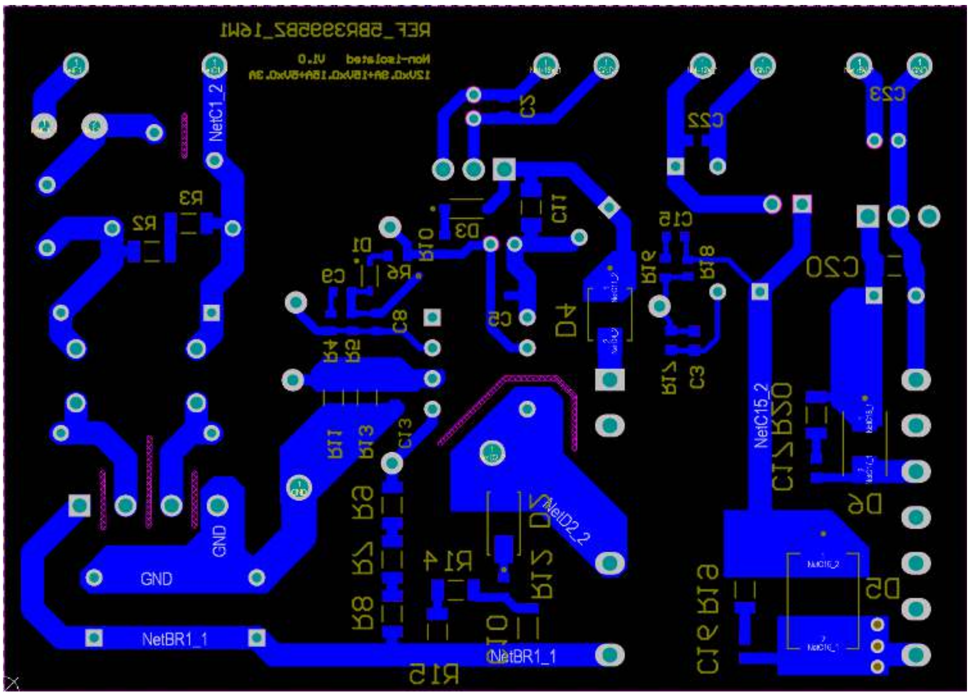


Figure 7 Bottom-side component legend

7 Bill of materials

Table 4 BOM

No.	Designator	Description	Part number	Manufacturer	Quantity
1	BR1	Bridge rectifiers 2 A 800 V	UD2KB80-7000	Shindengen	1
2	C1	Film capacitors, 150 nF, 310 V AC	890334023025	Würth Elektronik	1
3	C2, C5, C22, C23	MLCC – SMD/SMT 50 V 0.1 µF X7R 0603 10%			4
4	C4, C7	Aluminum capacitor 22 µF 20% 400 V radial	EKXG401ELL220MK20S	United Chemi-Con	2
5	C6, C24	Aluminum capacitor 100 µF 20% 25 V radial	25PX100MEFC5X11	Rubycon	2
6	C8	MLCC – SMD/SMT 0603 50 V 2200 pF 10%			1
7	C10	MLCC – SMD/SMT 500 V 1000 pF X7R 1206 10%			1
8	C9	MLCC – SMD/SMT 0603 50 V 68 nF 10%			1
9	C3, C13	MLCC – SMD/SMT 0603 50 V 680 pF 10%			2
10	C11, C20	MLCC – SMD/SMT 1206 50V 330nF 10%			2
11	C12	Aluminum capacitor 22 µF 20% 35V radial	UVR1V220MDD	Nichicon	1
12	C14, C21	Aluminum capacitor 220 µF 20% 35V radial	35ZLH220MEFCT78X11.5	Rubycon	2
13	C18	Aluminum capacitor 470 µF 20% 16V radial	UHE1C471MPD	Nichicon	1
14	C19	Aluminum capacitor 560 µF 20% 25V radial	25ZLJ560M8X20	Rubycon	1
15	D2	General-purpose diode 1 kV 1 A SMA	S1M		1
16	D3	General-purpose diode 100 V 150 mA SOD-123	BAV16W-7-F	Diodes Inc.	1
17	D4, D6	General-purpose diode 200 V 2 A SMB	MURS220T3G	ON Semiconductor	2
18	D5	General-purpose diode 200 V 3 A SMC	MURS320T3G	ON Semiconductor	1
19	F1	Time-lag fuse, 300 V, 1.6 A	36911600000	Littelfuse	1
20	L2	CMC 27 mH 700 mA 2LN TH	B82731M2701A030	TDK	1
21	L4	Inductor WE-TI, size 5075, 4.7 µH, 4.2 A	7447462047	Würth Elektronik	1
22	R1	ICL 5 Ω 20% 4.2 A 9.5 mm	B57235S0509M000	TDK Corporation	1
23	R2, R3	SMD resistor 4.7 mΩ 1% 1/4 W 1206			2
24	R4	SMD resistor 12 kΩ 1% 1/10 W 0603			1
25	R7	SMD resistor 50 mΩ 1% 300 mW 1206	CRHA1206AF50M0FKEF	Vishay	1
26	R8, R9	SMD resistor 120 kΩ 1% 1/4 W 1206			2
27	R10, R12	SMD resistor 10 Ω 1% 1/10 W 0603			2
28	R11, R13	SMD resistor 2.0 Ω 1% 1/4 W 1206			2
29	R17	Resistor 39 kΩ 1% 1/10 W 0603			1
30	R18	Resistor 220 kΩ 1% 1/10 W 0603			1
31	TR1	EE25/13/7	750344867	Würth Elektronik	1
32	U1	FF 950 V CoolSET™	ICE5BR3995BZ	Infineon	1
33	U2	IC linear regulator 5 V 1.5 A TO-220AB	L7805ABV	STMicroelectronics	1
34	U3	IC linear regulator 15 V 1.5 A TO-220AB	L7815ABV	STMicroelectronics	1
35	VAR1	S07K320E2 320 V AC 10%	B72207S2321K101	Epcos	1
36	+5 V, +12 V, +15 V, DRAIN, neutral	Test point THT, red	5010	Keystone	5
37	CS, FB, GATE, VERR, V_{CC}	Test point THT, white	5002	Keystone	5
38	GND1, GND2, GND3, GND4, line	Test point THT, black	5011	Keystone	5

8 Transformer specification

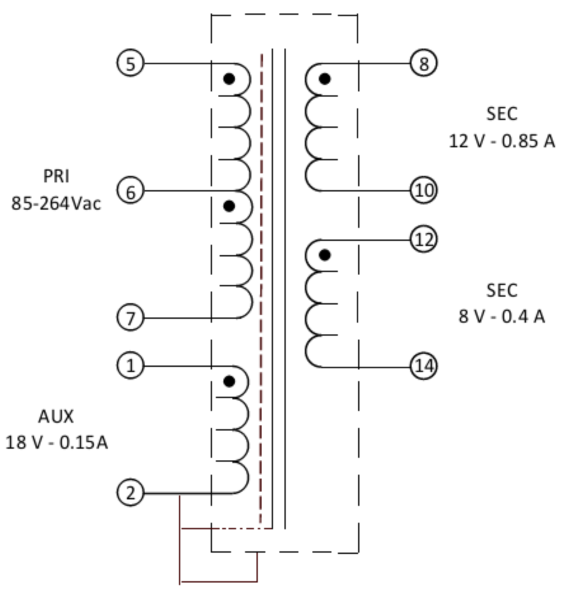
Refer to Appendix A for transformer design and Appendix B for WE transformer specification.

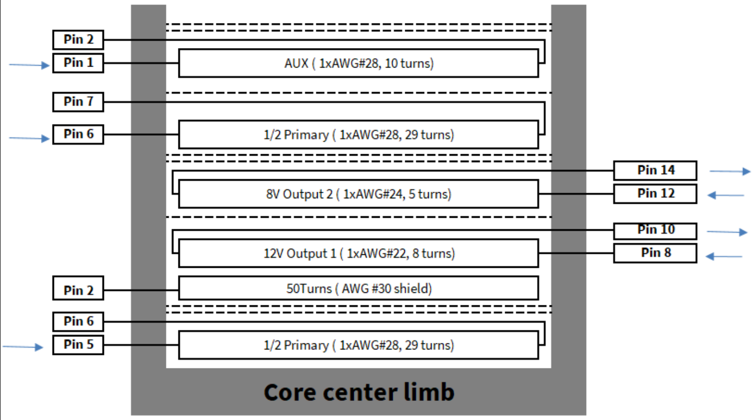
Core name and material: EE25/13/7, TP4A (TDG)

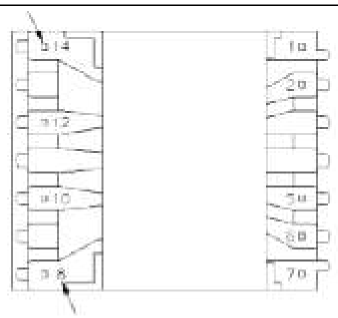
Würth Elektronik bobbin: 070-6725 (14-pin, THT, horizontal version)

Primary inductance: L_P = 820 µH (±10 percent), measured between pin 5 and pin 7

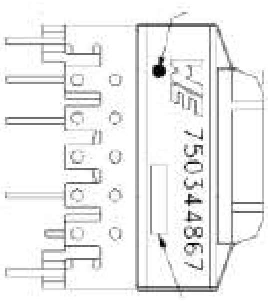
Manufacturer and part number: Würth Elektronik Midcom (750344867) Rev.01







Bottom view



Side view

Wire size requirement :

Start	Stop	No. of turns	Wire size	Layer
5	6	29	1 x AWG#28	1/2 Primary
2		50	1 x AWG#30	SHIELD
8	10	8	1 x AWG#22	O/P_1 Secondary
12	14	6	1 x AWG#24	O/P_2 Secondary
6	7	29	1 x AWG#28	1/2 Primary
1	2	12	1 x AWG#28	AUX

Horizontal and vertical external shields are added and tied topin 2

Figure 8 Transformer structure

9 Measurement data and graphs

Table 5 Electrical measurements

Input (V AC/Hz)	P_{IN} (W)	V_{O1} (V)	I_{O1} (A)	V_{O2} (V)	I_{O2} (A)	V_{O3} (V)	I_{O3} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)	OLP P_{IN} (W)	OLP I_{O1} (A)
85 V AC/ 60 Hz	0.80	11.968	0.040	15.230	0.005	4.99	0.005	0.580			21.37	1.02
	4.95	11.984	0.224	15.212	0.040	4.98	0.075	3.667	74.07	74.39		
	9.66	11.968	0.444	15.195	0.080	4.97	0.148	7.265	75.21			
	14.82	11.968	0.680	15.187	0.119	4.96	0.223	11.052	74.58			
	19.61	11.968	0.895	15.185	0.149	4.96	0.298	14.452	73.70			
115 V AC/ 60 Hz	0.81	11.968	0.040	15.250	0.005	4.99	0.005	0.580			20.92	1.02
	4.92	11.968	0.224	15.215	0.040	4.98	0.075	3.663	74.46	75.42		
	9.55	11.968	0.444	15.205	0.080	4.97	0.148	7.266	76.08			
	14.56	11.953	0.680	15.205	0.119	4.96	0.223	11.044	75.85			
	19.18	11.953	0.895	15.215	0.149	4.96	0.298	14.443	75.30			
230 V AC/ 50 Hz	0.83	11.968	0.040	15.207	0.005	4.99	0.005	0.580			20.53	1.07
	5.00	11.968	0.224	15.192	0.040	4.98	0.075	3.662	73.25	75.53		
	9.56	11.968	0.444	15.187	0.080	4.97	0.148	7.264	75.99			
	14.51	11.968	0.680	15.177	0.119	4.96	0.223	11.051	76.16			
	18.82	11.953	0.895	15.212	0.149	4.96	0.298	14.443	76.74			
264 V AC/ 50 Hz	0.85	11.968	0.040	15.215	0.005	4.99	0.005	0.580			20.77	1.10
	5.05	11.968	0.224	15.192	0.040	4.98	0.075	3.662	72.52	75.01		
	9.70	11.968	0.444	15.187	0.080	4.97	0.148	7.264	74.89			
	14.53	11.953	0.680	15.177	0.119	4.96	0.223	11.041	75.99			
	18.85	11.953	0.895	15.232	0.149	4.96	0.298	14.446	76.63			

Minimum load condition: 12 V/40 mA, 5 V/5 mA, 15 V/5 mA
25 percent load condition: 12 V/0.23 A, 5 V/0.08 A, 15 V/0.04 A
50 percent load condition: 12 V/0.45 A, 5 V/0.15 A, 15 V/0.08 A
75 percent load condition: 12 V/0.68 A, 5 V/0.23 A, 15 V/0.12 A
100 percent load condition: 12 V/0.9 A, 5 V/0.3 A, 15 V/0.15 A

Table 6 Efficiency and standby performance with single-output configuration (modified from original board for illustration purposes only)

Input (V AC/Hz)	P_{IN} (W)	V_{O1} (V)	I_{O1} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
85 V AC/60 Hz	0.011	11.984	0.000	0.000		
	1.368	11.875	0.093	1.104	80.73	
	3.070	11.875	0.216	2.565	83.55	82.89
	6.054	11.859	0.425	5.040	83.25	
	9.048	11.859	0.634	7.519	83.10	
	12.288	11.859	0.846	10.033	81.65	
115 V AC/60 Hz	0.014	11.984	0.000	0.000		
	1.368	11.875	0.093	1.104	80.73	
	3.053	11.875	0.216	2.565	84.02	83.70
	6.010	11.859	0.425	5.040	83.86	
	8.985	11.859	0.634	7.519	83.68	
	12.050	11.859	0.846	10.033	83.26	
230 V AC/50 Hz	0.021	11.984	0.000	0.000		
	1.463	11.875	0.093	1.104	75.49	
	3.124	11.875	0.216	2.565	82.11	83.46
	6.020	11.859	0.425	5.040	83.72	
	8.944	11.859	0.634	7.519	84.06	
	11.953	11.859	0.846	10.033	83.93	
264 V AC/50 Hz	0.029	11.984	0.000	0.000		
	1.501	11.875	0.093	1.104	73.58	
	3.164	11.875	0.216	2.565	81.07	82.85
	6.058	11.859	0.425	5.040	83.20	
	9.010	11.859	0.634	7.519	83.45	
	11.990	11.859	0.846	10.033	83.68	

Note: Single-output (+12 V) configuration efficiency measurement was done by removing two LDO output circuits, and connecting +12 V output directly to the V_{CC} circuit; the actual board comes with LDO circuits. The overall circuit is not optimized for single-output configuration; the above efficiency data is for illustration only.

9.1 Efficiency curve

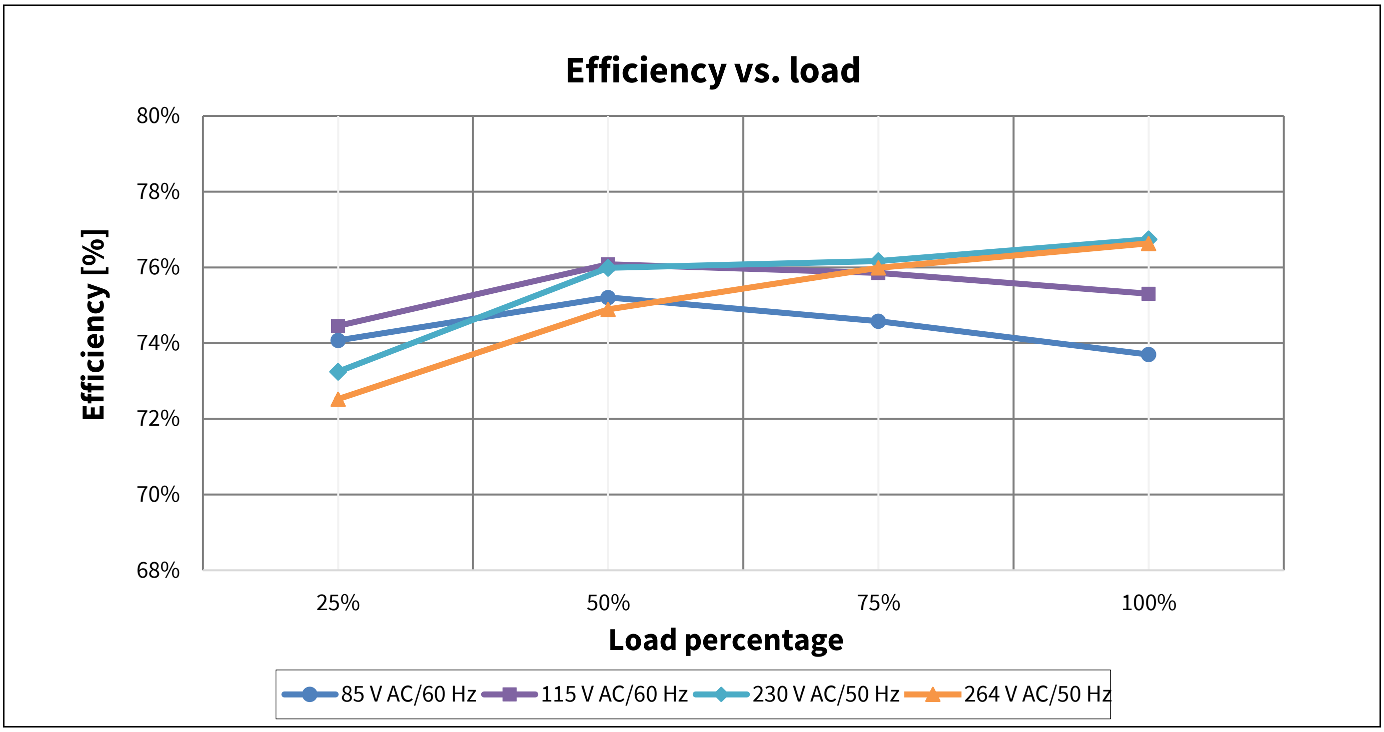


Figure 9 Efficiency vs. output load

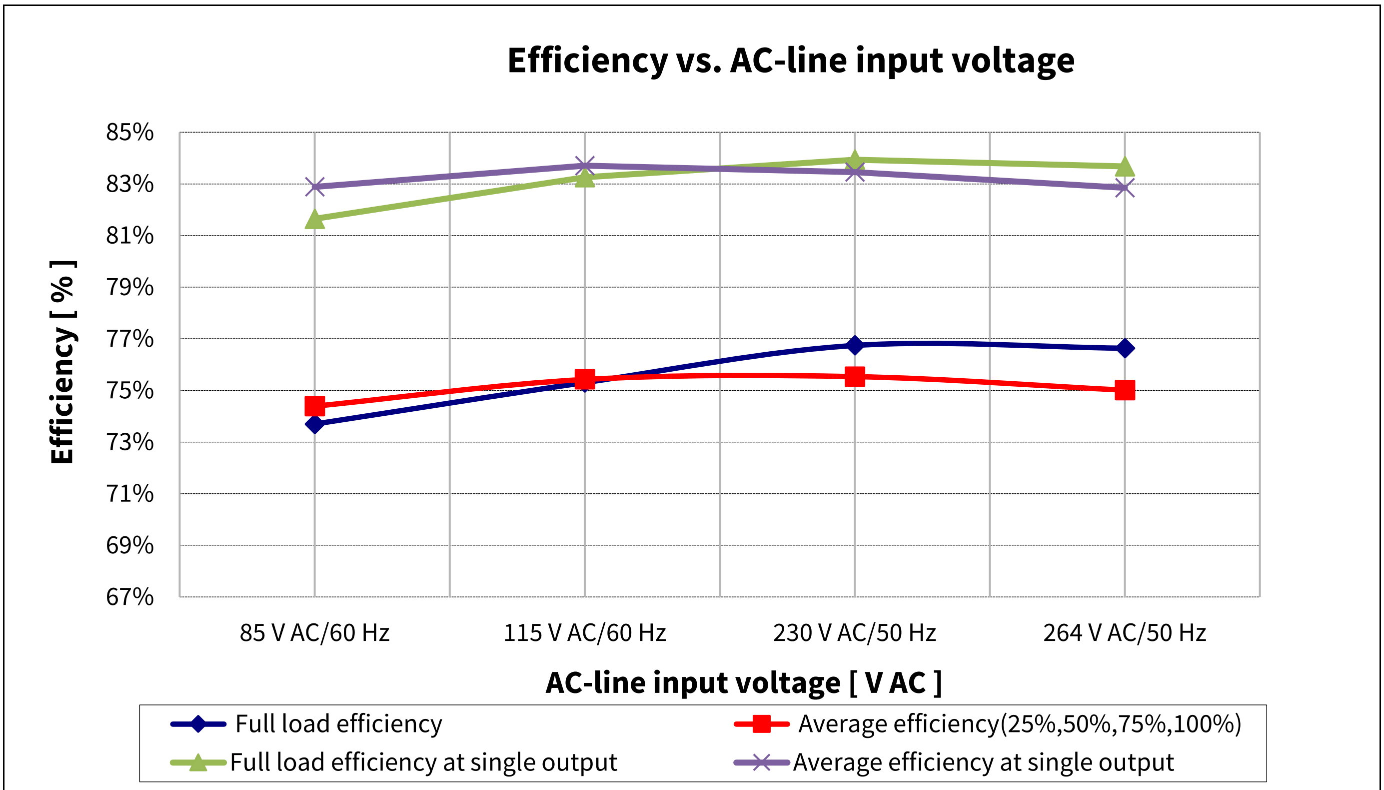


Figure 10 Efficiency vs. AC-line input voltage

9.2 Standby power

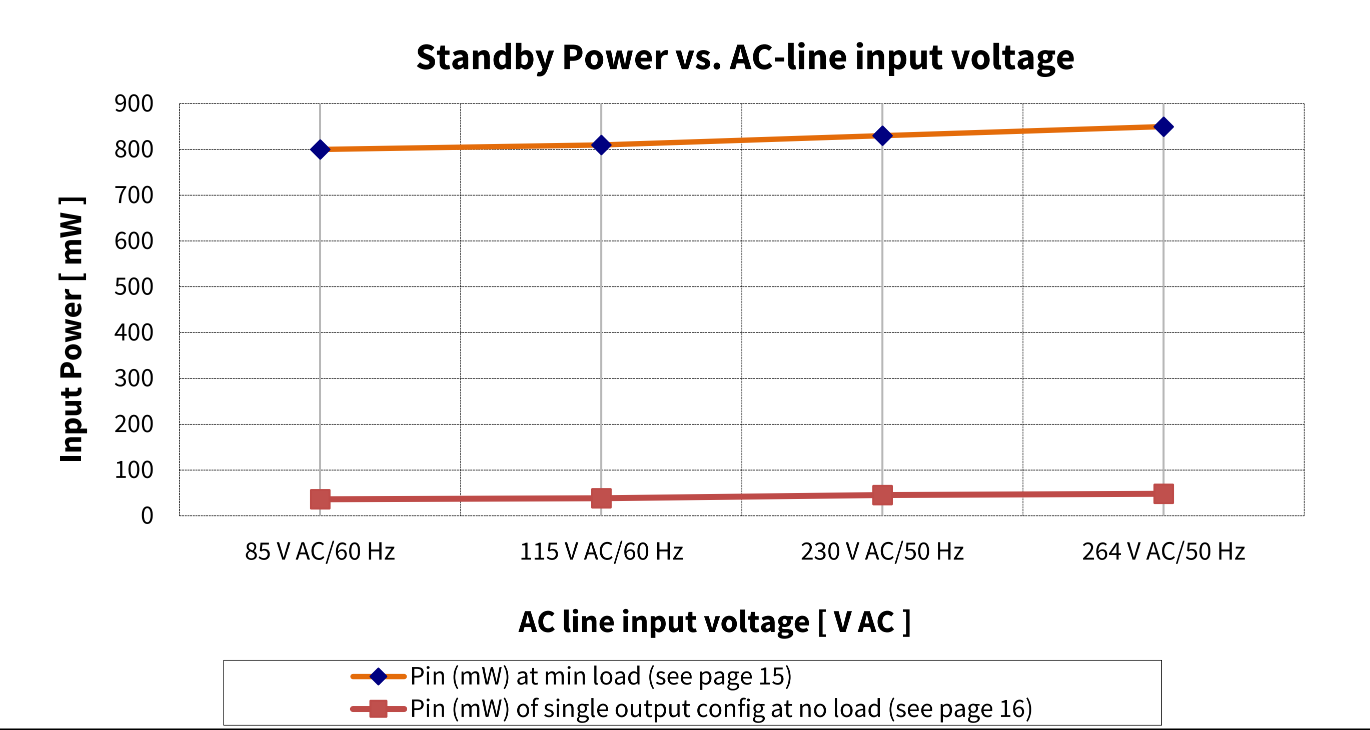


Figure 11 Standby power at minimum load vs. AC-line input voltage

9.3 Line and load regulation

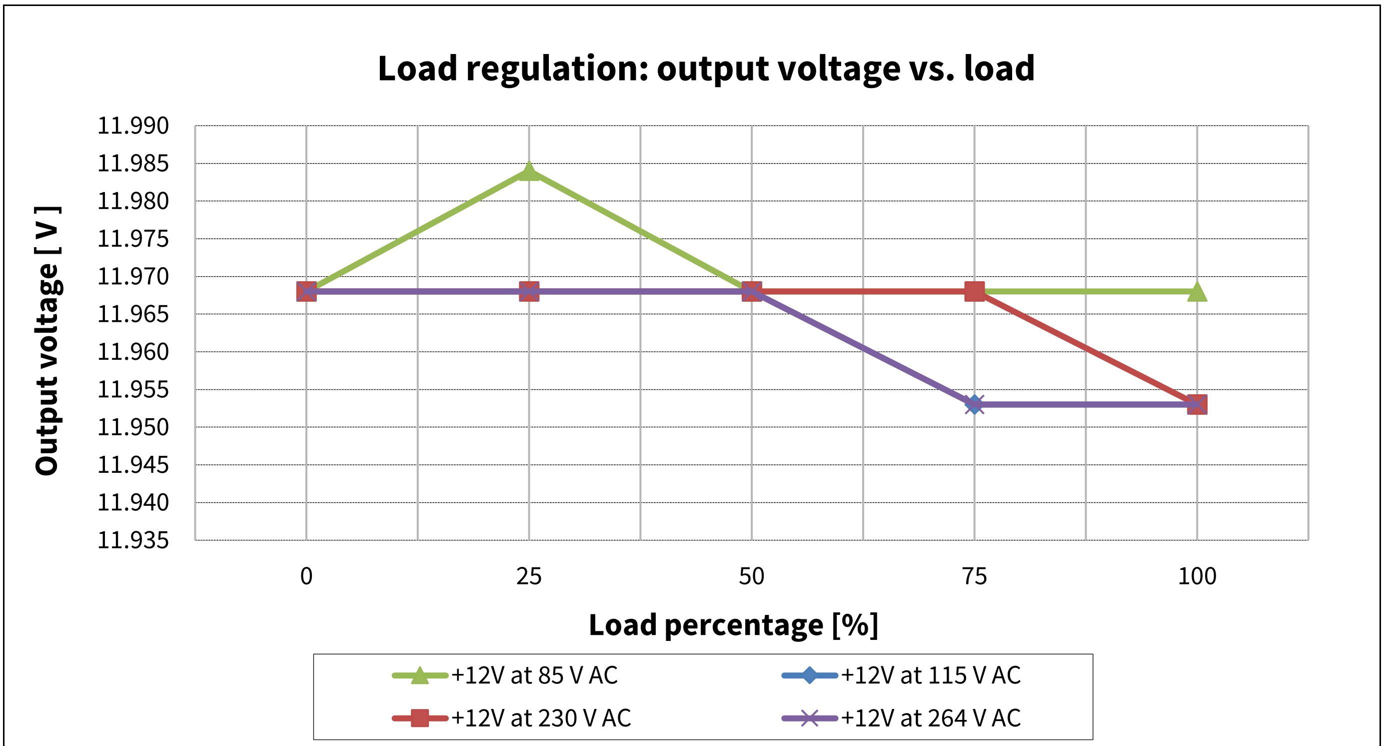


Figure 12 Output regulation vs. load at different AC-line input voltages

9.4 Maximum input power

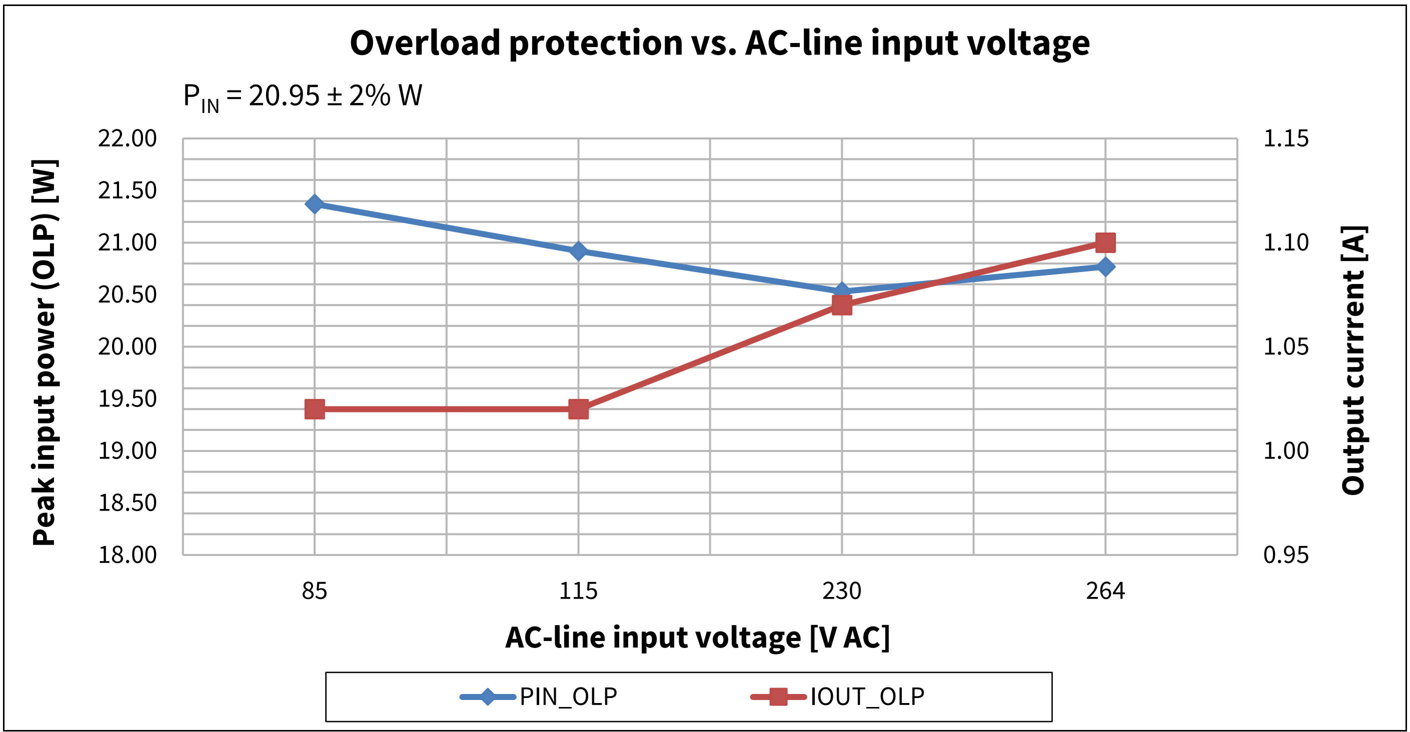


Figure 13 **Maximum input power and output current (before overload protection) vs. AC-line input voltage**

9.5 Surge immunity (EN 61000-4-5)

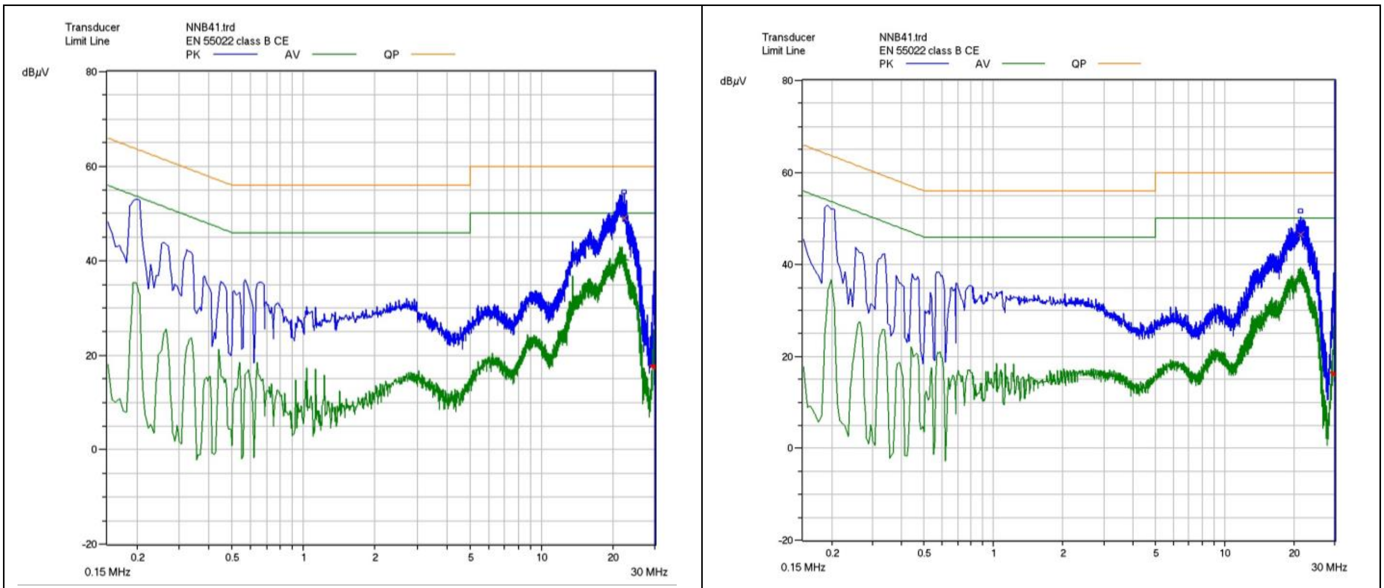
The reference board was subjected to a surge immunity test (±2 kV DM) according to EN 61000-4-5. It was tested at full load (resistive load). A test failure was defined as non-recoverable.

Table 7 **System surge immunity test result**

Description	Test	Level	Number of strikes				Test result
			0°	90°	180°	270°	
115/230 V AC	DM	±2 kV	3	3	3	3	Pass

9.6 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board was tested at full load (resistive load) at input voltage of 115 V AC and 230 V AC. It passed with more than 10 dB margin.



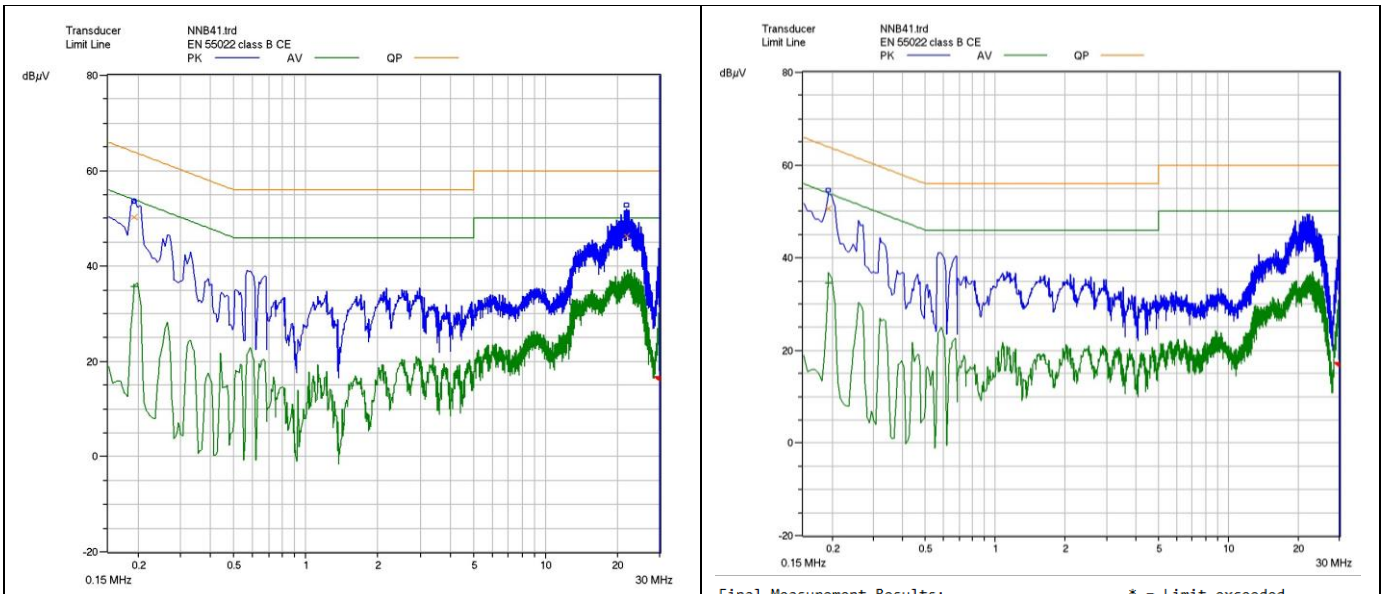
Final Measurement Results: * = Limit exceeded (line, left)

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Notes
22.1680	L	54.7	L	40.3	L	49.2	50.0	60.0	

Final Measurement Results: * = Limit exceeded (neutral, right)

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Notes
21.4400	L	51.7	L	38.2	L	46.6	50.0	60.0	

Figure 14 Conducted emissions at 115 V AC and full load on line (left) and neutral (right)



Final Measurement Results: * = Limit exceeded (line, left)

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Notes
0.1920	L	53.6	L	35.7	L	50.4	53.9	63.9	
21.8880	L	52.9	L	37.2	L	46.4	50.0	60.0	

Final Measurement Results: * = Limit exceeded (neutral, right)

Frequency		Level Pk		Level AV		Level QP	Limit AV	Limit QP	Notes
0.1920	L	54.6	L	34.6	L	50.7	53.9	63.9	

Figure 15 Conducted emissions at 220 V AC and full load on line (left) and neutral (right)

9.7 Thermal measurement (pending)

Thermal measurement was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C taken after one hour running at full load. The temperature of the components was taken in an open-frame set-up.

Table 8 Thermal measurement of components (open-frame)

No.	Component	Temperature at 85 V AC (°C)	Temperature at 264 V AC (°C)
1	BR1	53.9	40.7
2	U1	76.2	71.5
3	TR1	54.6	58.5
4	D5	87.4	89.3
5	D6	76.4	77.2
6	D4	65.3	63.8

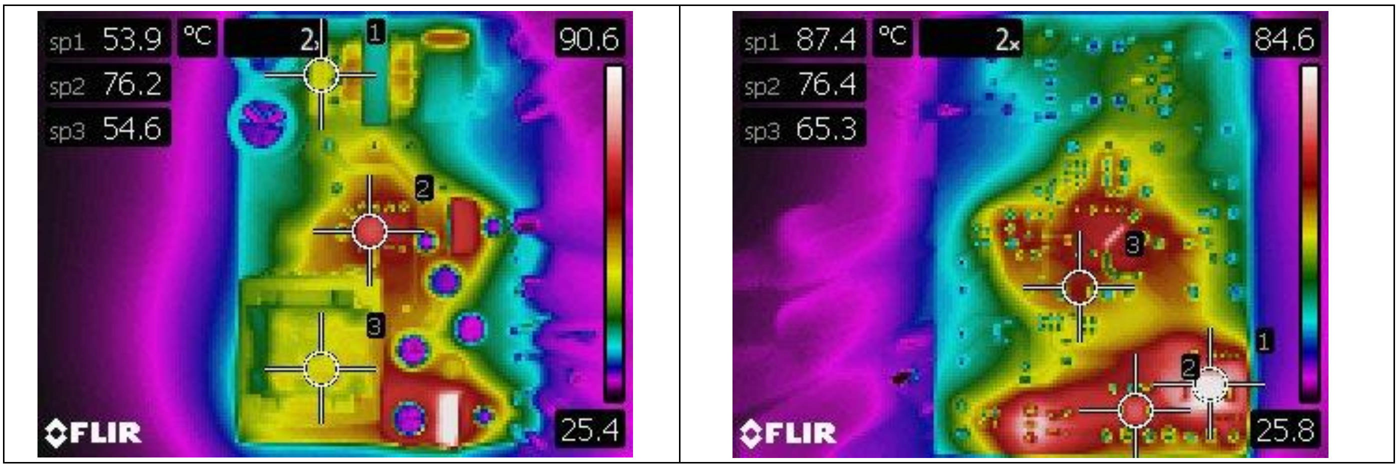


Figure 16 Top-layer (left) and bottom-layer (right) thermal image at 85 V AC input voltage

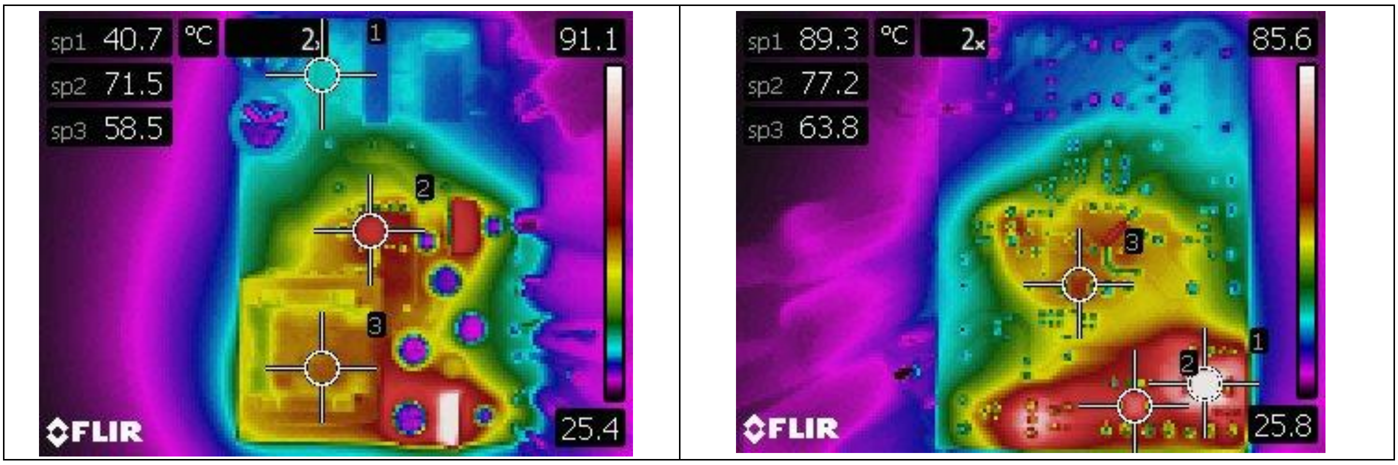


Figure 17 Top-layer (left) and bottom-layer (right) thermal image at 264 V AC input voltage

9.8 +18 V rail regulation (LDO input)

As the +15 V output via LDO is derived from the +18 V rail from the transformer which is also shared by the CoolSET™ V_{CC}, there are several design goals to achieve during normal operating conditions:

- Avoid V_{CC} UVLO (10 V typ.)
- Avoid V_{CC} OVP (25.5 V typ.)
- Meet the specification of the LDO: (V_{OUT} + 1~2 V) less than or equal to V_{IN} less than or equal to 30 V; load dependent.

From the chart and table below, the +18 V rail is operating between 18.51 V and 22.26 V under different load combinations and line conditions, which is well within the design objectives outlined above.

Table 9 +18 V rail line and load regulation

Conditions	12 V/40 mA 5 V/0 A 15 V/0 A (V)	12 V/40 mA 5 V/5 mA 15 V/5 mA (V)	12 V/0.9 A 5 V/5 mA 15 V/5 mA (V)	12 V/0.9 A 5 V/0.3 A 15 V/0.15 A (V)
85 V AC/60 Hz	18.66	18.51	22.26	18.65
115 V AC/60 Hz	18.67	18.52	22.26	18.67
230 V AC/50 Hz	18.67	18.52	22.04	18.64
264 V AC/50 Hz	18.67	18.51	22.01	18.64

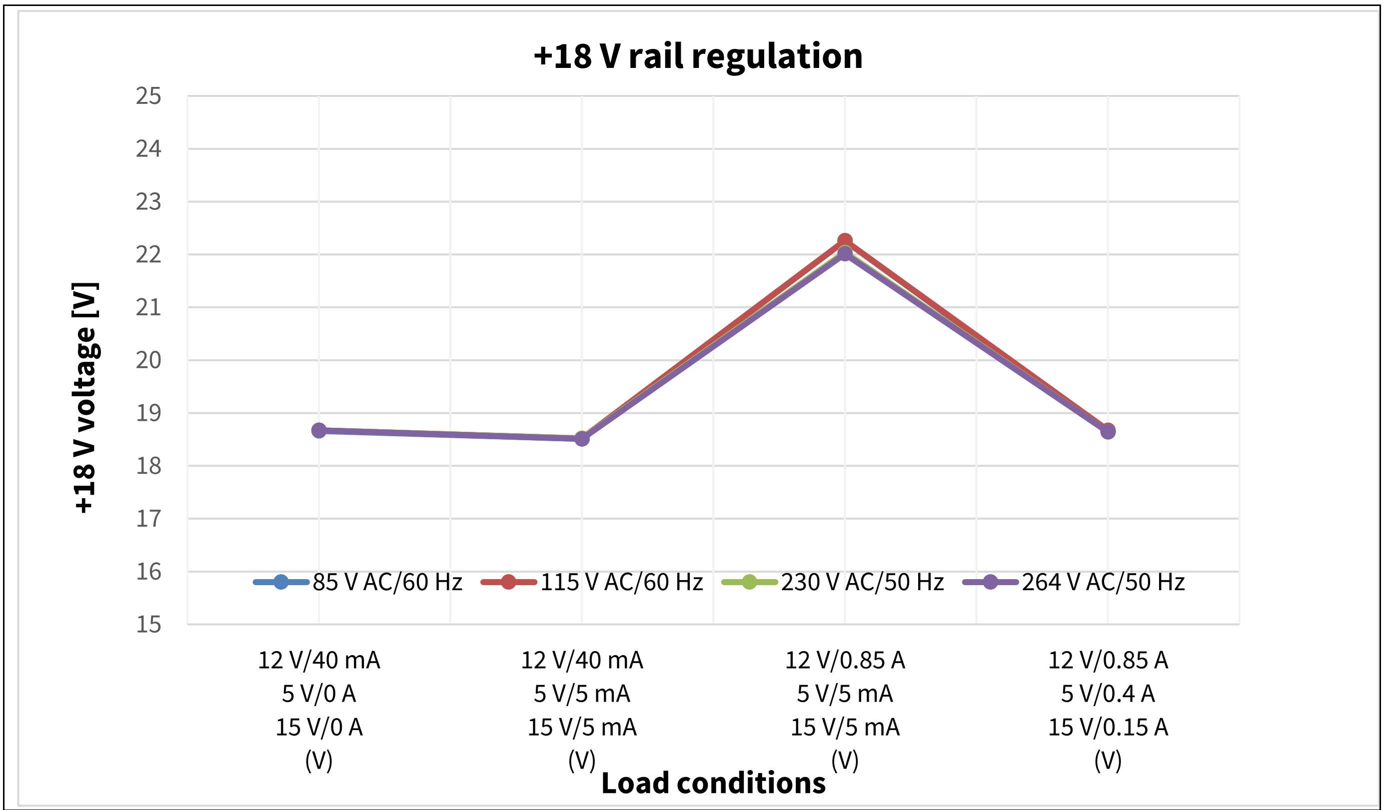


Figure 18 +18 V rail regulation

10 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy 606Zi oscilloscope.

10.1 Start-up at full load

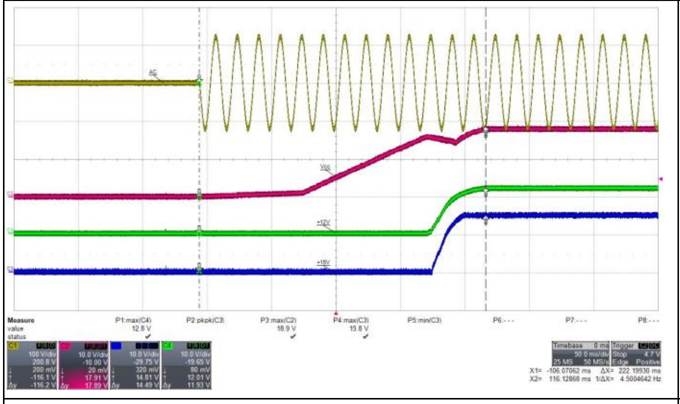
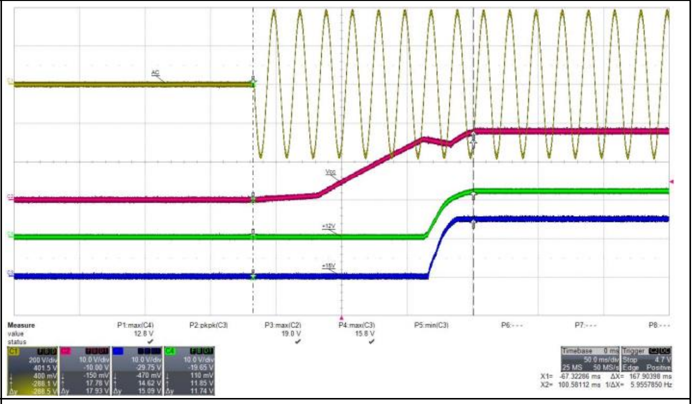
	
C1 (yellow) : AC-line voltage C2 (purple) : V_{CC} voltage C3 (blue) : +15 V output voltage C4 (green) : +12 V output voltage	C1 (yellow) : AC-line voltage C2 (purple) : V_{CC} voltage C3 (blue) : +15 V output voltage C4 (green) : +12 V output voltage
85 V AC start-up time at full load is around 222 ms	264 V AC start-up time at full load is around 167 ms

Figure 19 Start-up

10.2 Soft-start at full load

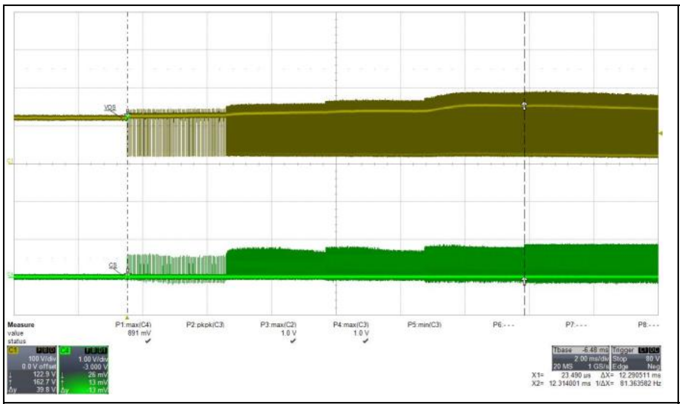
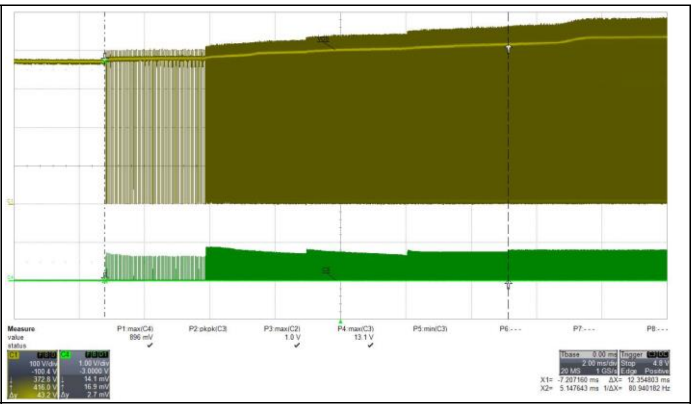
	
C1 (yellow) : Drain voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C4 (green) : CS voltage
85 V AC soft-start at full load within ~12 ms	264 V AC soft-start time at full load within ~12 ms

Figure 20 Soft-start

10.3 Drain and CS voltage at full load

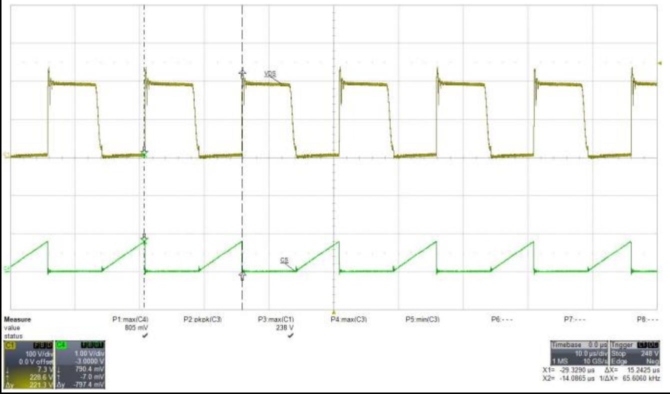
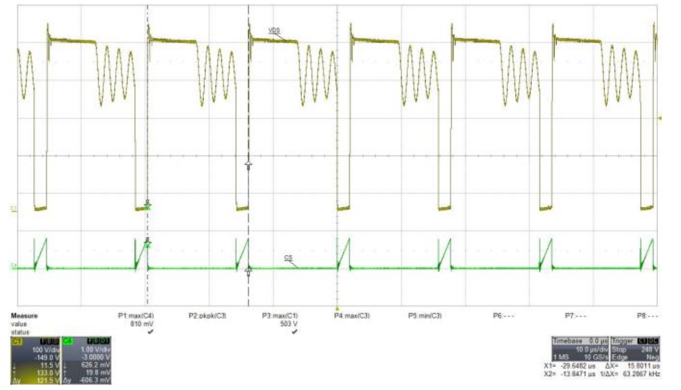
	
C1 (yellow) : Drain voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C4 (green) : CS voltage
85 V AC maximum drain voltage at full load is ~238 V	264 V AC maximum drain voltage at full load is ~503 V

Figure 21 Drain and CS voltage

10.4 Frequency jittering

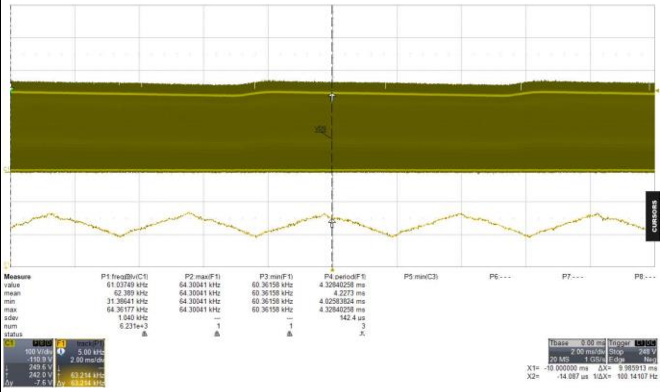
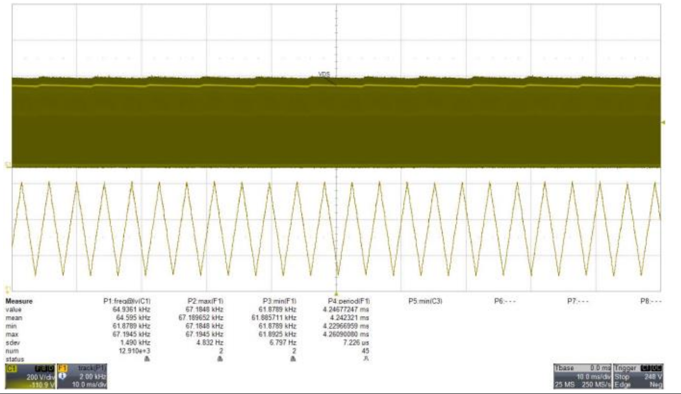
	
C1 (yellow) : Drain voltage F1 (yellow) : Frequency track of drain voltage	C1 (yellow) : Drain voltage F1 (yellow) : Frequency track of drain voltage
85 V AC frequency jittering at full load is ~60 kHz to ~64 kHz with jitter period of 4 ms	85 V AC frequency jittering at full load is ~62 kHz to ~67 kHz with jitter period of 4 ms

Figure 22 Frequency jittering

10.5 Load-transient response

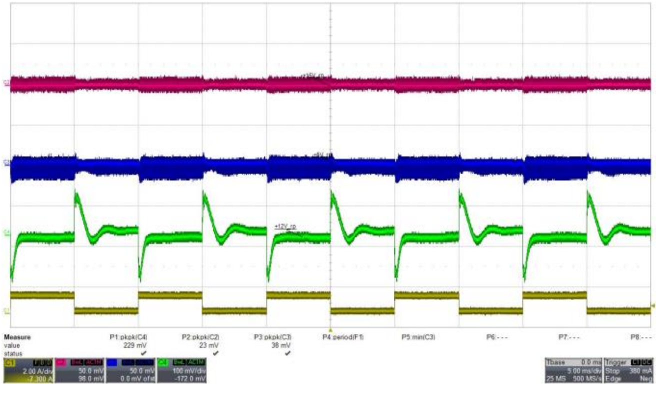
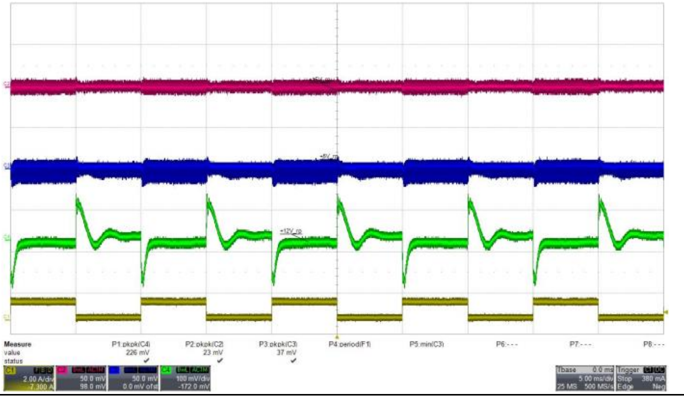
	
C1(yellow) : Output current at +12 V C2 (purple) : +15 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +12 V output voltage	C1(yellow) : Output current at +12 V C2 (purple) : +15 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +12 V output voltage
Input 85 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 229 mV $V_{ripple\_pk\_pk}$ for +5 V output voltage: 38 mV $V_{ripple\_pk\_pk}$ for +15 V output voltage: 23 mV	Input 264 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 226 mV $V_{ripple\_pk\_pk}$ for +5 V output voltage: 37 mV $V_{ripple\_pk\_pk}$ for +15 V output voltage: 23 mV

Figure 23 Load-transient response (+12 V output load change from 10 percent to 100 percent at 0.4 A/µs slew rate, 100 Hz, +15 V output and +5 V output load are fixed at full load; 20 MHz bandwidth and 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor)

10.6 Output ripple voltage at full load

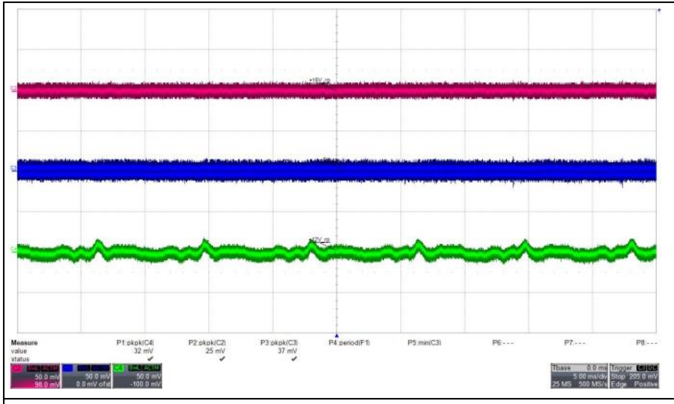
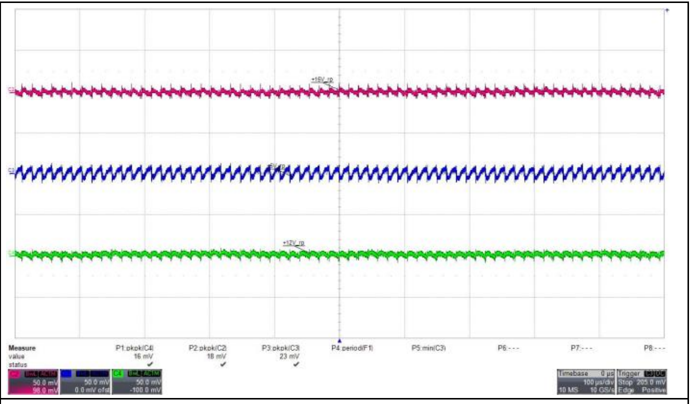
	
C2 (purple) : +15 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +12 V output voltage	C2 (purple) : +15 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +12 V output voltage
Input 85 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 32 mV $V_{ripple\_pk\_pk}$ for +5 V output voltage: 37 mV $V_{ripple\_pk\_pk}$ for +15 V output voltage: 25 mV	Input 264 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 16 mV $V_{ripple\_pk\_pk}$ for +5 V output voltage: 23 mV $V_{ripple\_pk\_pk}$ for +15 V output voltage: 18 mV

Figure 24 Output ripple voltage at full load. Probe terminals are decoupled with 10 µF electrolytic and 0.1 µF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz

10.7 Output ripple voltage at ABM (minimum load)

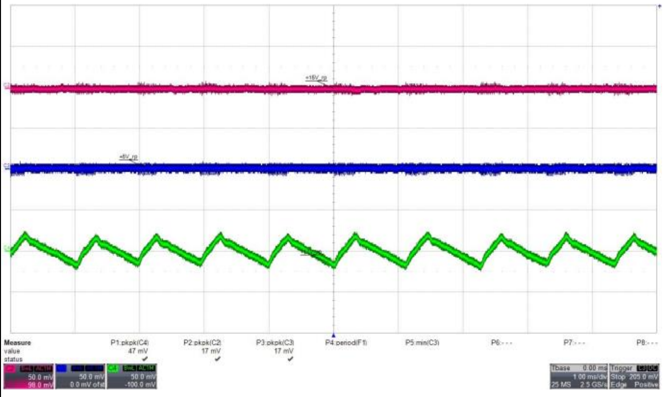
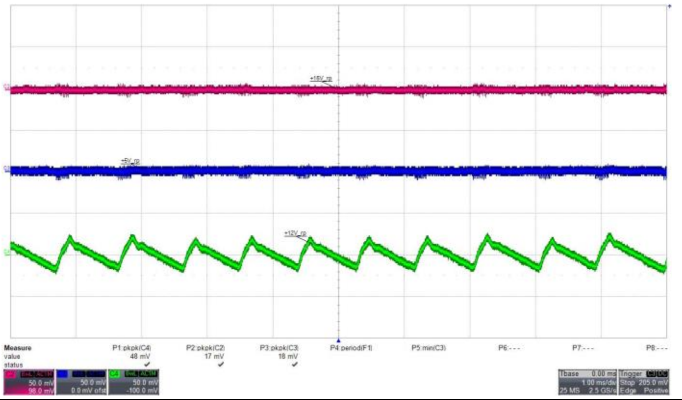
	
C2 (purple) : +15 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +12 V output voltage	C2 (purple) : +15 V output voltage C3 (blue) : +5 V output voltage C4 (green) : +12 V output voltage
Input 85 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 47 mV $V_{ripple\_pk\_pk}$ for +5 V output voltage: 17 mV $V_{ripple\_pk\_pk}$ for +15 V output voltage: 17 mV	Input 264 V AC $V_{ripple\_pk\_pk}$ for +12 V output voltage: 48 mV $V_{ripple\_pk\_pk}$ for +5 V output voltage: 18 mV $V_{ripple\_pk\_pk}$ for +15 V output voltage: 17 mV

Figure 25 Output ripple voltage at minimum load. Probe terminals are decoupled with 10 μF electrolytic and 0.1 μF ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz

10.8 Entering ABM

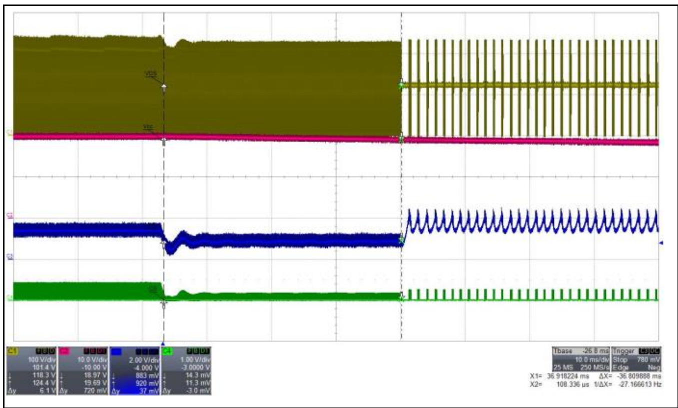
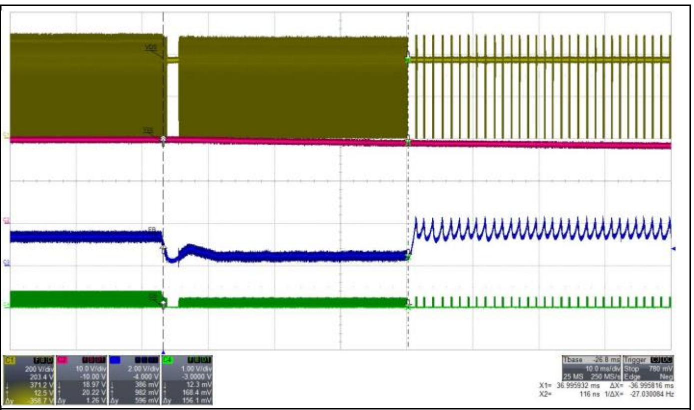
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC enters ABM at FB pin voltage less than 1.03 V (V_{FB_EBLP}) for more than 36 ms (t_{FB_BEB})	264 V AC enters ABM at FB pin voltage less than 1.03 V (V_{FB_EBLP}) for more than 36 ms (t_{FB_BEB})

Figure 26 Entering ABM

10.9 During ABM

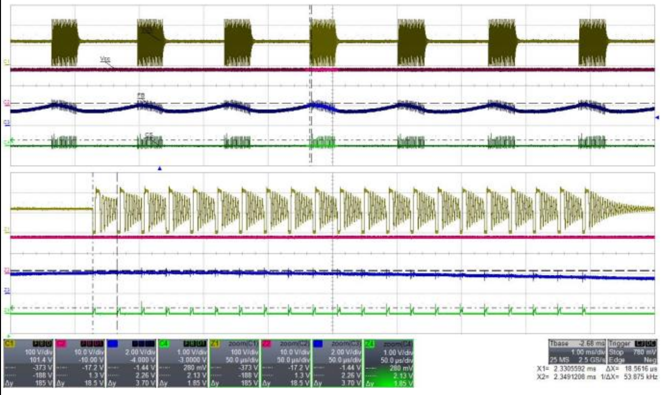
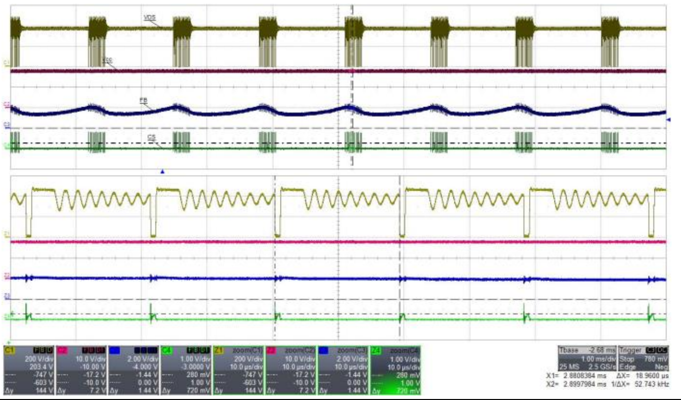
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC ABM. Burst-on at FB voltage 1.95 V ($V_{FB\_Bon\_NISO}$) and burst-off at 1.55 V ($V_{FB\_BOff\_NISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at ~54 kHz (f_{OSC2_ABM}).	264 V AC ABM. Burst-on at FB voltage 1.95 V ($V_{FB\_Bon\_NISO}$) and burst-off at 1.55 V ($V_{FB\_Boff\_NISO}$). CS voltage at 0.27 V (V_{CS_BHP}). Switching frequency at ~53 kHz (f_{OSC2_ABM}).

Figure 27 **During ABM**

10.10 Leaving ABM

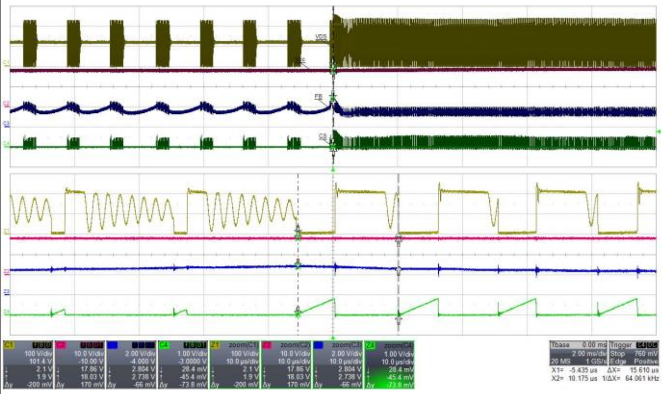
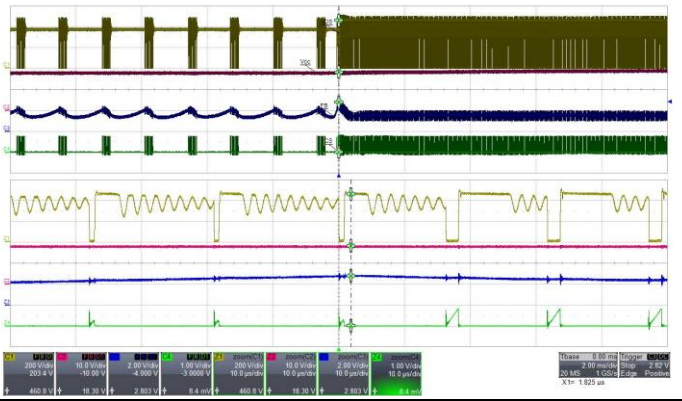
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC leaves ABM at FB voltage higher than 2.73 V (V_{FB_LB})	264 V AC leaves ABM at FB voltage higher than 2.73 V (V_{FB_LB})

Figure 28 **Leaving ABM**

10.11 V_{CC} OV/UV protection

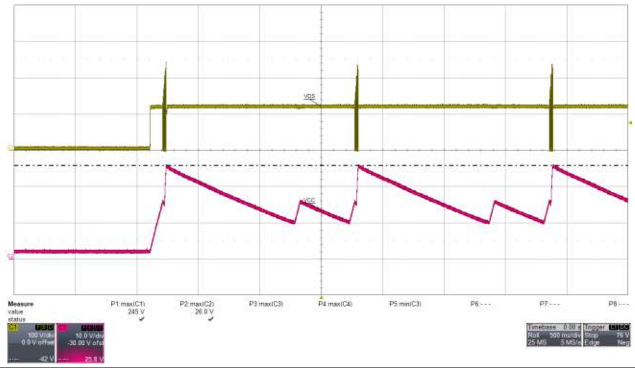
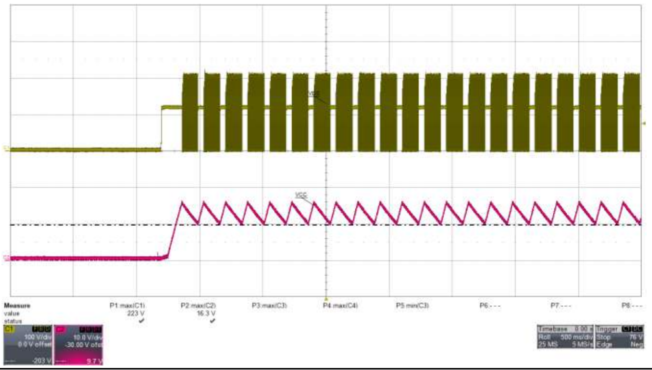
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage
85 V AC start-up at full load. Trigger V_{CC} OVP at V_{CC} voltage greater than 25.5 V (V_{VCC_OVP}). Odd-skip auto-restart mode. (Short R17.)	85 V AC start-up at no load. Trigger V_{CC} UVP at V_{CC} voltage less than 10 V (V_{VCC_OFF}). Auto-restart mode. (Open D3.)

Figure 29 V_{CC} OV/UV protection

10.12 Overload protection

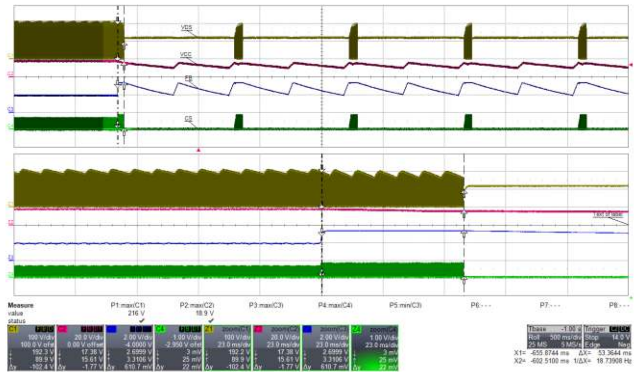
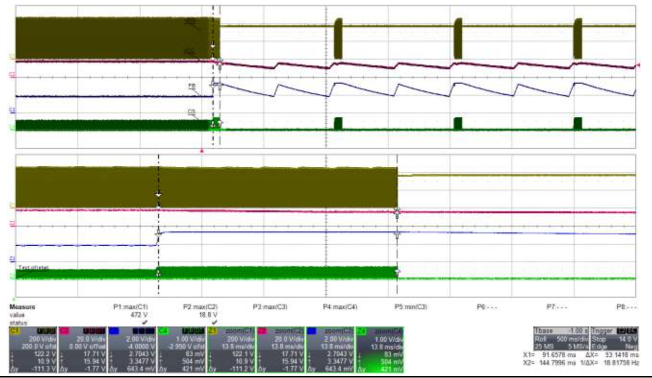
	
C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage	C1 (yellow) : Drain voltage C2 (purple) : V_{CC} voltage C3 (blue) : FB pin voltage C4 (green) : CS voltage
85 V AC at full load to overload. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.	264 V AC at full load to overload. Trigger protection at FB pin voltage greater than 2.73 V (V_{FB_OLP}) for more than 54 ms ($t_{FB\_OLP\_B}$). Odd-skip auto-restart mode.

Figure 30 Overload protection

11 Appendix A: Transformer design and spreadsheet [3]

Calculation tool for FF flyback converter using fifth-generation CoolSET™ (Version 1.1)

Project:	REF_5BR3995BZ_16W1
Application:	Aux for outdoor air-conditioner unit
CoolSET™:	ICE5BR3995BZ
Date:	14 February 2022
Revision:	V1.1

Notes:
Enter design variables in orange-colored cells
Read design results in green-colored cells
Equation numbers are according to the design guide
Component designators refer to the calculation tool
Select component values based on standard values available
Voltage/current rating does not include design margin, voltage spikes and transient currents
In “Output regulation”, only fill in either isolated or non-isolated, whichever is applicable

	Description	Eq. #	Parameter	Unit	Value
Input, output, CoolSET™ specs					
Line input					
Input	Minimum AC input voltage		V_{ACMin}	[V]	85
Input	Maximum AC input voltage		V_{ACMax}	[V]	264
Input	Line frequency		f_{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage		$V_{DCRipple}$	[V]	25
Output 1 specs					
Input	Output voltage 1		V_{Out1}	[V]	12
Input	Output current 1		I_{Out1}	[A]	0.9
Input	Forward voltage of output diode 1		V_{FOut1}	[V]	0.6
Input	Output ripple voltage 1		$V_{OutRipple1}$	[V]	0.2
Result	Output power 1	Eq. 001	P_{Out1}	[W]	10.8
Result	Output load weight 1	Eq. 004	K_{L1}		0.68
Output 2 specs					
Input	Output voltage 2		V_{Out2}	[V]	8
Input	Output current 2		I_{Out2}	[A]	0.3
Input	Forward voltage of output diode 2		V_{FOut2}	[V]	0.2
Input	Output ripple voltage 2		$V_{OutRipple2}$	[V]	0.2
Result	Output power 2	Eq. 002	P_{Out2}	[W]	2.4
Result	Output load weight 2	Eq. 005	K_{L2}		0.15
Auxiliary					
Input	V_{CC} voltage		V_{Vcc}	[V]	18
Input	Vcc current			[A]	0.15
Input	Forward voltage of output diode 3		V_{FOut3}	[V]	0.4
Input	Forward voltage of V_{CC} diode (D2)		$V_{F\,Vcc}$	[V]	0.6
Result	Output power 3	Eq. 002	P_{Out2}	[W]	2.7
Power					
Input	Efficiency		η		0.83
Result	Nominal output power	Eq. 003	P_{OutNom}	[W]	15.90
Input	Maximum output power for overload protection		P_{OutMax}	[W]	17
Result	Maximum input power for overload protection	Eq. 006	P_{InMax}	[W]	19.88
Input	Minimum output power		P_{OutMin}	[W]	3

Controller/CoolSET™

	Controller/CoolSET™				ICE5BR3995BZ
Input	Switching frequency		f_S	[Hz]	65000
Input	Targeted max. drain source voltage		V_{DSMax}	[V]	800
Input	Max. ambient temperature		T_{amax}	[°C]	50

Diode bridge and input capacitor

Diode bridge

Input	Power factor		cosφ		0.6
Result	Maximum AC input current	Eq. 007	I_{ACRMS}	[A]	0.390
Result	Peak voltage at V_{ACMax}	Eq. 008	$V_{DCMaxPk}$	[V]	373.35

Input capacitor

Result	Peak voltage at V_{ACMin}	Eq. 009	$V_{DCMinPk}$	[V]	120.21
Result	Selected minimum DC input voltage	Eq. 010	$V_{DCMinSet}$	[V]	95.21
Result	Discharging time at each half-line cycle	Eq. 011	T_D	[ms]	6.59
Result	Required energy at discharging time of input capacitor	Eq. 012	W_{In}	[Ws]	0.13
Result	Calculated input capacitor	Eq. 013	C_{INCal}	[µF]	48.66
Input	Select input capacitor (C1)		C_{in}	[µF]	44
Result	Calculated minimum DC input voltage	Eq. 015	V_{DCMin}	[V]	92.16

Transformer design

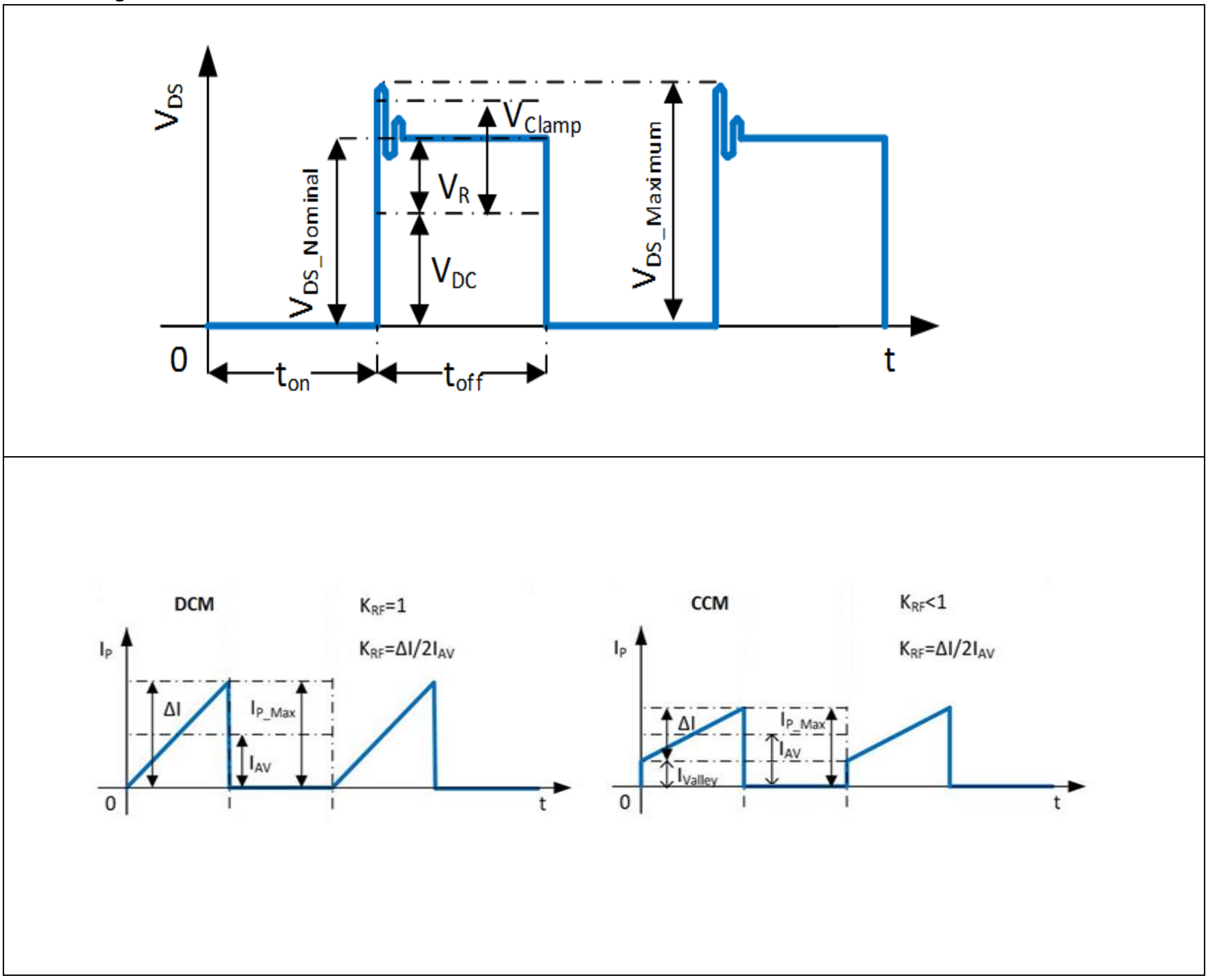


Figure 31 Drain voltage and current waveform

Primary inductance and winding currents

Input	Reflection voltage		V_{RSET}	[V]	92

Result	Maximum duty cycle	Eq. 016	D_{Max}		0.50
Input	Select current ripple factor		K_{RF}		1
Result	Primary inductance	Eq. 017	L_P	[H]	8.20E-04
Result	Primary turn-on average current	Eq. 018	I_{AV}	[A]	0.43
Result	Primary peak-to-peak current	Eq. 019	ΔI	[A]	0.86
Result	Primary peak current	Eq. 020	I_{PMax}	[A]	0.86
Result	Primary valley current	Eq. 021	I_{Valley}	[A]	0.00
Result	Primary RMS current	Eq. 022	I_{PRMS}	[A]	0.352

Select core type

Input	Select core type				2
Result	Core type				E25/13/7
Result	Core material				N87
Result	Maximum flux density		B_{Max}	[T]	0.3
Result	Cross-sectional area		A_e	[mm²]	52
Result	Bobbin width		BW	[mm]	15.6
Result	Winding cross-section		A_N	[mm²]	61
Result	Average length of turn		l_N	[mm]	50

Winding calculation

Result	Calculated minimum number of primary turns	Eq. 023	N_{PCal}	Turns	45.40
Input	Select number of primary turns		N_P	Turns	58
Result	Calculated number of secondary 1 turns	Eq. 024	N_{S1Cal}	Turns	7.94
Input	Select number of secondary 1 turns		N_{S1}	Turns	8
Result	Calculated number of secondary 2 turns	Eq. 025	N_{S2Cal}	Turns	5.17
Input	Select number of secondary 2 turns		N_{S2}	Turns	5
Result	Calculated number of auxiliary turns	Eq. 026	N_{VccCal}	Turns	11.81
Input	Select number of auxiliary turns		N_{Vcc}	Turns	12
Result	Calculated V_{CC} voltage	Eq. 027	V_{VccCal}	[V]	18.30

Post calculation

Result	Primary to secondary 1 turns ratio	Eq. 028	N_{PS1}		7.25
Result	Primary to secondary 2 turns ratio	Eq. 029	N_{PS2}		11.60
Result	Post-calculated reflected voltage	Eq. 030	V_{RPost}	[V]	91.35
Result	Post-calculated maximum duty cycle	Eq. 031	$D_{MaxPost}$		0.50
Result	Duty cycle prime	Eq. 032	D_{Max}'		0.50
Result	Actual flux density	Eq. 033	B_{MaxAct}	[T]	0.235
Result	Maximum DC input voltage for CCM operation	Eq. 034	$V_{DCmaxCCM}$	[V]	92.82

Transformer winding design

Input	Margin according to safety standard		M	[mm]	0
Input	Copper space factor		f_{Cu}		0.4
Result	Effective bobbin window	Eq. 035	BW_E	[mm]	15.6
Result	Effective winding cross-section	Eq. 036	A_{Ne}	[mm²]	61.0
Input	Primary winding area factor		AF_{NP}		0.45
Input	Secondary 1 winding area factor		AF_{NS1}		0.30
Input	Secondary 2 winding area factor		AF_{NS2}		0.15
Input	Auxiliary winding area factor		AF_{NVcc}		0.10

Primary winding

Result	Calculated copper wire cross-sectional area	Eq. 037	A_{PCal}	[mm²]	0.1893

Result	Calculated maximum wire size	Eq. 038	AWG_{PCal}		24
Input	Select wire size		AWG_{P}		28
Input	Select number of parallel wires		nw_{P}		1
Result	Copper wire diameter	Eq. 039	d_{P}	[mm]	0.32
Result	Copper wire cross-sectional area	Eq. 040	A_{P}	[mm²]	0.0821
Result	Wire current density	Eq. 041	S_{P}	[A/mm²]	4.29
Input	Insulation thickness		INS_{P}	[mm]	0.01
Result	Turns per layer	Eq. 042	NL_{P}	Turns/layer	45
Result	Number of layers	Eq. 043	Ln_{P}	Layers	2

Secondary 1 winding

Result	Calculated copper wire cross-sectional area	Eq. 044	A_{NS1Cal}	[mm²]	0.9150
Result	Calculated maximum wire size	Eq. 045	AWG_{S1Cal}		18
Input	Select wire size		AWG_{S1}		22
Input	Select number of parallel wires		nw_{S1}		1
Result	Copper wire diameter	Eq. 046	d_{S1}	[mm]	0.6465
Result	Copper wire cross-sectional area	Eq. 047	A_{S1}	[mm²]	0.3282
Result	Peak current	Eq. 048	I_{S1Max}	[A]	4.2527
Result	RMS current	Eq. 049	I_{S1RMS}	[A]	1.7431
Result	Wire current density	Eq. 050	S_{S1}	[A/mm²]	5.31
Input	Insulation thickness		INS_{S1}	[mm]	0.02
Result	Turns per layer	Eq. 051	NL_{S1}	Turns/layer	8
Result	Number of layers	Eq. 052	Ln_{S1}	Layers	1

Secondary 2 winding

Result	Calculated copper wire cross-sectional area	Eq. 053	A_{NS2Cal}	[mm²]	0.7320
Result	Calculated maximum wire size	Eq. 054	AWG_{S2Cal}		19
Input	Select wire size		AWG_{S2}		24
Input	Select number of parallel wires		nw_{S2}		1
Result	Copper wire diameter	Eq. 055	d_{S2}	[mm]	0.5131
Result	Copper wire cross-sectional area	Eq. 056	A_{S2}	[mm²]	0.2068
Result	Peak current	Eq. 057	I_{S2Max}	[A]	1.5121
Result	RMS current	Eq. 058	I_{S2RMS}	[A]	0.6198
Result	Wire current density	Eq. 059	S_{S2}	[A/mm²]	3.00
Input	Insulation thickness		INS_{S2}	[mm]	0.02
Result	Turns per layer	Eq. 060	NL_{S2}	Turns/layer	28
Result	Number of layers	Eq. 061	Ln_{S2}	Layers	1

RCD clamper and CS resistor

RCD clamper circuit

Input	Leakage inductance percentage		$L_{LK\%}$	[%]	2
Result	Leakage inductance	Eq. 062	L_{LK}	[H]	1.64E-05
Result	Clamping voltage	Eq. 063	V_{Clamp}	[V]	335.30
Result	Calculated clamping capacitor	Eq. 064	$C_{ClampCal}$	[nF]	0.09
Input	Select clamping capacitor value (C2)		C_{clamp}	[nF]	1
Result	Calculated clamping resistor	Eq. 065	$R_{clampCal}$	[kΩ]	436.8
Input	Select clamping resistor value (R4)		R_{clamp}	[kΩ]	240

CS resistor

Input	CS threshold value from datasheet		V_{CS_N}	[V]	0.8
Result	Calculated CS resistor (R8A, R8B)	Eq. 066	R_{sense}	[Ω]	0.93

Output rectifier

Secondary 1 output rectifier

Result	Diode reverse voltage	Eq. 067	$V_{RDiode1}$	[V]	63.50
Result	Diode RMS current		I_{S1RMS}	[A]	1.74
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.5
Input	Number of clock periods		n_{cp1}		20
Result	Output capacitor ripple current	Eq. 068	$I_{Ripple1}$	[A]	1.49
Result	Calculated minimum output capacitor	Eq. 069	$C_{Out1Cal}$	[µF]	554
Input	Select output capacitor value (C152)		C_{Out1}	[µF]	560
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR1}	[Ω]	0.032
Input	Number of parallel capacitors		nc_{COut1}		1
Result	Zero frequency of output capacitor	Eq. 070	f_{ZCOut1}	[kHz]	8.88
Result	First-stage ripple voltage	Eq. 071	$V_{Ripple1}$	[V]	0.136085
Input	Select LC filter inductor value (L151)		L_{out1}	[µH]	4.7
Result	Calculated LC filter capacitor	Eq. 072	C_{LCCal1}	[µF]	68.3
Input	Select LC filter capacitor value (C153)		C_{LC1}	[µF]	220
Result	LC filter frequency	Eq. 073	f_{LC1}	[kHz]	4.95
Result	Second-stage ripple voltage	Eq. 074	$V_{2ndRipple1}$	[mV]	0.78

Secondary 2 output rectifier

Result	Diode reverse voltage	Eq. 075	$V_{RDiode2}$	[V]	40.19
Result	Diode RMS current		I_{S2RMS}	[A]	0.62
Input	Max. voltage undershoot at output capacitor		ΔV_{Out1}	[V]	0.3
Input	Number of clock periods		n_{cp2}		20
Result	Output capacitor ripple current	Eq. 076	$I_{Ripple2}$	[A]	0.54
Result	Calculated minimum output capacitor	Eq. 077	$C_{Out2Cal}$	[µF]	308
Input	Select output capacitor value (C152)		C_{Out2}	[µF]	470
Input	ESR (Z_{max}) value from datasheet at 100 kHz		R_{ESR2}	[Ω]	0.032
Input	Number of parallel capacitors		nc_{COut2}		1

V_{CC} diode and capacitor

V_{CC} diode and capacitor

Result	Auxiliary diode reverse voltage (D2)	Eq. 083	$V_{RDiodeVCC}$	[V]	95.55
Input	Soft-start time from datasheet		t_{ss}	[ms]	12
Input	$I_{VCC,Normal2}$ from datasheet		$I_{VCC\_Charge3}$	[mA]	3
Input	V_{CC} on-threshold		V_{VCC_ON}	[V]	16
Input	V_{CC} off-threshold		V_{VCC_OFF}	[V]	10
Result	Calculated V_{CC} capacitor	Eq. 084	C_{VCCCal}	[µF]	6.00
Input	Select V_{CC} capacitor (C3)		C_{VCC}	[µF]	22
Input	V_{CC} short threshold from datasheet		V_{VCC_SCP}	[V]	1.1
Input	$I_{VCC\_Charge1}$ from datasheet		$I_{VCC\_Charge1}$	[mA]	0.2
Result	Start-up time	Eq. 085	$t_{StartUp}$	[ms]	230.267

Calculation of losses

Input diode bridge

Input	Diode bridge forward voltage		V_{FBR}	[V]	0.6
Result	Diode bridge power loss	Eq. 086	P_{DIN}	[W]	0.47

Transformer copper

Result	Primary winding copper resistance	Eq. 087	R_{PCu}	[mΩ]	607.52
Result	Secondary 1 winding copper resistance	Eq. 088	R_{S1Cu}	[mΩ]	20.96
Result	Secondary 2 winding copper resistance	Eq. 089	R_{S2Cu}	[mΩ]	20.79
Result	Primary winding copper loss	Eq. 090	P_{PCu}	[mW]	75.44
Result	Secondary 1 winding copper loss	Eq. 091	P_{S1Cu}	[mW]	63.69
Result	Secondary 2 winding copper loss	Eq. 092	P_{S2Cu}	[mW]	7.99
Result	Total transformer copper loss	Eq. 093	P_{Cu}	[W]	0.1471

Output rectifier diode

Result	Secondary 1 diode loss	Eq. 094	P_{Diode1}	[W]	1.05
Result	Secondary 2 diode loss	Eq. 095	P_{Diode2}	[W]	0.12

RCD clamper circuit

Result	RCD clamper loss	Eq. 096	$P_{Clamper}$	[W]	0.51

CS resistor

Result	CS resistor loss	Eq. 097	P_{CS}	[W]	0.12

MOSFET

Input	$R_{DS(on)}$ from datasheet		$R_{DS(on)}$ at T_A = 125°C	[Ω]	7.69
Input	$C_{o(er)}$ from datasheet		$C_{o(er)}$	[pF]	5
Input	External drain-to-source capacitance		C_{DS}	[pF]	0
Result	Switch-on loss at minimum AC input voltage	Eq. 098	$P_{SONMinAC}$	[W]	0.0055
Result	Conduction loss at minimum AC input voltage	Eq. 099	$P_{condMinAC}$	[W]	0.9550
Result	Total MOSFET loss at minimum AC input voltage	Eq. 100	$P_{MOSMinAC}$	[W]	0.9604
Result	Switch-on loss at maximum AC input voltage	Eq. 101	$P_{SONMaxAC}$	[W]	0.0351
Result	Conduction loss at maximum AC input voltage	Eq. 102	$P_{condMaxAC}$	[W]	0.2357
Result	Total MOSFET loss at maximum AC input voltage	Eq. 103	$P_{MOSMaxAC}$	[W]	0.2708
Result	Total MOSFET loss (from minimum or maximum AC)		P_{MOS}	[W]	0.9604

Controller

Input	Controller current consumption		I_{VCC_Normal}	[mA]	0.9
Result	Controller loss	Eq. 104	P_{Ctrl}	[W]	0.0165

Efficiency after losses

Result	Total power loss	Eq. 105	P_{Losses}	[W]	3.38
Result	Post calculated efficiency	Eq. 106	η_{Post}	%	82.99%

CoolSET™/MOSFET temperature

CoolSET™/MOSFET temperature

Input	Enter thermal resistance junction-ambient (include copper pour)		R_{thJA_As}	[°K/W]	91
Result	Temperature rise	Eq. 107	ΔT	[°K]	87.4
Result	Junction temperature at T_{amax}	Eq. 108	Tjmax	°C	137.4

Note: T_{Jmax} was calculated by using maximum $R_{DS(on)}$ at 125℃ with footprint copper area as heatsink, only for reference.

Output regulation (non-isolated)

Input	Error amplifier reference voltage		V_{ERR_REF}	[V]	1.8
Input	Weighted regulation factor of V_{O1}		W_1	%	100%
Input	Select voltage divider R_{O1} (R11)		R_{O1}	[kΩ]	39
Result	Calculated voltage divider RO2	Eq 125	R_{O2cal}	[kΩ]	221.00
Input	Select voltage divider RO2 (R153)		R_{O2}	[kΩ]	220.0

Final design

Electrical

Minimum AC voltage			[V]	85
Maximum AC voltage			[V]	264
Maximum input current			[A]	0.23
Minimum DC voltage			[V]	92
Maximum DC voltage			[V]	373
Maximum output power			[W]	16.5
Output voltage 1			[V]	12.0
Output ripple voltage 1			[mV]	0.8
Output voltage 1			[V]	8.0
Transformer peak current			[A]	0.86

Maximum duty cycle				0.50
Reflected voltage			[V]	91
Copper losses			[W]	0.15
MOSFET losses			[W]	0.96
Sum losses			[W]	3.38
Efficiency			[Percent]	82.99%

Transformer

Core type				E25/13/7
Core material				N87
Effective core area			[mm^2]	52
Maximum flux density			[mT]	235
Inductance			[µH]	820
Margin			[mm]	0
Primary turns			Turns	58
Primary copper wire size			AWG	28
Number of primary copper wires in parallel				1
Primary layers			Layer	2
Secondary 1 turns (N_{S1})			Turns	8
Secondary 1 copper wire size			AWG	22
Number of secondary 1 copper wires in parallel				1
Secondary 1 layers			Layer	1
Auxiliary turns			Turns	5
Leakage inductance			[µH]	24

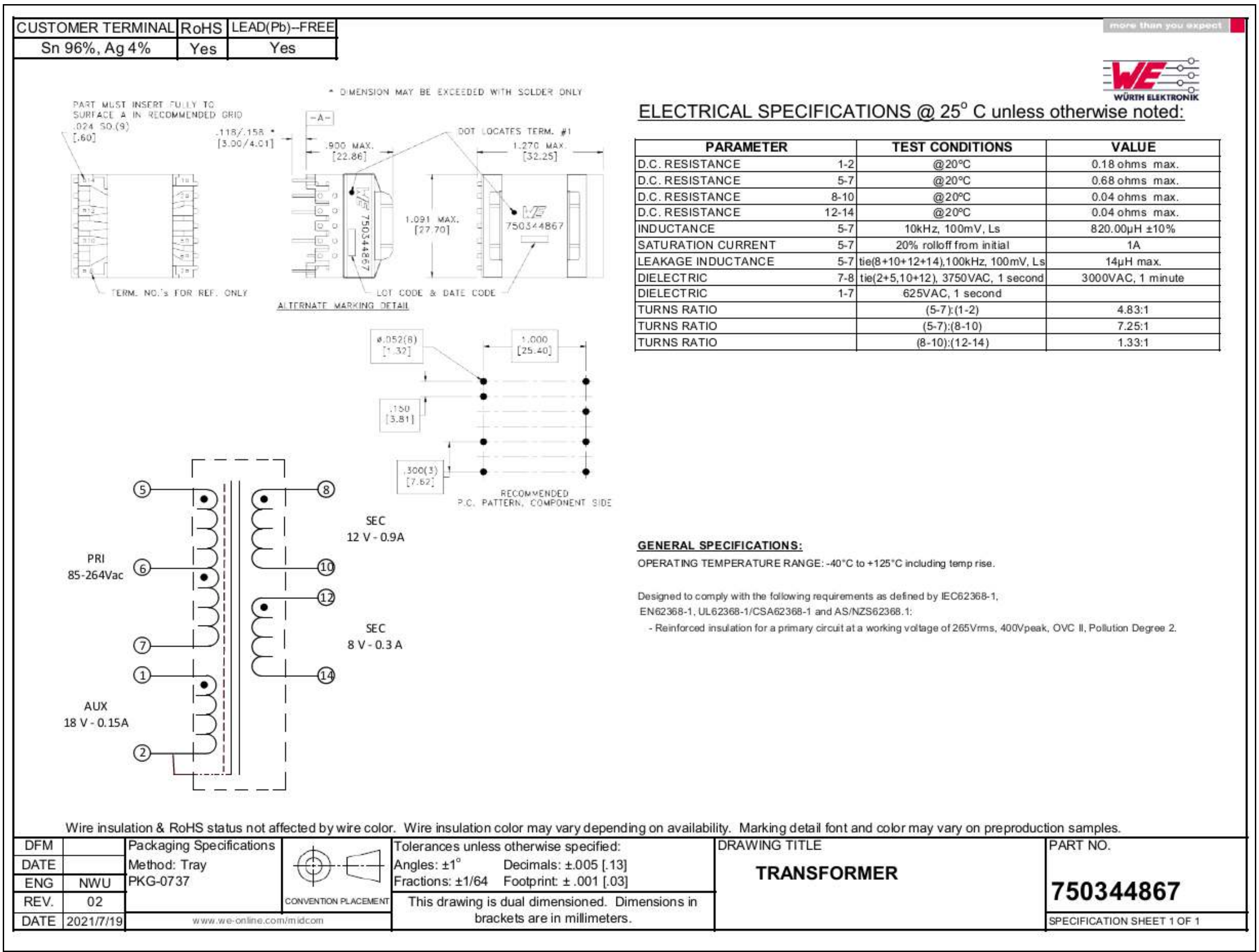
Components

Input capacitor (C1)			[µF]	44.0
Secondary 1 output capacitor (C152)			[µF]	560.0
Secondary 1 output capacitor in parallel				1.0
Secondary 1 LC filter inductor			[µH]	4.7
Secondary 1 LC filter capacitor			[µF]	220.0
Secondary 2 output capacitor (C152)			[µH]	470.0
Secondary 2 output capacitor in parallel			[µF]	1
V_{CC} capacitor (C3)			[µF]	22.0
Sense resistor (R8A, R8B)			[Ω]	0.93
Clamping resistor (R4)			[kΩ]	240.0
Clamping capacitor (C2)			[nF]	1.0

Regulation components (non-isolated)

Voltage divider (R11)		R_{O1}	[kΩ]	39.0
Voltage divider (V_{O1} sense) (R153)		R_{O2}	[kΩ]	220.0

12 Appendix B: WE transformer specification



CUSTOMER TERMINAL	RoHS	LEAD(Pb)–FREE
Sn 96%, Ag 4%	Yes	Yes

ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-2	@20°C	0.18 ohms max.
D.C. RESISTANCE	5-7	@20°C	0.68 ohms max.
D.C. RESISTANCE	8-10	@20°C	0.04 ohms max.
D.C. RESISTANCE	12-14	@20°C	0.04 ohms max.
INDUCTANCE	5-7	10kHz, 100mV, Ls	820.00µH ±10%
SATURATION CURRENT	5-7	20% rolloff from initial	1A
LEAKAGE INDUCTANCE	5-7	tie(8+10+12+14),100kHz, 100mV, Ls	14µH max.
DIELECTRIC	7-8	tie(2+5,10+12), 3750VAC, 1 second	3000VAC, 1 minute
DIELECTRIC	1-7	625VAC, 1 second	
TURNS RATIO		(5-7):(1-2)	4.83:1
TURNS RATIO		(5-7):(8-10)	7.25:1
TURNS RATIO		(8-10):(12-14)	1.33:1

GENERAL SPECIFICATIONS:

OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC62368-1, EN62368-1, UL62368-1/CSA62368-1 and AS/NZS62368.1:

- Reinforced insulation for a primary circuit at a working voltage of 265Vrms, 400Vpeak, OVC II, Pollution Degree 2.

Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability. Marking detail font and color may vary on preproduction samples.

DFM		Packaging Specifications		Tolerances unless otherwise specified:	DRAWING TITLE	PART NO.
DATE		Method: Tray		Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER	
ENG	NWU	PKG-0737		Fractions: ±1/64 Footprint: ± .001 [.03]		750344867
REV.	02		CONVENTION PLACEMENT	This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		
DATE	2021/7/19	www.we-online.com/midcom				SPECIFICATION SHEET 1 OF 1

Figure 32 WE transformer specification

13 References

[1] Infineon Technologies AG: Fixed-frequency 800 V / 950 V CoolSET™, ICE5xRxxxxxZ Datasheet (V 1.0); 2022-02-22; **ICE5xRxxxxxZ Datasheet**

[2] Infineon Technologies AG: Fifth-generation fixed-frequency design guide (V 1.1); 2019-07-24; **Fifth-generation fixed-frequency design guide**

[3] Infineon Technologies AG: Calculation tool for fixed-frequency flyback converter using fifth-generation CoolSET™ (V 1.0); 2018-02-26; **Calculation tool fixed-frequency CoolSET™ 5th generation**

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-06-15	First release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-06-15

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_2101_PL21_2105_101156