PRELIMINARY DATA SHEET

SKY87609: 28 V Step-Down DC-DC Controller with Optional Synchronous MOSFET Driver

Applications

- Set-top boxes
- LCD TV LED backlighting
- Industrial applications

Features

- 4.5 V to 28 V input voltage
- Controller with internal 10 Ω refresh MOSFET
- Up to 6 A load current
- Optional low-side MOSFET driver
- Adjustable output voltage (0.9 V to 0.8 × V_{IN})
- Fixed 450 kHz switching frequency
- 4 ms soft-start period
- External compensation
- Less than 1 μA shutdown current
- Up to 97% efficiency
- Current limit protection
- Compact TSOPJW (12-pin, 2.85 mm × 3.00 mm) package (MSL1, 260 °C per JEDEC-J-STD-020)

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Description

The SKY87609 is a step-down DC-DC controller that operates over a wide 4.5 V to 28 V input voltage range and regulates output voltage as low as 0.9 V while supplying up to 6 A to the output. The 450 kHz switching frequency allows an efficient step-down regulator design.

The SKY87609 uses an adjustable output voltage that can be set from 0.9 V to 80% of the input voltage by an external resistive voltage divider. Internal soft-start prevents excessive inrush current without requiring an external capacitor.

The SKY87609 includes input under-voltage and over-current protection to prevent damage in the event of a fault. Thermal overload protection prevents damage to the SKY87609 or circuit board when operating beyond its thermal capability.

The SKY87609 is available in a small 12-pin 2.85 mm × 3.00 mm TSOPJW package.

A typical application circuit is shown in Figure 1. The pin configuration is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

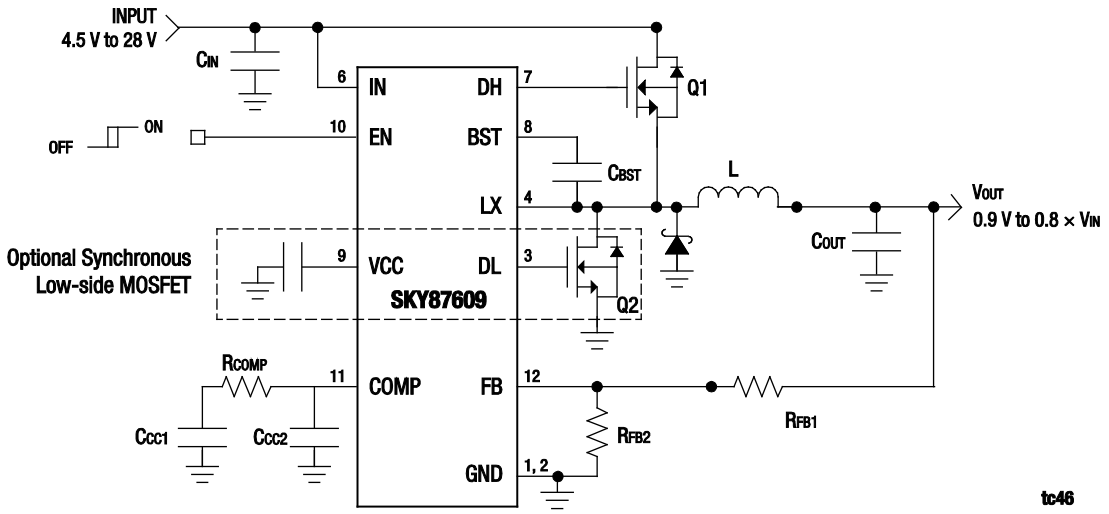

Figure 1. SKY87609 Typical Application Circuit

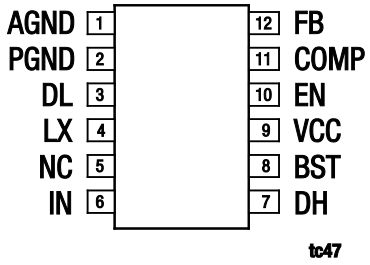

Figure 2. SKY87609 12-Pin TSOPJW (Top View)

Table 1. SKY87609 Signal Descriptions

Pin #	Name	Description
1	AGND	Analog ground. AGND is internally connected to the analog ground of the control circuitry.
2	PGND	Power ground. PGND is internally connected to the low-side driver and source of the 30 Ω refresh MOSFET.
3	DL	Low-side N-channel MOSFET driver output. For efficient designs, connect to the gate of the low-side N-channel MOSFET. DL switches between VCC and PGND. For simple non-synchronous designs, leave DL unconnected.
4	LX	Inductor switching node. LX is internally connected to the high-side driver and current-sense circuitry. Connect to the source of the high-side N-channel MOSFET, the power inductor, and the rectifier (diode or low-side MOSFET) as shown in Figure 1.
5	NC	Do not connect.
6	IN	Input supply. Connect IN to the input power source. Bypass IN to GND with a 10 µF or greater ceramic capacitor. IN externally connects to the source of the high-side N-channel MOSFET and internally connects to the linear regulators powering the controller and drivers.
7	DH	High-side N-channel MOSFET driver output.
8	BST	Boot-strapped high-side driver supply. Connect a 0.1 µF ceramic capacitor between BST and LX as shown in Figure 1.
9	VCC	Driver bypass. VCC is the output of the linear regulator used to power the MOSFET drivers. For synchronous designs, connect a 0.1 µF to 1 µF ceramic capacitor between VCC and PGND. For non-synchronous designs, the capacitor may be left open.
10	EN	Enable input. A logic high enables the controller. A logic low forces the SKY87609 into shutdown mode, placing the output into a high-impedance state and reducing the quiescent current to less than 1 µA.
11	COMP	Compensation pin of the error amplifier.
12	FB	Feedback input. FB senses the output voltage for regulation control. Connect a resistive divider network from the output to FB to GND to set the output voltage accordingly. The FB regulation threshold is 0.9 V.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY87609 are provided in Table 2. Thermal information is provided in Table 3, and electrical specifications are provided in Table 4.

Typical performance characteristics of the SKY87609 are illustrated in Figures 3 through 35.

Table 2. SKY87609 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Typical	Maximum	Units
IN to PGND	V_{IN}	–0.3		+30	V
LX to PGND	V_{LX}	–0.3		V_{IN} + 0.3	V
BST to PGND	V_{BST}	Vcc – 0.3		V_{IN} + 6.0	V
Vcc to AGND	V_{CC}	–0.3		7.5, or V_{IN} + 0.3	V
DH to LX	V_{DH}	–0.3		V_{BST} + 0.3	V
EN to AGND	V_{EN}	–0.3		+30	V
FB to AGND	V_{FB}	–0.3		+6.0	V
COMP to AGND	V_{COMP}	–0.3		+6.0	V
DL to PGND	V_{DL}	–0.3		V_{CC} – 0.3	V
AGND to PGND	V_{GND}	–0.3		+0.3	V

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. SKY87609 Thermal Information (Note 1)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Operating ambient temperature	T_A	–40		+85	°C
Operating junction temperature	T_J	–40		+150	°C
Maximum soldering temperature (at leads, 10 seconds)	T_{LEAD}		300		°C
Maximum junction-to-ambient thermal resistance	θ_{JA}		140		°C/W
Maximum power dissipation (Note 2)	P_D		0.7		W

Note 1: Mounted on 1 in^2 FR4 board.

Note 2: Derate 7 mW/°C above 25 °C.

Table 4. SKY87609 Electrical Specifications (Note 1)
(V_{IN} = 12 V, V_{EN} = 5 V, AGND = PGND, T_A = -40 °C to 85 °C [Typical Values are at T_A = 25 °C], Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Input voltage	V_{IN}		4.5		28	V
No load supply current	I_Q	No load current; not switching		1.6	3.2	mA
Shutdown current	I_{SHDN}	EN = GND, V_{IN} = 28 V		1	5	µA
Output voltage (Note 2)	V_{OUT}		V_{FB}		0.8 × V_{IN}	V
Nominal feedback voltage				0.9		V
FB accuracy	V_{FB}	V_{IN} = 24 V	0.88	0.90	0.92	V
FB leakage current	I_{FB}	FB = 1.5 V or GND	–0.2		+0.2	µA
Load regulation	ΔV_{OUT} / I_{OUT}	V_{IN} = 12 V, Vout = 5 V		0.5		%
Line regulation	ΔV_{OUT} / V_{IN}	V_{IN} = 4.5 V to 28 V		0.1		%
Oscillator frequency	f_{OSC}		380	450	520	kHz
Minimum on time	$t_{ON(MIN)}$			370	540	ns
Maximum duty cycle	D_{MAX}	No Load	80	83		%
Current limit voltage threshold	$V_{CL(TH)}$	IN to LX	400	500		mV
Refresh MOSFET On resistance	$R_{DS(ON)LO}$	V_{IN} = 5 V		10		Ω
Input under-voltage lockout	V_{UVLO}	V_{IN} rising, hysteresis = 200 mV	3.5		4.2	V
Over-temperature shutdown threshold	T_{SHDN}	Rising edge, hysteresis = 15 °C		150		°C
EN input logic threshold	V_{EN}		0.4		1.7	V
EN input current	I_{EN}	0.4 V, 12 V	–2.0		+25	µA
Soft-start period	t_{SS}			4		ms

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: The minimum output voltage must be greater than $t_{ON(MIN)} \times f_{OSC} \times V_{IN(MIN)}$ due to duty cycle limitations.

Typical Performance Characteristics

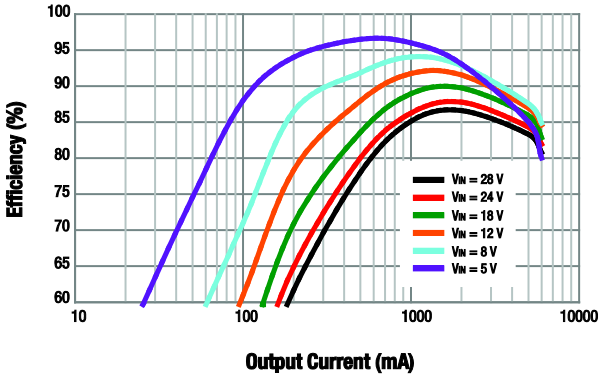

Figure 3. Efficiency vs Output Current (VOUT = 3.3 V)

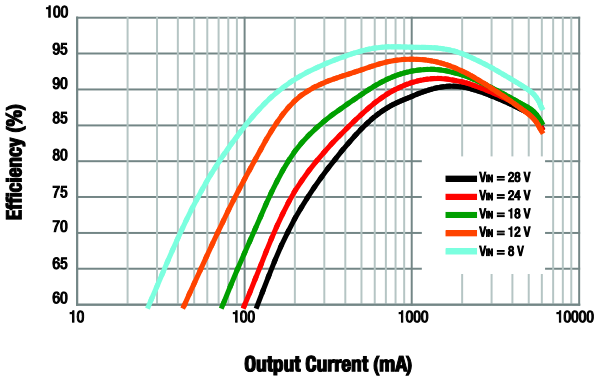

Figure 4. Efficiency vs Output Current (VOUT = 5.0 V)

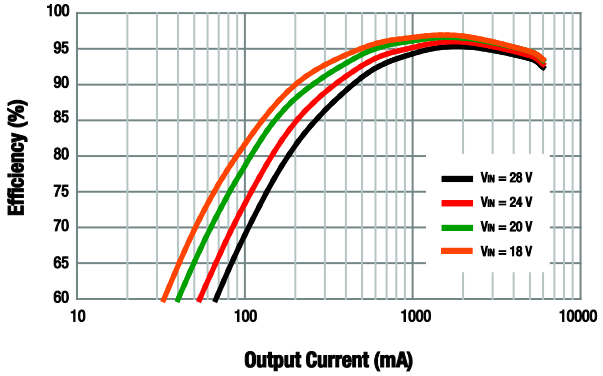

Figure 5. Efficiency vs Output Current (VOUT = 12 V)

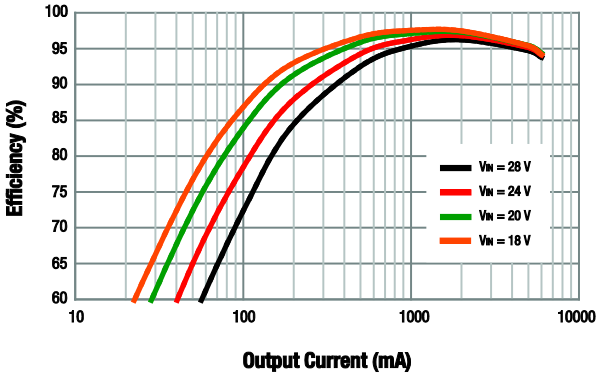

Figure 6. Efficiency vs Output Current (VOUT = 15 V)

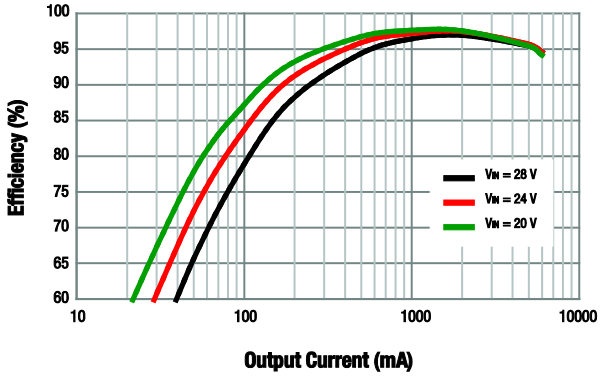

Figure 7. Efficiency vs Output Current (VOUT = 18 V)

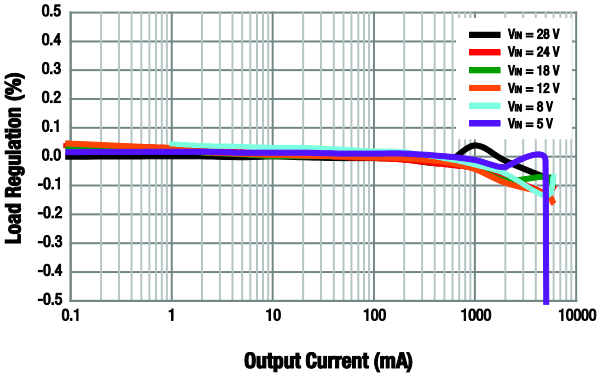

Figure 8. Load Regulation vs Output Current (VOUT = 3.3 V)

Typical Performance Characteristics

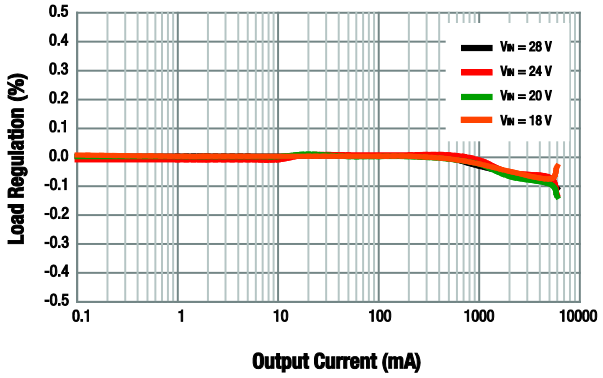

Figure 9. Load Regulation vs Output Current (VOUT = 12 V)

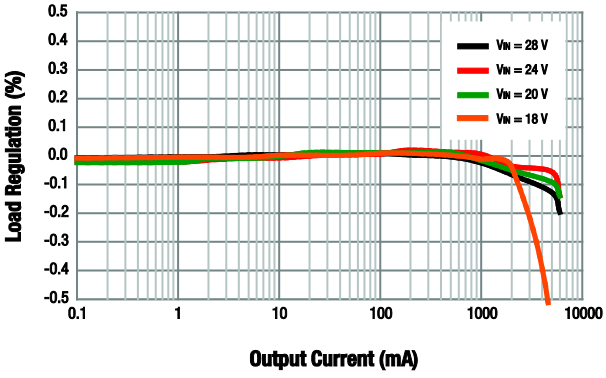

Figure 10. Load Regulation vs Output Current (VOUT = 15 V)

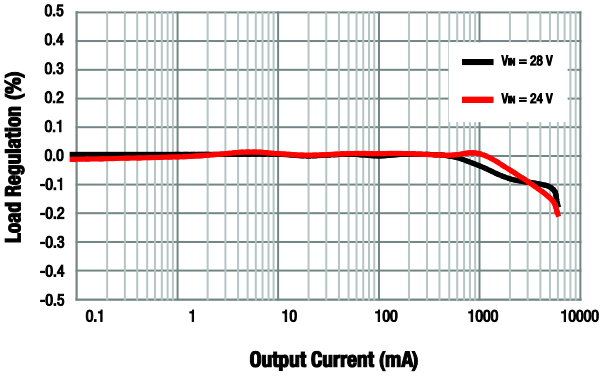

Figure 11. Load Regulation vs Output Current (VOUT = 18 V)

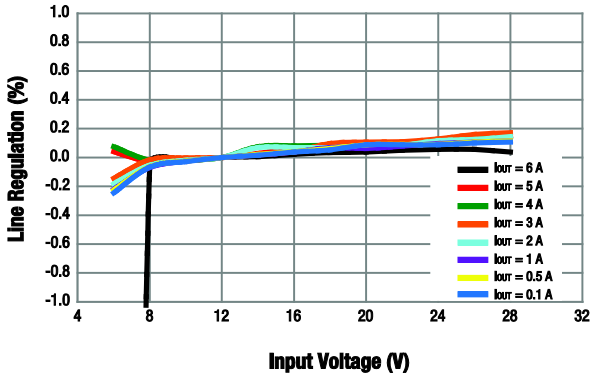

Figure 12. Line Regulation vs Input Voltage (VOUT = 3.3 V)

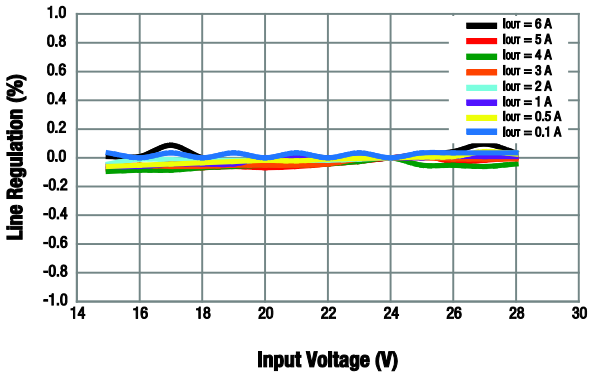

Figure 13. Line Regulation vs Input Voltage (VOUT = 12 V)

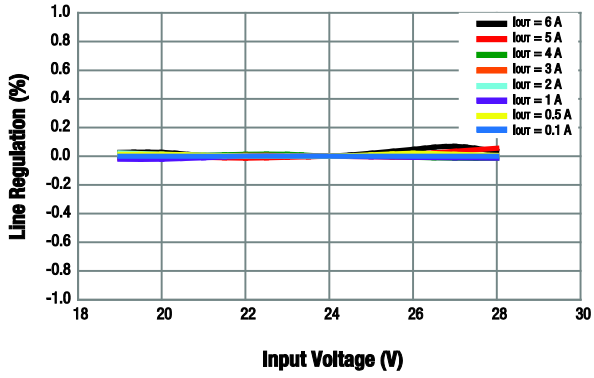

Figure 14. Line Regulation vs Input Voltage (VOUT = 15 V)

Typical Performance Characteristics

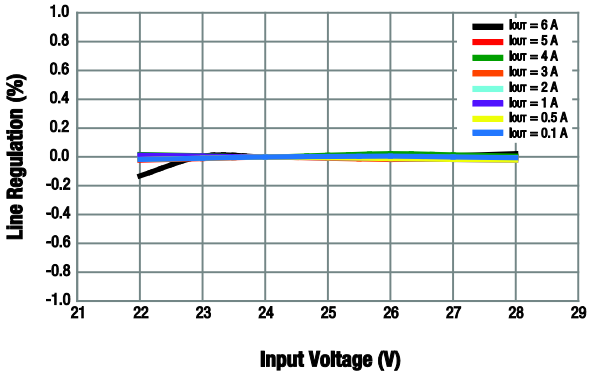

Figure 15. Line Regulation vs Input Voltage (VOUT = 18 V)

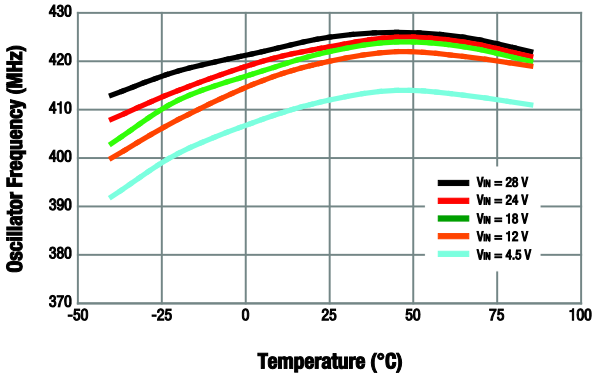

Figure 16. Oscillator Frequency vs Temperature (IOUT = 100 mA)

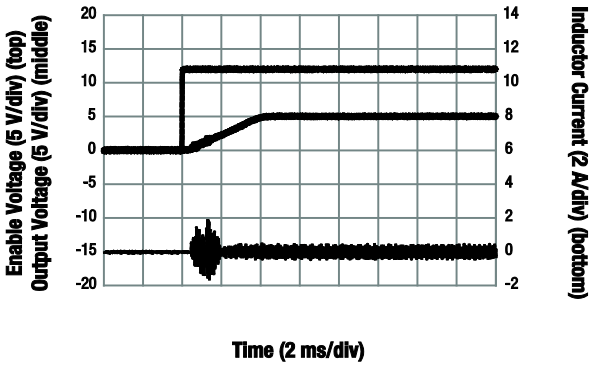

Figure 17. Soft Start (VOUT = 5 V, VIN = 12 V, IOUT = 0 A)

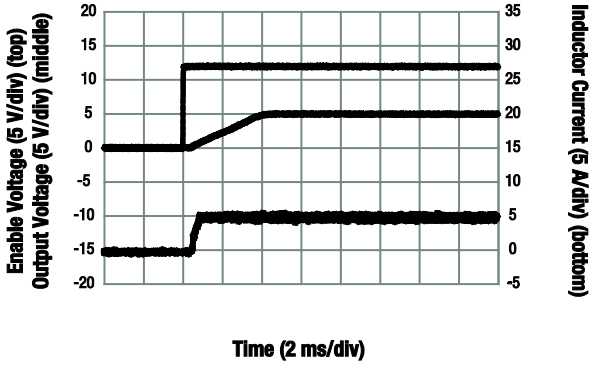

Figure 18. Soft Start (VOUT = 5 V, VIN = 12 V, IOUT = 5 A)

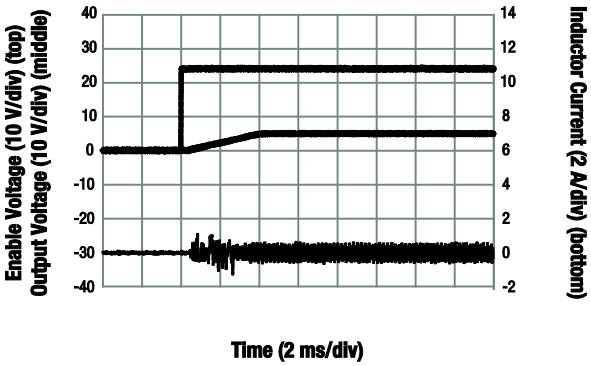

Figure 19. Soft Start (VOUT = 5 V, VIN = 24 V, IOUT = 0 A)

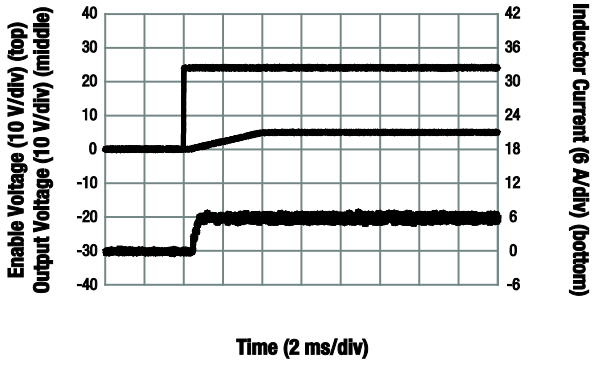

Figure 20. Soft Start (VOUT = 5 V, VIN = 24 V, IOUT = 6 A)

Typical Performance Characteristics

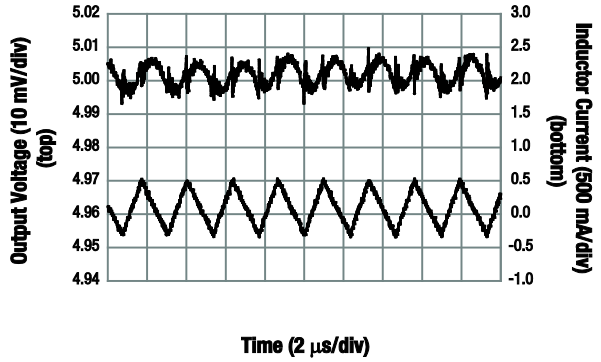

Figure 21. Output Voltage Ripple
(V_{OUT} = 5 V, V_{IN} = 12 V, I_{OUT} = 100 mA)

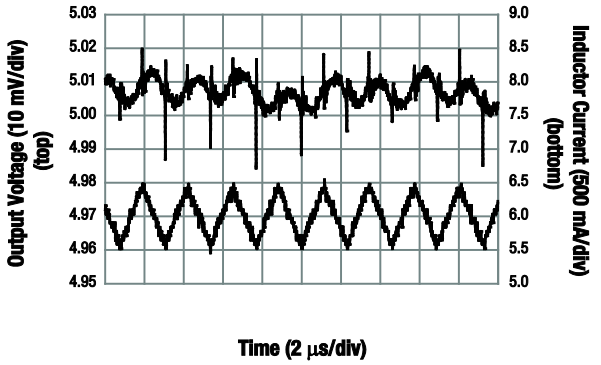

Figure 22. Output Voltage Ripple
(V_{OUT} = 5 V, V_{IN} = 12 V, I_{OUT} = 6 A)

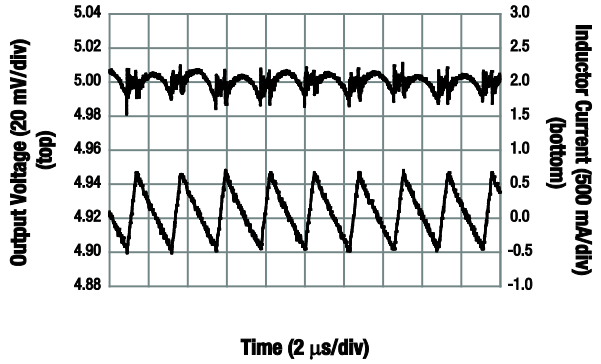

Figure 23. Output Voltage Ripple
(V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 100 mA)

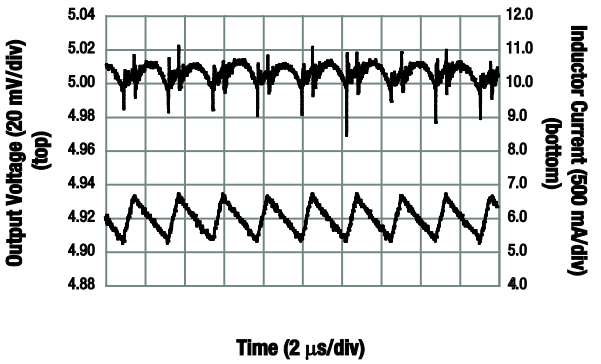

Figure 24. Output Voltage Ripple
(V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 6 A)

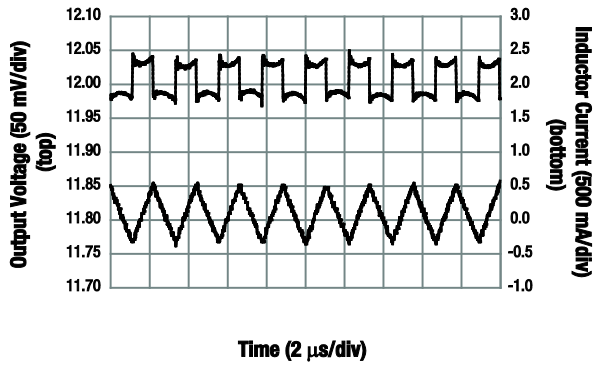

Figure 25. Output Voltage Ripple
(V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 100 mA)

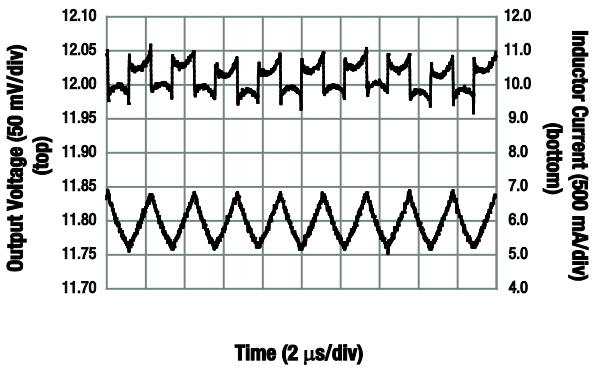

Figure 26. Output Voltage Ripple
(V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 6 A)

Typical Performance Characteristics

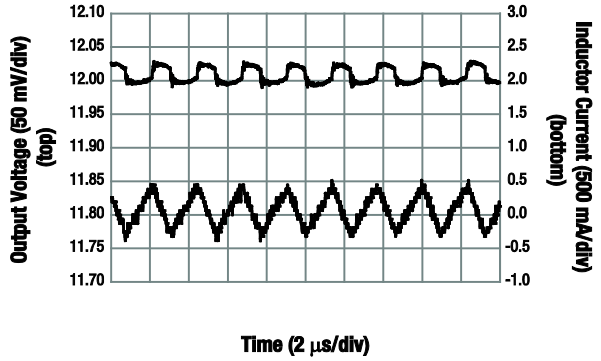

Figure 27. Output Voltage Ripple
(V_{OUT} = 15 V, V_{IN} = 24 V, I_{OUT} = 100 mA)

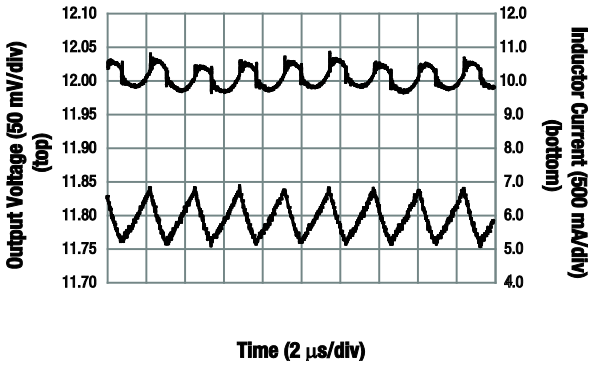

Figure 28. Output Voltage Ripple
(V_{OUT} = 15 V, V_{IN} = 24 V, I_{OUT} = 6 A)

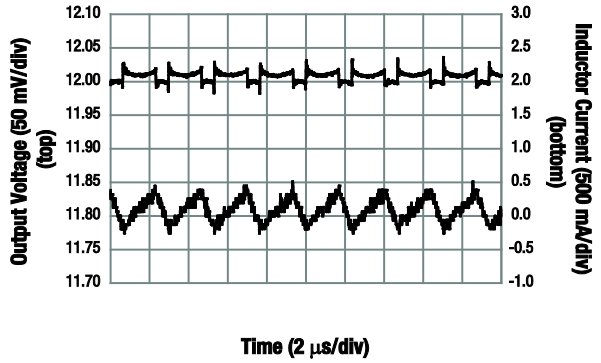

Figure 29. Output Voltage Ripple
(V_{OUT} = 18 V, V_{IN} = 24 V, I_{OUT} = 100 mA)

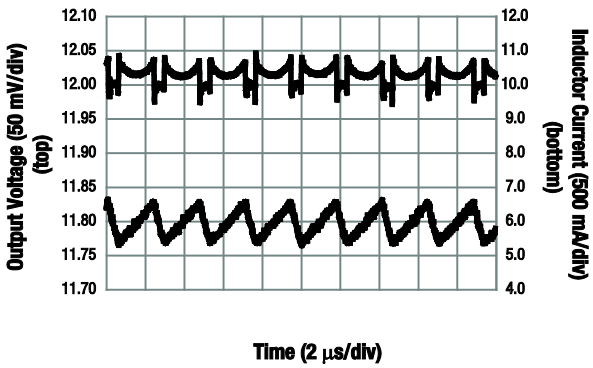

Figure 30. Output Voltage Ripple
(V_{OUT} = 18 V, V_{IN} = 24 V, I_{OUT} = 6 A)

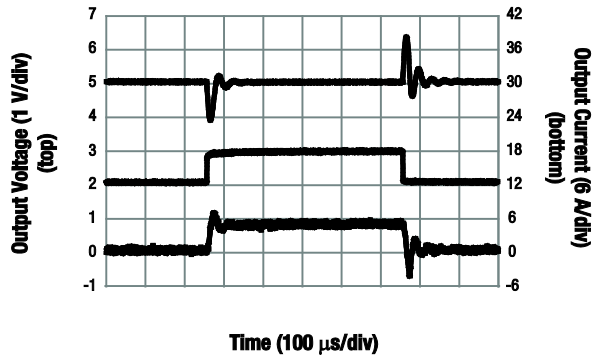

Figure 31. Load Transient
(V_{OUT} = 5 V, V_{IN} = 12 V, I_{OUT} = 0.1 to 6 A)

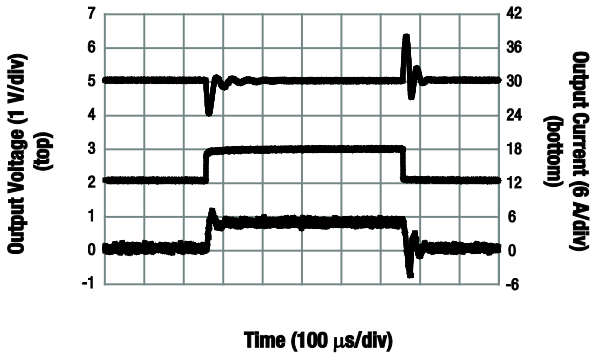

Figure 32. Load Transient
(V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 0.1 to 6 A)

Typical Performance Characteristics

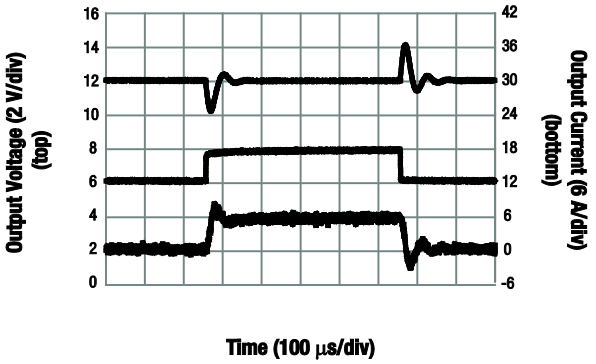

Figure 33. Load Transient
(V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 0.1 to 6 A)

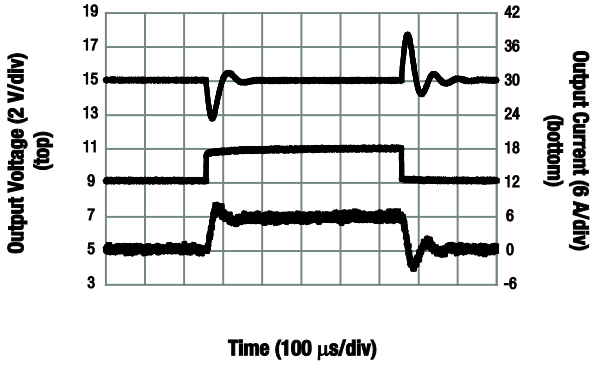

Figure 34. Load Transient
(V_{OUT} = 15 V, V_{IN} = 24 V, I_{OUT} = 0.1 to 6 A)

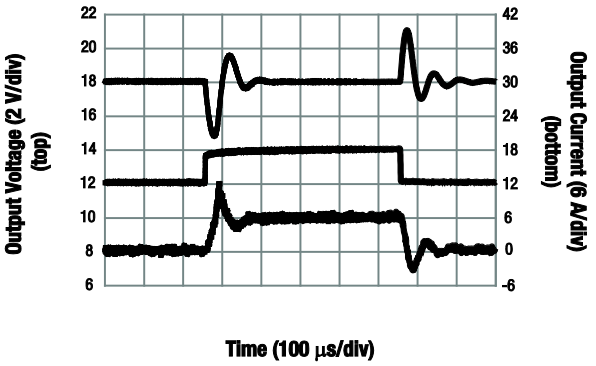

Figure 35. Load Transient
(V_{OUT} = 18 V, V_{IN} = 24 V, I_{OUT} = 0.1 to 6 A)

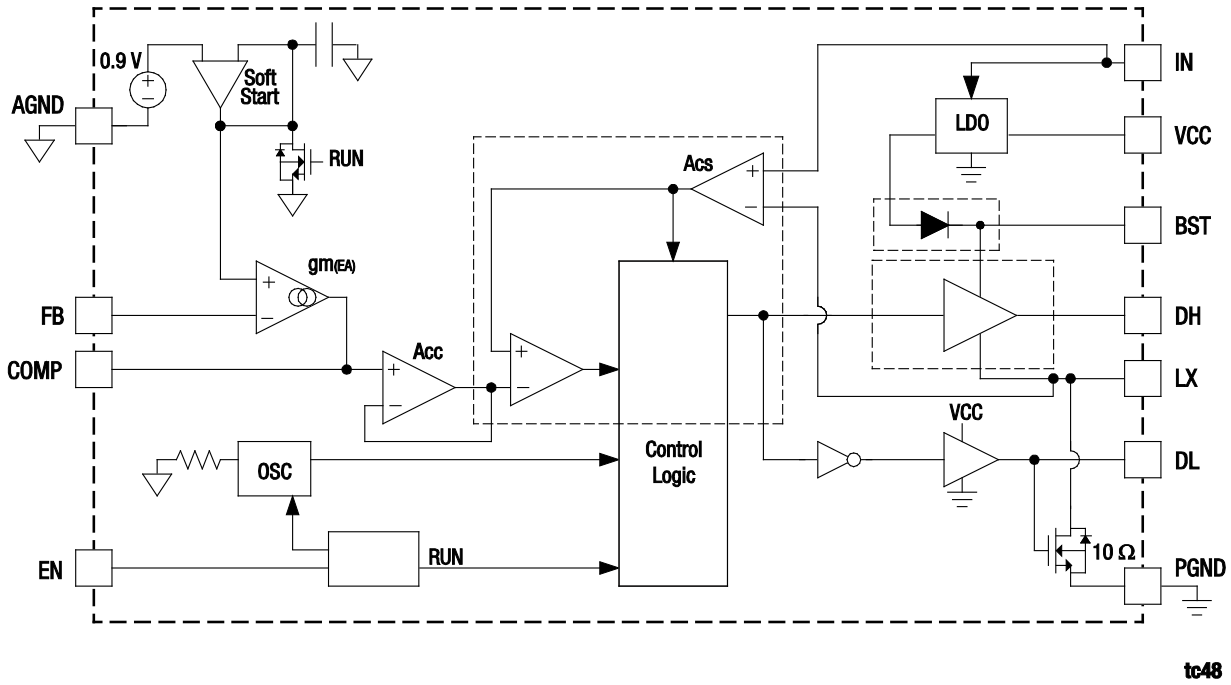

Figure 36. SKY87609 Functional Block Diagram

Functional Description

A functional block diagram is provided in Figure 36.

Control Scheme

The SKY87609 is a constant frequency, current-mode step-down controller. The controller has a low-side MOSFET driver and an internal 10 Ω boost capacitor refresh MOSFET that allows both synchronous and non-synchronous designs. A floating gate driver powers the high-side N-channel MOSFET from an external bootstrap capacitor through the BST pin. The capacitor is charged when LX is pulled low through an external rectifier, and the BST capacitor maintains sufficient voltage to enhance the high-side N-channel MOSFET during the on time.

The SKY87609 supports an adjustable output voltage using an external resistive voltage divider, allowing the output to be set to any voltage between 0.9 V and 80% of the input voltage. The SKY87609 switches at 450 kHz.

Current Limit Protection

The SKY87609 includes protection for overload and short-circuit conditions by limiting the peak inductor current. During the on time, the controller monitors the current through the high-side MOSFET (IN to LX voltage). If the voltage drop across the MOSFET exceeds 500 mV (typical), the regulator immediately turns off the high-side MOSFET.

Voltage Soft-Start

The soft-start circuit ramps the reference voltage from ground up to the 0.9 V nominal feedback regulation voltage (see the functional block diagram in Figure 36). The internal soft-start capacitor sets the soft-start period as 4 ms (typical).

The soft-start is discharged/reset if any of the following events occurs: the controller is disabled (EN is pulled low), the input voltage drops below the Under-Voltage Lockout (UVLO) threshold, or the thermal shutdown is activated.

Thermal Shutdown

The SKY87609 includes thermal protection that disables the controller when the die temperature reaches 150 °C. The thermal shutdown resets the soft-start circuit and automatically restarts when the temperature drops below 135 °C.

Application Information

To ensure that the maximum possible performance is obtained from the SKY87609, refer to the following application recommendations for component selection.

Design Methodology

This section details the component selection process for the SKY87609 in continuous conduction mode to assist with the design process. Many of the equations make heavy use of the small ripple approximation. This process includes the following steps:

1. Operational parameters definition
2. Output voltage setting
3. Inductor selection
4. Output capacitor selection
5. Input capacitor selection
6. Peak current limit setting
7. N-channel MOSFET(s) selection
8. Rectifying Schottky diode selection
9. Stability and compensation components selection
10. Bootstrap capacitor selection
11. Thermal consideration

Define Operational Parameters

Before starting the design, define the operating parameters of the application. These parameters include:

$V_{IN(MIN)}$: minimum input voltage, in Volts
$V_{IN(MAX)}$: maximum input voltage, in Volts
V_{OUT}: output voltage, in Volts
$I_{OUT(MAX)}$: maximum output current, in Amps
I_{CL}: desired typical cycle-by-cycle current limit, in Amps

Using the equation below:

$$V_{OUT} = D \times V_{IN}$$

where D is the duty cycle, the minimum and maximum duty cycles can be closely approximated by the following equations:

$$D_{(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}}$$

$$D_{(MAX)} = \frac{V_{OUT}}{V_{IN(MIN)}}$$

Both the minimum and maximum duty cycles actually are higher due to power losses in the conversion. The exact duty cycle depends on conduction and switching losses. The SKY87609 has a typical maximum duty cycle of 90%. If the maximum duty cycle is exceeded due to a low $V_{IN(MIN)}$ voltage, V_{OUT} is out of regulation, and can be determined by the following equation:

$$V_{OUT} = D_{MAX} \times V_{IN(MIN)}$$

where D_{MAX} = the maximum duty cycle of the SKY87609 (83% typical).

Setting the Output Voltage

The SKY87609 output voltage is adjustable from 0.9 V up to 80% of V_{IN} by connecting FB to the center tap of a resistor-divider between the output and GND (see Figure 37). The resistive feedback voltage divider sets the output voltage according to the following relationship:

$$R_{FB1} = \left(\frac{V_{OUT}}{0.9V} - 1 \right) \times R_{FB2}$$

which is rounded to the nearest 1% resistor value. $R_{FB}2$ is typically selected to be between 10 kΩ and 200 kΩ. The lower resistance value improves the noise immunity, but results in higher feedback current (reducing the efficiency).

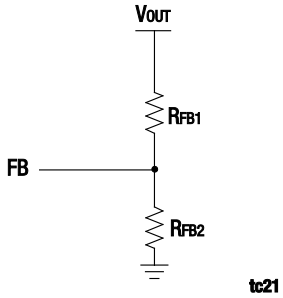

Figure 37. FB Resistor Divider

Table 5 shows the divider resistor value for different output voltages.

Table 5. Resistor Selection for Different Output Voltages

Output Voltage (V)	$R_{FB}1$ (kΩ) ($R_{FB}2$ = 20 kΩ)
1.5	13.3
3.3	53.6
5.0	91.0
8.0	158.0
10.0	200.0
12.0	249.0
15.0	316.0
18.0	383.0
20.0	422.0

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected to make the inductor current down slope meet the internal slope compensation requirements. The internal slope compensation is designed to be 75% of the inductor current down slope of 5 V output with a 6.8 µH inductor.

$$m_C = \frac{0.75 \times V_{OUT}}{L} = \frac{0.75 \times 5V}{0.68\mu H}$$

$$m_C = 0.55 \times \frac{A}{\mu s}$$

For other output voltages, the inductance can be calculated based on the internal slope compensation requirement and equal to:

$$L = \frac{0.75 \times V_{OUT}}{m_C} = \left(1.36 \times V_{OUT}\right)\left(\mu H\right)$$

Manufacturer specifications list both the inductor DC current rating, which is dependent on the thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions.

The saturation current is a very important parameter for inductor selection. It must be more than the sum of DC current and maximum peak current through the inductor, and the adequate margin is important for safe application. The maximum peak current is given by the equation below.

$$I_{PEAK\_INDUCTOR\_MAX} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{L \times f}$$

where L is the inductance, and f is the operation frequency.

Some inductors that meet the peak and average current ratings requirements still result in excessive losses due to a high Direct Current Resistance (DCR). Always consider the losses associated with the DCR and their effect on the total regulator efficiency when selecting an inductor.

Table 6 shows the recommended inductors for different output voltages.

Table 6. Inductor Selection for Different Output Voltages (1 of 2)

Vout (V)	Inductance (µH)	Part Number	Saturation Current (A)	DCR (mΩ)	Dimensions L×W×H (mm)	Manufacturer
1.5	2.5	CDRH8D38NP-2R5N	5.5	17.5	8.3×8.3×4	Sumida
	2.2	744777002	6.5	20	7.3×7.3×4.5	Wurth Elektronik
		DR73-2R2-R	5.52	16.5	7.9×7.9×3.8	Coil Tronics
3.3	4.7	CDRH105RNP-4R7N	6.4	12.3	10.5×10.3×5.1	Sumida
		CDRH10D68NP-4R7N	6.6	9.8	10.5×10.5×7.1	
		7447715004	6.3	16	12×12×4.5	Wurth Elektronik
5	6.8	CDRH105RNP-6R8N	5.4	18	10.5×10.3×5.1	Sumida
		CDRH124NP-6R8M	4.9	23	12.3×12.3×4.5	
		7447715006	4.7	25	12×12×4.5	Wurth Elektronik
10	15	CDRH127NP-15M	4.5	27	12.3×12.3×8	Sumida
		CDRH127/LDHF-150M	5.65	26.4	12.3×12.3×8	
		744771115	4.55	30	12×12×6	Wurth Elektronik
		DR125-150-R	5.69	29.8	13×13×6.3	Coil Tronics
12	18	CDRH127/LDHF-180M	5.1	28	12.3×12.3×8	Sumida
		744771118	4.3	34	12×12×6	Wurth Elektronik
		DR125-180-R	5.32	37.7	13×13×6.3	Coil Tronics

Table 6. Inductor Selection for Different Output Voltages (2 of 2)

Vout (V)	Inductance (µH)	Part Number	Saturation Current (A)	D.C.R (mΩ)	Dimension(mm) L×W×H	Manufacturer
15	22	CDRH127/LDHF-220M	4.7	36.4	12.3×12.3×8	Sumida
		744770122	5.0	43	12×12×8	Wurth Elektronik
		DR125-220-R	4.71	39.6	13×13×6.3	Coil Tronics
18	27	CDRH127/LDHF-270M	4.2	41.6	12.3×12.3×8	Sumida
		744770127	3.8	46	12×12×8	Wurth Elektronik
		7447709270	5.8	40	12×12×10	
20	27	CDRH127/LDHF-270M	4.2	41.6	12.3×12.3×8	Sumida
		744770127	3.8	46	12×12×8	Wurth Elektronik
		7447709270	5.8	40	12×12×10	

Output Capacitor Selection

The output capacitor impacts stability, limits the output ripple voltage, and maintains the output voltage during large load transitions. The SKY87609 is designed to work with any type of output capacitor since the controller features externally adjustable compensation (see the "Stability Considerations" and "Compensation Component Selection" sections of this Data Sheet).

The key capacitor parameters for selecting the output capacitors are capacitance, Equivalent Series Resistance (ESR), (Effective Series Inductance (ESL) and voltage ratings. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$V_{OUT(\,RIPPLE\,)} = V_{RIPPLE(\,C\,)} + V_{RIPPLE(\,ESR\,)} + V_{RIPPLE(\,ESL\,)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(\,ESR\,)} = \Delta I_L \times ESR$$

$$V_{RIPPLE(\,ESL\,)} = V_{LX} \times \frac{ESL}{L} = V_{IN} \times \frac{ESL}{L}$$

The peak-to-peak inductor current ΔI_L is:

$$\Delta I_L = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \times \frac{V_{OUT}}{V_{IN(MAX)}}}{L \times f_{SW}}$$

The capacitive ripple and ESR ripple are phase shifted from each other, but depending on the type of output capacitor chemistry, one of them typically dominates. When using ceramic capacitors, which generally have low ESR, $V_{RIPPLE(C)}$ dominates. When using electrolytic capacitors, $V_{RIPPLE(ESR)}$ dominates. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

After a load step occurs, the output capacitor must support the difference between the load requirement and inductor current. Once the average inductor current increases to the DC load level, the output voltage recovers. Therefore, based on limitations in the ability to discharge the inductor, a minimum output voltage deviation may be determined by the following:

$$V_{SOAR(C)} = \frac{\Delta I_{OUT}^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

$$V_{SOAR(ESR)} = \Delta I_{OUT} \times ESR$$

where V_{SOAR} is the output voltage overshoot and undershoot deviation. Bandwidth and gain limitations (dependent on output capacitor and compensation component selection) may result in larger output voltage deviations.

The ceramic output capacitor provides low ESR and low ESL, resulting in low output ripple dominated by capacitive ripple voltage ($\Delta V_{OUT(c)}$). However, due to the lower capacitance value, the load transient response is significantly worse. Therefore, ceramic output capacitors are generally recommended only for designs with soft load transients (slow di/dt and/or small load steps).

Tantalum and electrolytic capacitors can provide a high-capacitance, low-cost solution. The bulk capacitance provides minimal output voltage drop/soar after load transients occur.

Input Capacitor Selection

Typically, the input impedance is so low (or other input capacitors are distributed throughout the system) that a single 10 µF, X7R, or X5R ceramic capacitor located near the SKY87609 is sufficient. However, additional input capacitance may be necessary depending on the impedance of the input supply. To estimate the required input capacitance requirement, determine the acceptable input ripple level (VPP) and solve CIN:

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{SW}} = \frac{D \times (1 - D)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{SW}}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when evaluating ceramic bypass capacitors.

In addition to the capacitance requirement, the RMS current rating of the input capacitor must be able to support the pulsed current drawn by the step-down regulator. The input RMS current requirement may be determined by:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The term D × (1 – D) appears in both the input ripple voltage and input capacitor RMS current equations, so the maximum occurs when VOUT = 0.5 × VIN (50% duty cycle). This results in a set of "worst case" capacitance and RMS current design requirements:

$$C_{IN(MIN)} = \frac{1}{4 \times \left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_{SW}}$$

$$I_{RMS(MAX)} = \frac{I_{OUT}}{2}$$

The input capacitor provides a low impedance loop for the pulsed current drawn by the SKY87609. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize the stray inductance, the capacitor should be placed as closely as possible to the high-side MOSFET. This keeps the high-frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor can be seen in the Evaluation Board layout.

In applications where the lead inductance of the input power source cannot be reduced to a level that does not affect the regulator performance, a high-ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL ceramic capacitor. This reduces the input impedance and dampens the high-Q network, stabilizing the input supply.

Setting the Peak Current Limit

The SKY87609 uses the RDS(ON) of the high-side MOSFET to convert the on-time inductor current to a proportional voltage. That voltage is compared with the 500 mV (reference) voltage of the CS comparator. When the voltage drop across the MOSFET exceeds 500 mV (typical), the regulator immediately turns off the high-side MOSFET for the duration of the switching cycle. Calculating the current limit:

$$I_{PCL} = \frac{V_{CLTH}}{R_{DS(ON)}}$$

where VCLTH = 500 mV.

Be sure that the rated peak current of the MOSFET is greater than the set current limit.

N-Channel MOSFET(s) Selection

High-Side Switching MOSFET

The following key parameters must be met by the selected MOSFET:

- Drain-source voltage, VDS, must be able to withstand the input voltage plus overshoots that may be on the switching node. For a VIN of 12 V, a VDS rating of 25 to 30 V is recommended.
- Drain current, ID, at 25°C must be greater than the calculated switching current:

$$I_D = \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} \times \left(I_{LOAD(MAX)}^2 + \frac{\Delta I^2}{12}\right)}$$

- Gate-source voltage, VGS, must be greater than Vin.

Once the above boundary parameters are defined, the next step in selecting the high-side switching MOSFET is to select the key performance parameters. Efficiency is the performance characteristic that drives the other selections criteria. Based on the target efficiency, the power losses in the converter can be calculated as:

$$I_D = (1 - \eta_{TARGET}) \times (V_{OUT} \times I_{LOAD})$$

For example, if the target efficiency is 90% for a 5 V output and 5 A load, then the power loss in the converter is:

$$(1 - 0.90) \times (5\ V \times 5\ A) = 2.5\ W$$

Typically, 20% of the power loss in the converter is used as the power dissipated in the switching MOSFET.

The following equations can be used to calculate the power losses, PHSFET, in the high-side switching MOSFET.

$$P_{HSFET} = P_{HSFET(CON)} + P_{HSFET(SW)} + P_{HSFET(GATE)}$$

$$P_{HSFET(CON)} = \frac{V_{OUT}}{V_{IN}} \times \left(I_{LOAD}^2 + \frac{\Delta I^2}{12}\right)$$

$$P_{HSFET(SW)} = V_{IN} \times f_{SW} \times \left[\frac{\left(I_{LOAD}^2 + \frac{\Delta I^2}{12} \right) \times \left(Q_{GS1} + Q_{GD} \right)}{I_G} + \frac{Q_{OSS(\,HSFET\,)} + Q_{OSS(\,LSFET\,)}}{2} \right]$$

$$P_{HSFET(GATE)} = Q_{G(TOT)} \times V_G \times f_{SW}$$

where:

PHSFET(CON) = conduction losses
PHSFET(SW) = switching losses
PHSFET(GATE) = gate drive losses
QGD = drain-source charge or Miller charge
QGS1 = gate-source post threshold charge
IG = gate drive current
QOSS(HSFET) = high-side switching MOSFET output charge
QOSS(LSFET) = low-side synchronous MOSFET output charge
QG(TOT) = total gate charge from 0 V to gate voltage
VG = gate voltage

It is not always possible to get a MOSFET that meets both of these criteria, so a compromise may have to be made. Also, by selecting different MOSFETs close to this criteria and calculating power losses, the final selection can be made.

Low-Side synchronous MOSFET

Similar criteria can be used for the rectifier MOSFET, with one significant difference. The body diode is conducting, so the rectifier MOSFET switches with near zero voltage across its drain and source, and the switching losses are near zero. However, there are some losses in the body diode. These are minimized by reducing the delay time between the transition from the switching MOSFET turn-off to rectifier MOSFET turn-on and vice versa.

The following equations can be used to calculate the power loss, PLSFET, in the low-side synchronous MOSFET:

$$P_{LSFET} = P_{LSFET(CON)} + P_{LSFET(DIODE)} + P_{HSFET(GATE)}$$

$$P_{LSFET(CON)} = R_{DS(\,ON\,)} \times \frac{V_{OUT}}{V_{IN}} \times \left(I_{LOAD}^2 + \frac{\Delta I^2}{12} \right)$$

$$P_{LSFET(DIODE)} = V_F \times I_{LOAD} \times \left(t1 + t2 \right) \times f_{SW}$$

$$P_{LSFET(GATE)} = Q_{G(TOT)} \times V_G \times f_{SW}$$

where,

PLSFET(DIODE) = body diode losses
t1 = body diode conduction prior to the turn on of channel
t2 = body diode conduction after the turn off of channel
VF = body diode forward voltage

Rectifying Schottky Diode Selection

Power dissipation is the limiting factor when choosing a diode. The worst-case average power can be calculated as follows:

$$P_{DIODE} = \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right) \times I_{OUT(\,MAX\,)} \times V_{DIODE}$$

where VDIODE is the voltage drop across the diode at the given output current IOUT(MAX). (Typical values are 0.7 V for a silicon diode and 0.3 V for a Schottky diode.) Ensure that the selected diode is able to dissipate that much power. For reliable operation over the input voltage range, also ensure that the reverse repetitive maximum voltage is greater than the maximum input voltage (VRRM ≥ VIN(MAX)). The diode's forward current specification must meet or exceed the maximum output current (i.e., IFAX ≥ IOUT(MAX)).

Stability Considerations

The SKY87609 uses a current-mode architecture that relies on the output capacitor and a series resistor-capacitor network on the COMP pin for stability. COMP is the output of the transconductance error amplifier, so the RC network creates a pole-zero pair used to control the gain and bandwidth of the control loop.

The DC loop gain (ADC) is set by the voltage gain of the internal transconductance amplifier (AEA = gm(EA) × ROUT = 500 V/V), the compensation gain (ACC = 400 mV/V), and the current-sense gain (ACS = 1 V/V):

$$A_{DC} = \frac{V_{FB}}{V_{OUT}} \times \frac{A_{CC}}{A_{CS} \times R_{DS(\,ON\,)}} \times A_{EA} \times R_{LOAD}$$

where VFB is the 0.9 V feedback voltage, VOUT is the output voltage determined by the feedback resistors, RDS(ON) is the on-resistance of the high-side N-channel MOSFET, and RLOAD is the output load resistance (RLOAD = VOUT /IOUT). Since the output impedance is a function of the load current and output voltage, the equation may be rewritten independent of the VOUT term:

$$A_{DC} = \frac{V_{FB}}{I_{OUT}} \times \frac{A_{CC}}{A_{CS} \times R_{DS(\,ON\,)}} \times A_{EA}$$

Additionally, the high-side on-resistance RDS(ON) is inversely proportional to the maximum output current (IOUT) due to the peak current limit. This effectively limits the typical value of ADC to a value of 360 V/V (51 dB).

The control loop has two dominant poles: one created by the output capacitor (COUT) and load resistance, and the other formed by the total compensation capacitance (CCC1 + CCC2) and the error amplifier transconductance (gm(EA) = 500 µA/V):

$$f_{P1} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}}$$

$$f_{P2} = \frac{gm_{(EA)}}{2\pi \times A_{EA} \times (C_{CC1} + C_{CC2})}$$

However, the system also has two zeros in the control loop: one created by the series compensation resistor (RCOMP) and capacitor (CCC1), and the other formed by the output capacitor and its parasitic series resistance (ESR):

$$f_{Z1} = \frac{1}{2\pi \times R_{COMP} \times C_{CC1}}$$

$$f_{Z2} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

The ESR zero is highly dependent on the type of output capacitors being used (ceramic vs tantalum), and may not occur before crossover. If the ESR zero occurs low enough, the compensation zero formed by RCOMP may be placed at crossover to avoid stability problems.

However, if both zeros are required below crossover, a third pole is needed to maintain stability. This third pole can be added by including another compensation capacitor (CCC2 in Figure 38) in parallel with the main series RC network:

$$f_{P3} = \frac{1}{2\pi \times R_{COMP} \times \left(\frac{C_{CC1} \times C_{CC2}}{C_{CC1} + C_{CC2}} \right)}$$

If CCC2 << CCC1, the third pole is simplified to:

$$f_{P3} = \frac{1}{2\pi \times R_{COMP} \times C_{CC2}}$$

To safely avoid the Nyquist pole (half the switching frequency), the crossover frequency should occur between 1/20th and 1/5th of the switching frequency. Lower crossover frequencies result in slower transient response speed, while higher crossover frequencies could result in instability.

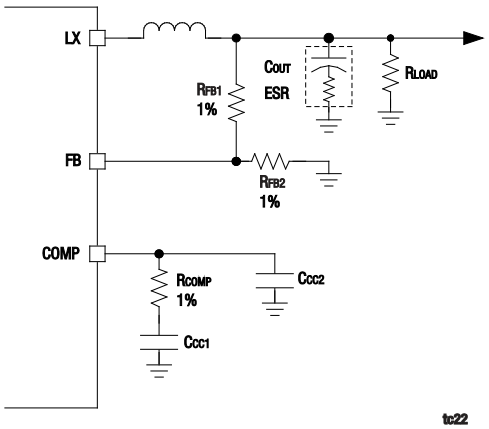

Figure 38. Compensation Components

Compensation Component Selection

This is peak current mode control. An R-C series network (or type II) compensation is applied at the transconductance amplifier output (COMP).

- ROUT(EA) is the output impedance of the transconductance error amplifier.
- N is the scaling factor of output current, Isen = IOUT/N, N = 1 in this case.
  - RSEN is the high-side current sensing resistor, RSEN = RDS(HS) in this case.

There is already a 90 °C phase shift at very low frequency, ωP1. Compensating the 2nd pole ωP2 with 1st zero ωZ1, the unity gain frequency can be simplified as:

$$f_T = \frac{V_{REF} \times (gm \times R_{COMP})}{2\pi \times V_{OUT} \times C_{OUT} \times R_{SEN}}$$

Set the unity gain frequency far away from the switching frequency to avoid any switching noise in the voltage loop, fT = fSW/20.

$$R_{COMP} = 2\pi \times f_T \times \frac{V_{OUT} \times C_{OUT} \times R_{SEN}}{V_{REF} \times gm}$$

$$C_{CC1} = \frac{C_{OUT} \times R_{LOAD(MIN)}}{R_{COMP}}$$

The ESR zero ωZ2 is used to cancel the high frequency pole ωP3.

$$C_{CC2} = \frac{C_{OUT} \times R_{ESR}}{R_{COMP}}$$

where gm = 570 µA/V, gm × ROUT(EA) = 150 V/V, RSEN =100 mΩ, COUT = 22 µF, and RESR =10 mΩ.

For VOUT = 3.3 V: RCOMP = 2 kΩ, CCC1= 10 nF, and CCC2 = 100 pF.

For VOUT = 5 V: RCOMP = 3 kΩ, CCC1= 10 nF, and CCC2 = 56 pF.

For VOUT = 15 V: RCOMP = 9.1 kΩ, CCC1= 10 nF, and CCC2 = 22 pF.

Table 7 gives the recommended compensation value for different output voltages.

Table 7. The Recommended Compensation Value for Different Output Voltages

Vout (V)	Rcomp (kΩ)	Ccc1 (nF)	Ccc2 (pF)
1.5	1.5	10	100
3.3	2	10	100
5	3	10	56
10	6.2	10	33
12	7.5	10	33
15	9.1	10	22
18	10	10	22
20	12	10	22

The type of output capacitor determines how the compensation components should be selected. With large tantalum and electrolytic capacitors, the output capacitor pole dominates the control loop design. Alternatively, small low-ESR ceramic capacitors rely on the compensation capacitor to generate the dominant pole.

Bootstrap Capacitor Selection

To fully turn on the high side N-channel MOSFET, a bootstrap capacitor is connected between the BST pin and the LX pin. During the off time, the switching node is pulled to ground and the bootstrap capacitor charges up to approximately 5 V through an internal diode (see the Functional Block Diagram in Figure 36). The bootstrap capacitor should be a 22 nF to 200 nF ceramic capacitor with a 10 V or greater voltage rating.

Thermal Calculations

There are three types of losses associated with the SKY87609 step-down converter: switching losses, conduction losses, and quiescent current losses. The conduction losses are associated with the $R_{DS(ON)}$ characteristics of the internal high-side MOSFET. The switching losses are dominated by the gate charge and parasitic capacitance of the high-side MOSFET. Under full load conditions, the total power loss within the SKY87609 may be estimated by:

$$P_{TOTAL} = \left(\frac{I_{OUT}^2 \times R_{DS(ON)H} \times V_{OUT}}{V_{IN}} \right) + \left(t_{SW} \times f_S \times I_{OUT} + I_Q \right) \times V_{IN}$$

where I_Q is the step-down converter quiescent current, and t_{SW} is the turn-on/off time of the MOSFET used to estimate the full load step-down converter switching losses. Since the on-time, quiescent current, and switching losses all vary with input voltage, the total power losses within the SKY87609 should be investigated over the complete input voltage range.

The maximum junction temperature can be derived from the θ_{JA} for the 12-pin TSOPJW package, which is 140 °C/W.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA} + T_A$$

Layout Considerations

The following guidelines should be used to help ensure a proper layout:

1. The input capacitor should connect as closely as possible to the drain of the high-side N-channel MOSFET and the anode of the Schottky diode (and/or source of the low-side N-channel MOSFET). Keeping this loop compact reduces the switching noise.
2. COUT and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible and made at the source of the high-side N-channel MOSFET for current-sense accuracy.
3. The feedback trace or FB pin should be separated from any power trace and connected as closely as possible to the load point. Sensing along a high-current load trace degrades DC load regulation.
4. The resistance of the trace from the load return to PGND should be kept to a minimum. This helps minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. Connect PGND to the exposed pad to enhance thermal impedance.

Evaluation Board Description

The SKY87609 Evaluation Board schematic diagram is provided in Figure 39. The PCB layer details are shown in Figure 40. Component values for the SKY87609 Evaluation Board are listed in Table 8.

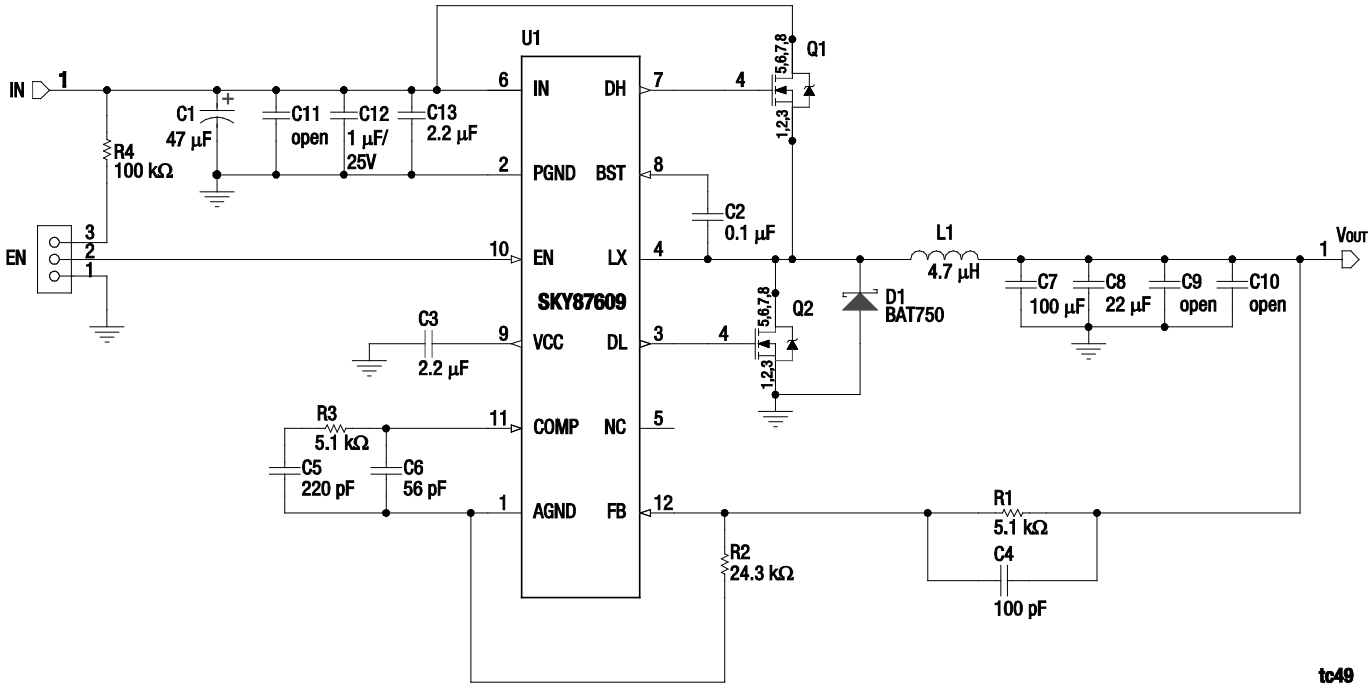

Figure 39: SKY87609 Evaluation Board Schematic

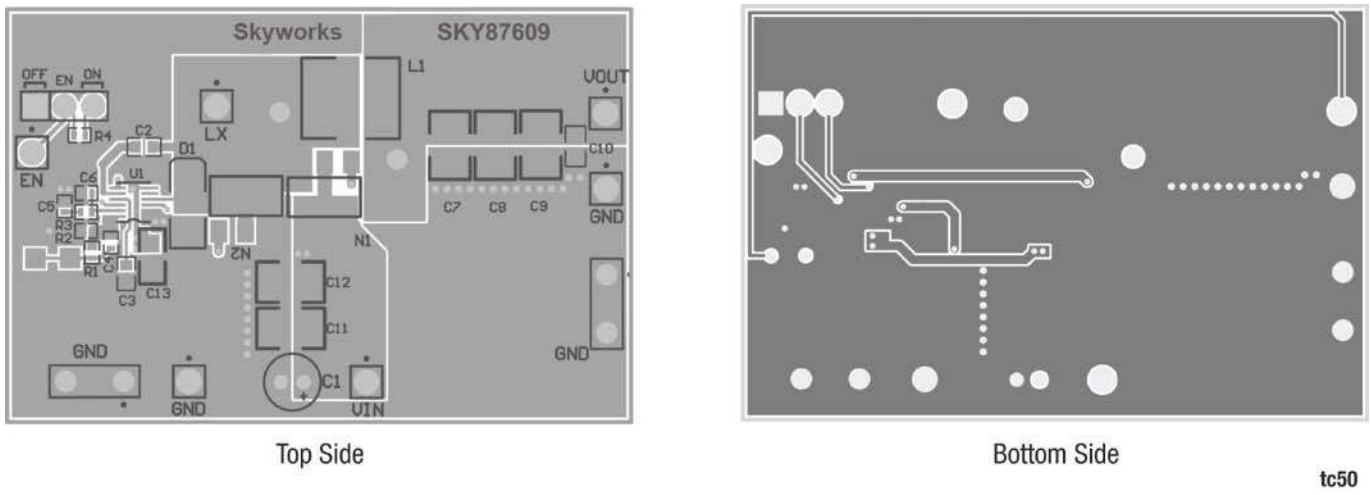

Figure 40: SKY87609 Evaluation Board Layer Details

Table 8. SKY87609 Standard Application Circuit Bill of Materials (BOM)

Component	Part Number	Description	Manufacturer
U1	SKY87609ITP-T1	SKY87609ITP-T1	Skyworks
L1	744 7798 151	INDUCTOR POWER, 15 μH, 4.9 A, SMD	Wurth Electronics
C1	ECA-1HHG330	CAP ALUM, 33 μF, 50 V, 20% RADIAL	Panasonic
C2	GRM188R71C104KA01D	CAP CER, 0.1 μF, 16 V, 10% X7R	Murata
C3	GRM188R61C225KE15D	CAP CER, 2.2 μF, 16 V, 10% X5R	Murata
C5	GRM155R71C103KA01D	CAP CER, 10000 pF 16 V, 10% X7R	Murata
C6	GRM1555C1H560JA01D	CAP CER, 56 pF, 50 V, 5% NP0	Murata
C7, C8, C11, C12	GMK325AB710y6MM-T	CAP CER, 56 pF, 50 V, 5% NP0	Taiyo Yuden
C13	UMK316BJ225KD-T	CAP CER, 2.2 μF, 50 V, 10% X5R	Taiyo Yuden
R1	CRCW0402301KFKED	RES, 301 kΩ, 1/16 W, 1% 0402	Vishay
R2	CRCW040224K3FKED	RES, 24.3 kΩ, 1/16 W, 1% 0402	Vishay
R3	CRCW04021K50FKTD	RES, 1.50 kΩ, 1/16 W, 1% 0402	Vishay
R4	CRCW040210K0FKED	RES, 10.0 kΩ, 1/16 W 1% 0402	Vishay
N1, N2	FDT457N	MOSFET N-CH, 30 V, 5 A, SOT-223	Fairchild Semiconductor
EN	22-28-4360	CONN HEADER, 36POS .100 VERT TIN	Molex
EN	SSC02SYAN	CONN JUMPER SHORTING GOLD	Sullins Connector Solutions
GND, Vin, Vout, GND, LX, EN	6821-0-00-01-00-00-08-0	Test Point - Mill-Max	BISCO
GND, GND		Buswire, 20 AWG	

Package Information

Package dimensions are shown in Figure 41, and tape and reel dimensions are shown in Figure 42.

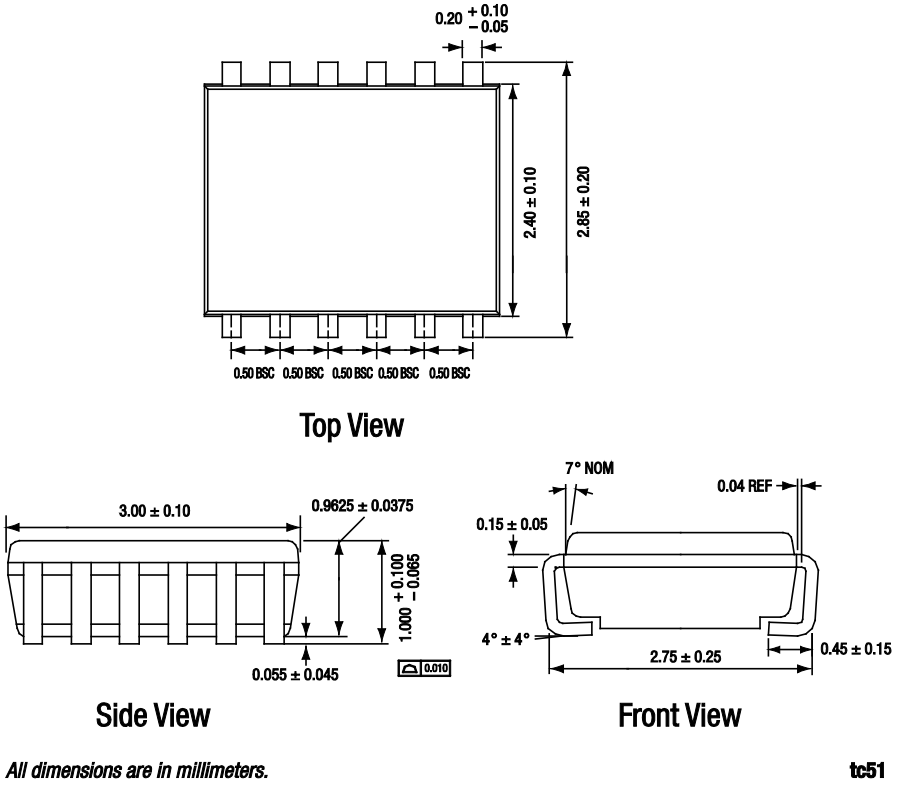

Figure 41. SKY87609 12-pin TSOPJW Package Dimensions

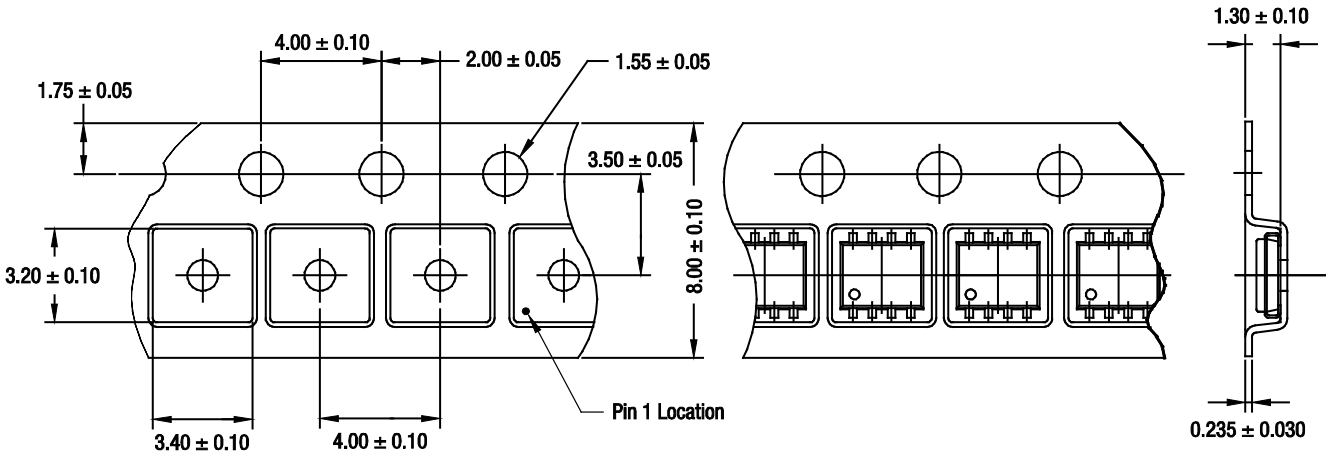

Figure 42. SKY87609 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number (Note 1)	Evaluation Board Part Number
SKY87609 Step-Down DC-DC Controller with Optional Synchronous MOSFET Driver	SKY87609ITP-T1	SKY87609ITP-EVB

Note 1: Sample stock is generally held on the part number listed in BOLD.