MN34041 Sensor NanoVesta Head Board

User's Guide

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Introduction

The MN34041 Sensor NanoVesta Head Board comprises a compact, low cost, high dynamic range (HDR) image sensor, lens and lens housing with adjustable focus, that can bolt directly onto the Lattice HDR-60 Base Board. Both the NanoVesta and HDR-60 boards have been designed to work together as part of the Lattice HDR-60 Video Camera Development Kit. The MN34041 Sensor NanoVesta Head Board is designed to use the Panasonic MN34041PL 1/3-inch CMOS Digital Image Sensor which features:

- HD video (1092p60), 2.1 megapixels
- Full HD resolution at 12 bits and 60fps
- Full scan resolution at 10 bits and 120fps
- High sensitivity (1,580 G/LSB typical)
- LGA ceramic package

You can read more about the specifications for the image sensor in the Panasonic MN34041PL data sheet.

Important: This document (including the schematics in Appendix A) describes the MN34041 Sensor NanoVesta Head Board marked as MN34041 SENSOR BRD Rev A. This marking can be seen on the top layer silkscreen of the printed circuit board, below the outside perimeter of the lens holder.

Features

Key features of the MN34041 Sensor NanoVesta Head Board include:

- Panasonic MN34041 1/3-inch CMOS Digital Image Sensor
- Lens: F/1.59, <7% distortion, with minimized flare, halo and ghosting
- Lens holder with adjustable focus
- Serial signal connections to the HDR-60 Base Board
- Selectable on-board 27.000 MHz MEMs oscillator or HDR-60 Base Board oscillator
- 3.3V, AVDD, 1.8V and 1.2V voltages are generated from the HDR-60 Base Board 5V
- Power status LEDs with one user-defined LED

General Description

The MN34041 Sensor NanoVesta Head Board has been designed for use on the HDR-60 Base Board as part of the HDR-60 Video Camera Development Kit. The MN34041 Sensor NanoVesta Head Board contains the camera sensor portion of the kit, while the HDR-60 Base Board contains the follow-on video camera image processing system. See the HDR-60 Base Board User's Guide for more information concerning that board.

Initial Setup and Handling

The following is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: The devices on the boards can be damaged by improper handling.

The devices on the evaluation boards contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the "Human Body Model" specification for an example of ESD characterization requirements). Even so, the devices are static-sensitive to conditions that exceed their designed-in protection. For example: higher static voltages, as well as lower voltages with lower series resistance

or larger capacitance than the respective ESD specifications require can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation boards when they are removed from the static shielding bag. If you will not be using the boards for a while, it is best to put them back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the boards when they are not in use.

When reaching for the boards, it is recommended that you first touch the outside shield portion of the J11 BNC connector on the HDR-60 Base Board. If the MN34041 Sensor NanoVesta Head Board is not installed on the HDR-60 Base Board, then when reaching for the NanoVesta board, it is recommended that you first touch the outside edge pin of D2, D3 or D4 on the NanoVesta board. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: To minimize the possibility of ESD damage, the first and last electrical connection to the board, should be from test equipment chassis ground to the J11 BNC shield GND on the HDR-60 Base Board.

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the J11 BNC shield GND on the HDR-60 Base Board. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged should be the chassis GND connection to the evaluation board GND. If you have a signal source that is floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board while it is not in a static shielding bag, please keep one finger on the J11 BNC shield GND on the HDR-60 Base Board. If carrying the NanoVesta board alone, keep one finger on the outside pin of LED D2, D3 or D4. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back in it.

Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 42mm x 42mm (1.654" x 1.654"). Additional mechanical board dimension information is included on the mechanical drawing shown in Appendix A, Figure 7. On the physical board itself, connectors include pin 1 indictors as either an arrow, or triangle point near pin 1 on the outer layer silk screen. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: <95% without condensation

Functional Description

Figure 1. MN34041 Sensor NanoVesta Head Board

Voltage Regulators

The MN34041 Sensor NanoVesta Head Board power is supplied by the 5V DC power applied at connectors J4 and J5, pins 1, 2, 39 and 40. The on-board linear voltage regulators then provide the necessary supply voltages to power the sensor: 3.3V, AVDD, 1.8V, and 1.2V. LEDs D2, D7, and D8 will light up if their respective powers are active. The regulator output voltages are set as shown in Table 1.

Table 1. MN34041 Sensor NanoVesta Head Board Regulator Voltages

Supply	Voltage Regulator	Resistor Ratio	LED	Comments
5.0V	On HDR-60 Base Board	—	D3	5V arrives at J4 and J5
3.3V	U4	R16/R20	D2	
AVDD	U3	R16/R20	—	
1.8V	U5	R44/R46	D7	
1.2V	U6	R56/R55	D8	

Each of the LT3025 regulators (U2, U3, U4, and U5) are of the linear low dropout voltage type. An external resistor divider network is used to divide down the regulator output and compare it against an internal reference voltage. The regulator adjusts the output voltage by comparing the feedback from the resistor divider network and the internal reference voltage. By doing this, each regulator output voltage remains at a constant voltage value independent of the load it drives. Each regulator output voltage follows this equation:

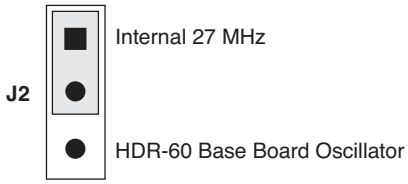
V_{OUT} = (1 + resistor ratio) x (regulator internal reference voltage)

See the LT3025 device data sheet for additional details about this device.

MEMS Oscillator (Y1)

As shown in Figure , J2 is set such that the NanoVesta sensor will receive a clock input signal from the internal 27.000 MHz MEMS oscillator (Y1). The alternate position of J2 down will select the HDR-60 Base Board oscillator for the NanoVesta sensor clock input.

Figure 2. MN34041 Sensor NanoVesta Head Board Default Jumpers Diagram



Serial Interface Connector (J5)

The Panasonic MN34041 (IC1) serial sub-LVDS video signals are available at connector J5 after the proper sensor initialization discussed in the Panasonic MN34041 data sheet. The serial clock and data signals are differential signal pairs with 'P' and 'N' polarities. The receiving LatticeECP3 device should be set to LVDS, 100 ohm differential termination. The other signals on J5 are single-ended LVCMOS type. The pinout of the Panasonic MN34041 device, J5 Interface connector, and LatticeECP3 on the HDR-60 Base Board are shown in Table 2.

Table 2. Sensor (U1) Interface to HiSPi Connector J5

MN34041 Sensor NanoVesta Head Board				HDR-60 Base Board	
J5 Pin	I/O Pin	Signal	Polarity	LatticeECP3 I/O Pin	sysIO Bank
18	K11	MN34041_SDOCAP	P	M21	2
16	L11	MN34041_SDOCAM	N	M20	2
13	K12	MN34041_SDODA0P	P	K21	2
11	L12	MN34041_SDODA0N	N	L21	2
29	K9	MN34041_SDODA1P	P	L22	2
27	L9	MN34041_SDODA1N	N	M22	2
21	K8	MN34041_SDODA2P	P	P21	2
19	L8	MN34041_SDODA2N	N	N22	2
26	K4	MN34041_SDOCBP	P	M18	2
24	L4	MN34041_SDOCBM	N	N17	2
22	K3	MN34041_SDODB0P	P	K20	2
20	L3	MN34041_SDODB0N	N	K19	2
17	K6	MN34041_SDODB1P	P	K17	2
15	L6	MN34041_SDODB1N	N	K18	2
25	K7	MN34041_SDODB2P	P	H21	2
23	L7	MN34041_SDODB2N	N	H22	2
4	—	V1P8_rH	—	A13	1
12	—	MN34041_LED	—	L19	2

Interface Connector (J4)

The Panasonic MN34041 (IC1) is controlled by the signals available at connector J4. The pinout of the Panasonic MN34041 device, J4 Interface connector, and LatticeECP3 on the HDR-60 Base Board are shown in Table 3.

Table 3. Sensor (U1) Interface to Parallel Connector J4

MN34041 Sensor NanoVesta Head Board			HDR-60 Base Board	
J5 Pin	I/O Pin	Signal	LatticeECP3 I/O Pin	sysIO Bank
9	F2	MN34041_EXTCLK_FPGA	A19	1
11	B5	MN34041_VD	A18	1
12	A5	MN34041_HD	B16	1
25	C2	MN34041_SO	B18	1
27	C1	MN34041_RESET_BAR	A17	1
29	D2	MN34041_PSV	F16	1
31	E2	MN34041_MSSEL	F15	1
26	A4	MN34041_SCS	G15	1
28	B4	MN34041_SCK	D15	1
30	B3	MN34041_SI	C15	1
32	—	MN34041_OSZ_ENABLE	E15	1
4	—	V1P8_rP	A12	1

References

- MN34041 Sensor NanoVesta Head Board web page
- HDR-60 Video Camera Development Kit web page
- DS1021, LatticeECP3 Family Data Sheet
- HB1009, LatticeECP3 Family Handbook
- EB59, HDR-60 Base Board User's Guide
- QS010, LatticeECP3 Video Camera Development Kit QuickSTART Guide

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
HDR-60 Video Camera Development Kit *(Contains: HDR-60 Base Board with LatticeECP3 FPGA pre-loaded with Image Signal Processing (ISP) Demo, NanoVesta Head Board with Aptina A-1000 720p HDR Sensor and Sunex lens, two USB cables, HDMI cable with HDMI-to-DVI adapter, 12V AC adapter power supply, QuickSTART Guide)*	LFE3-70EAHDR60-DKN	
MN34041 Sensor NanoVesta Head Board	LF-PNV-EVN	

Technical Support Assistance

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e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
February 2012	01.0	Initial release.

Appendix A. Schematics

Figure 3. MN34041PL - Serial Interface

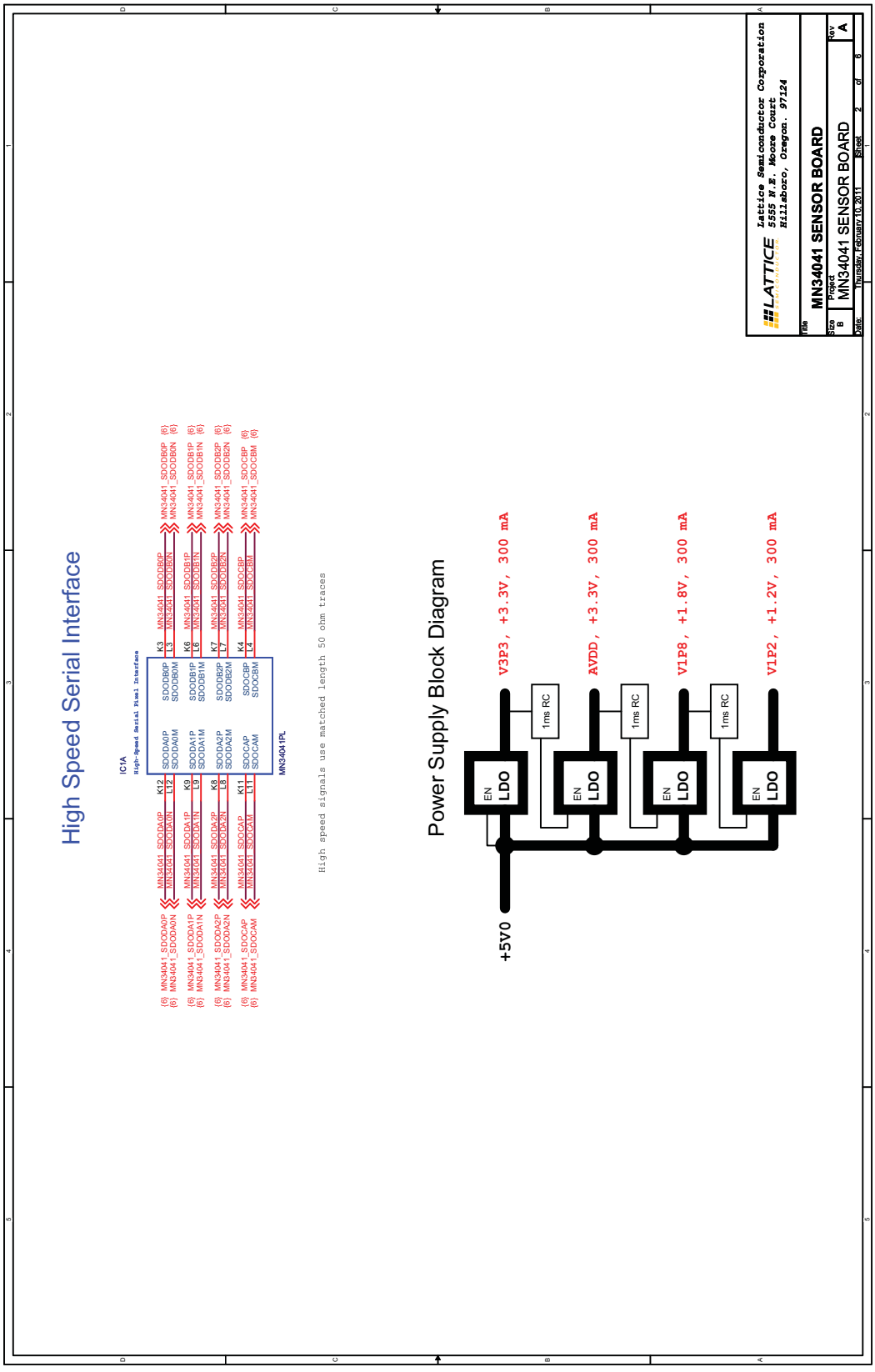


Figure 4. MN34041PL Power

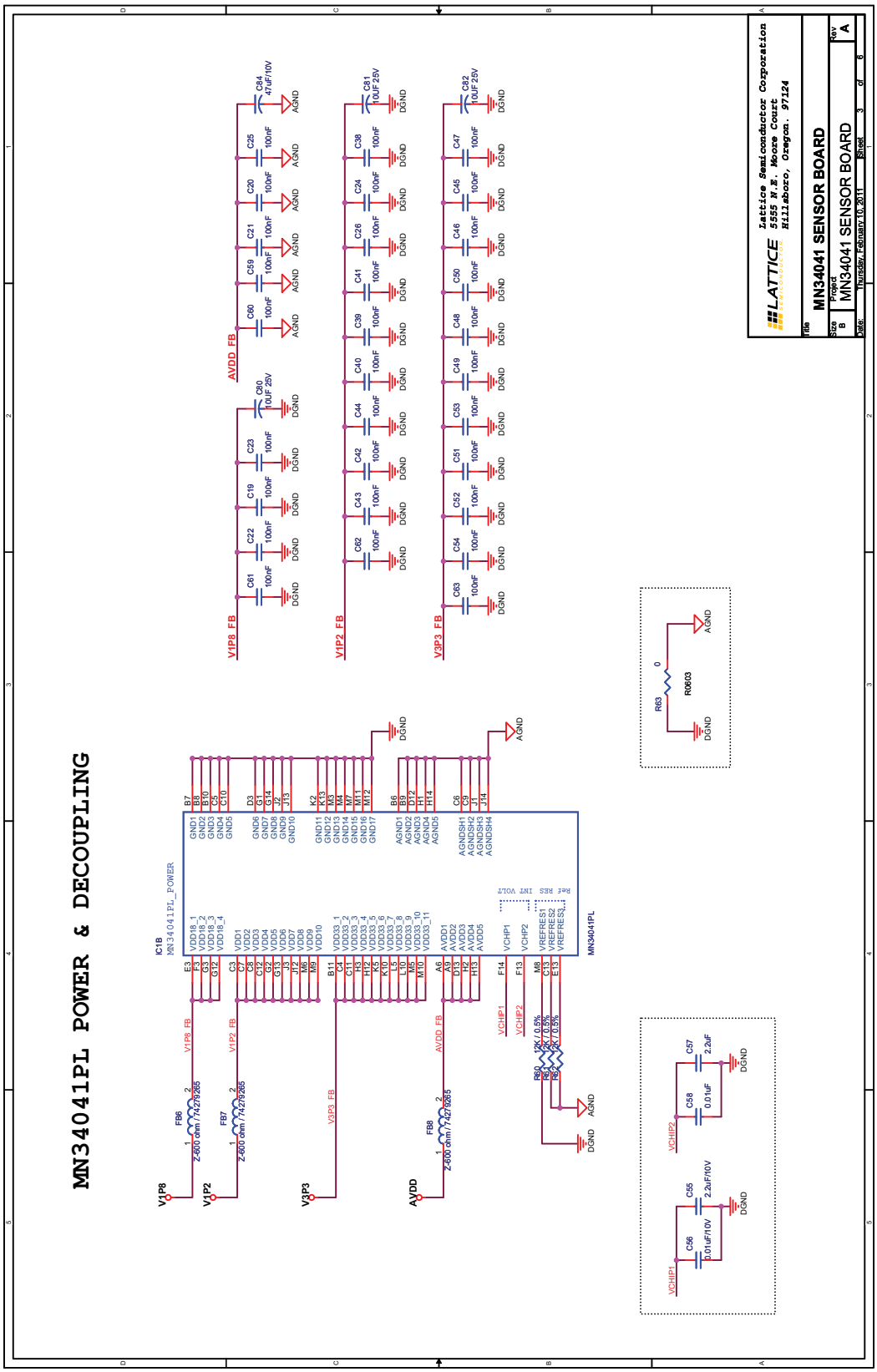


Figure 5. Power Regulators

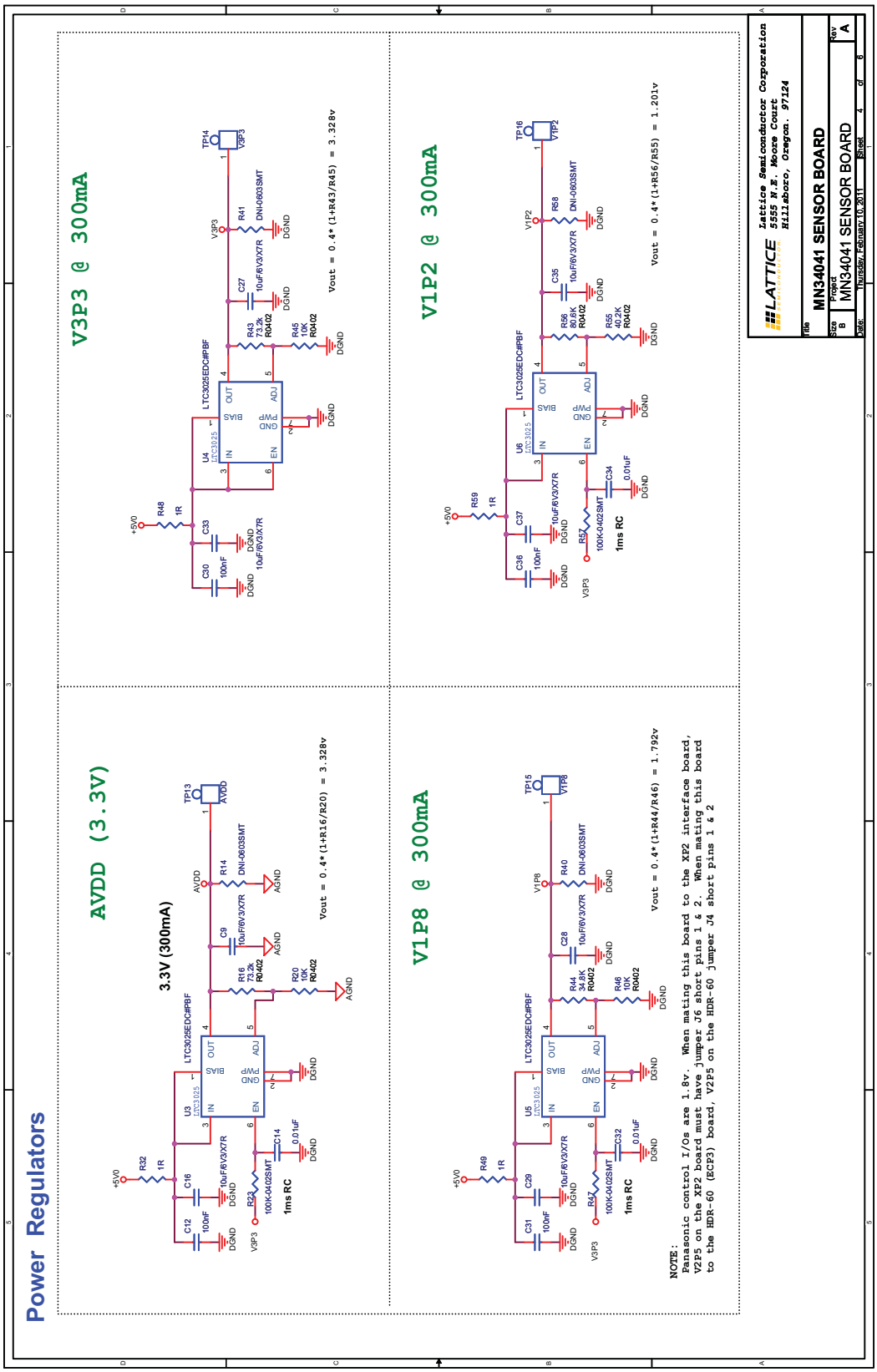


Figure 6. Image Sensor

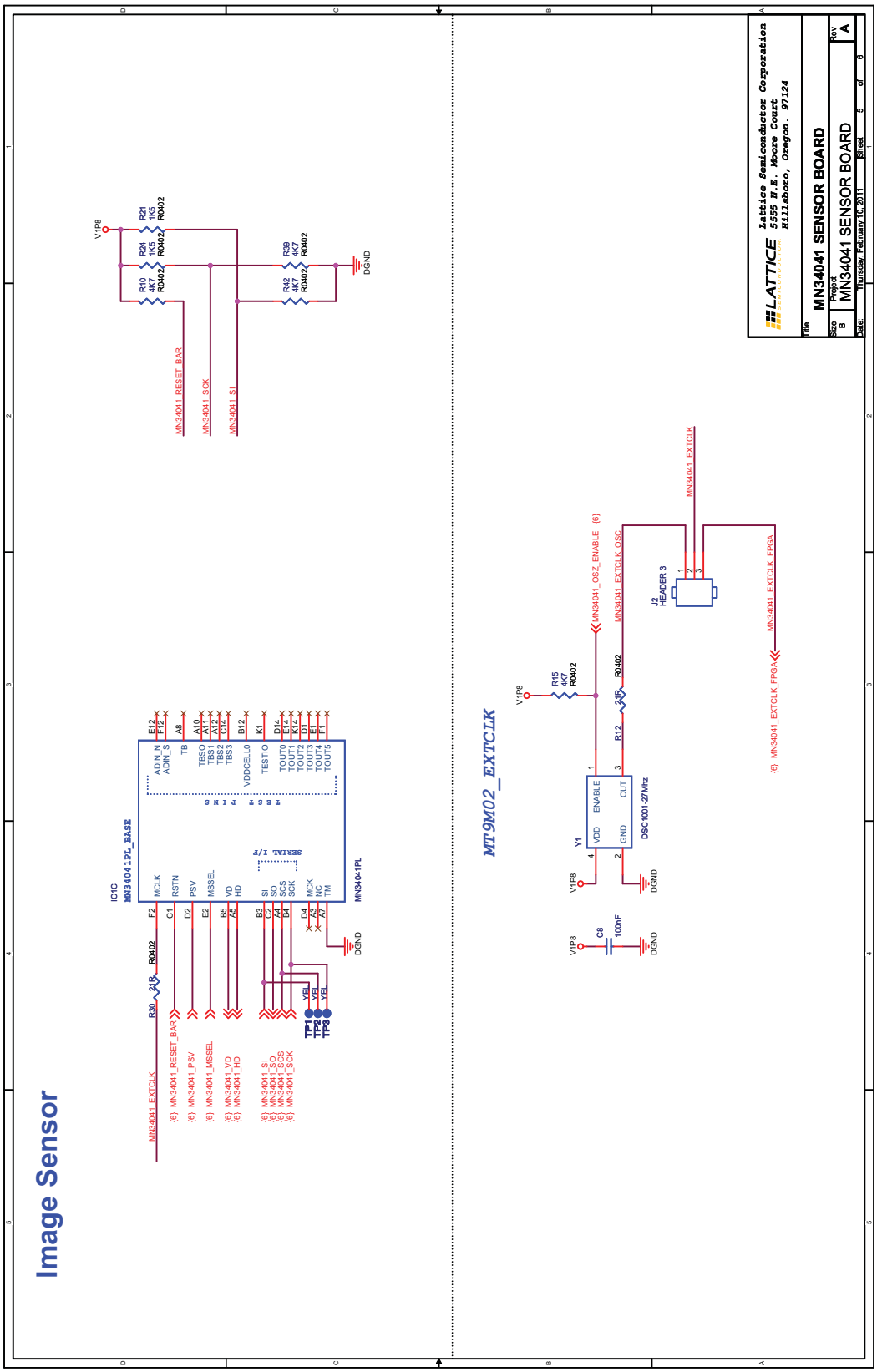
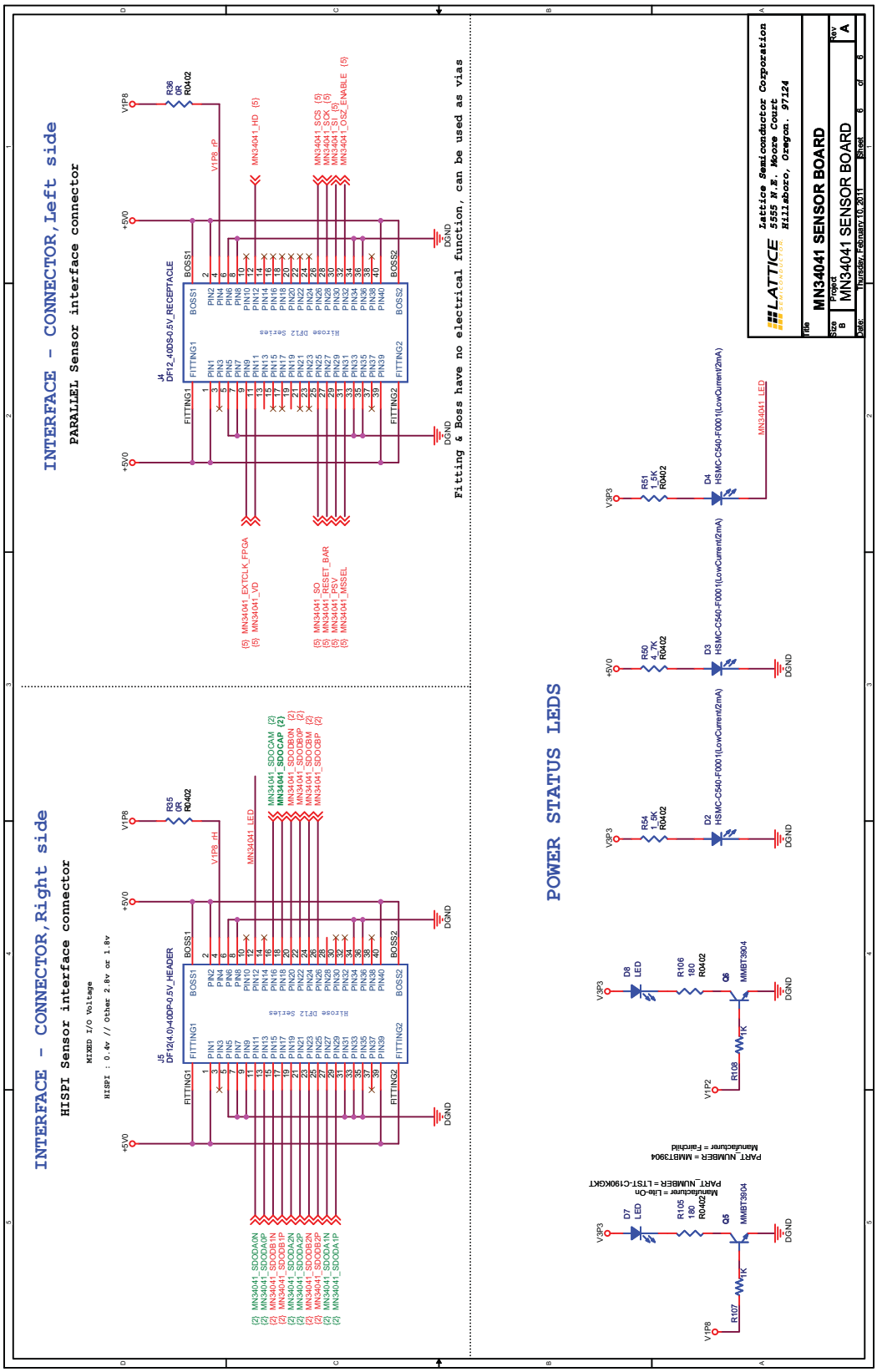


Figure 7. Interface Connectors



Appendix B. Bill of Materials