3.3 V/5 V ECL Differential Receiver/Driver with High and Low Gain

MC100EP16VB

ON Semiconductor®

Description

The EP16VB is a world-class differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices but with both high and low gain outputs. Q_{HG} and $\overline{Q_{HG}}$ outputs have a DC gain several times larger than the DC gain of an EP16. $\overline{Q}$ output is provided for feedback purposes.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Special considerations are required for differential inputs under No Signal conditions to prevent instability.

The 100 Series contains temperature compensation.

Features

- Gain = > 200
- Maximum Frequency = > 3 GHz Typical
- PECL Mode Operating Range:
  $V_{CC} = 3.0$ V to 5.5 V with $V_{EE} = 0$ V
- NECL Mode Operating Range:
  $V_{CC} = 0$ V with $V_{EE} = -3.0$ V to −5.5 V
- V_{BB} Output
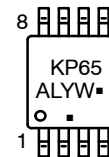- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

TSSOP−8
DT SUFFIX
CASE 948R−02

MARKING DIAGRAM*

```
8 ████
   KP65
   ALYW▪
   o   ▪
1 ████
```

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping
MC100EP16VBDTG	TSSOP−8 (Pb−Free)	100 Units / Tube

MC100EP16VB
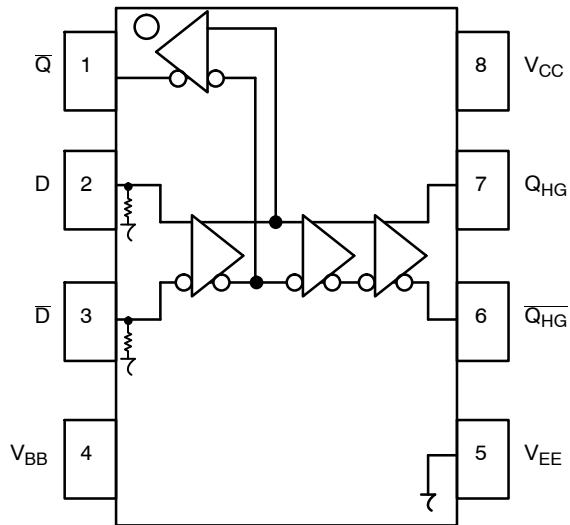
Figure 1. 8-Lead Pinout (Top View)
and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
D*, $\overline{D}$*	ECL Data Inputs
$\overline{Q}$	ECL Data Output
Q_{HG}, $\overline{Q_{HG}}$	ECL High Gain Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

*Pins will default LOW when left open.

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A

ESD Protection
    Human Body Model
    Machine Model
    Charged Device Model
	> 4 kV
	> 200 V
	> 2 kV

Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
TSSOP−8	Level 3
Flammability Rating, Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	167 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			±0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm		185 140	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board		41 to 44	°C/W
T_{sol}	Wave Solder			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 4. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	22	30	38	24	32	40	mA
V_{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 2)	1305	1430	1555	1305	1400	1555	1305	1380	1555	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	2045	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −2.2 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 5. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 5.0 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	22	30	38	24	32	40	mA
V_{OH}	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 2)	3005	3130	3255	3005	3100	3255	3005	3080	3255	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{BB}	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to −0.5 V.
2. All loading with 50 Ω to V_{CC} − 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
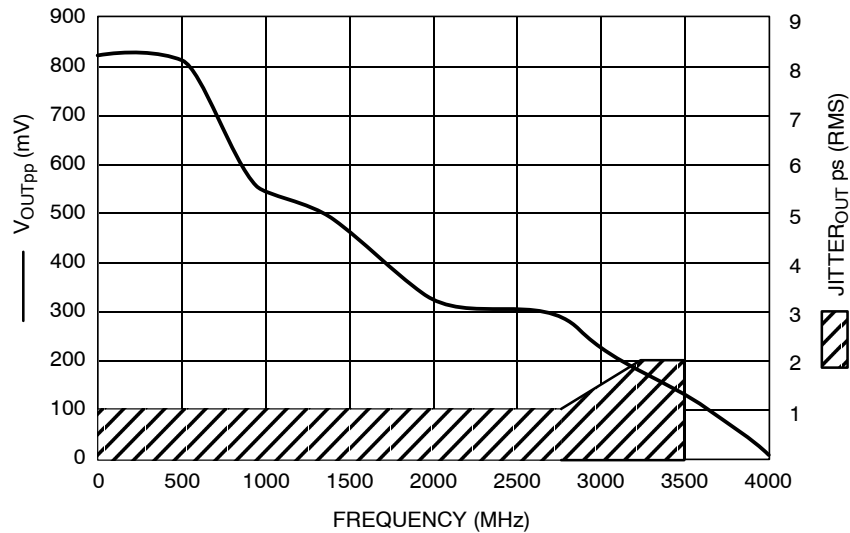
Table 6. 100EP DC CHARACTERISTICS, NECL (V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	27	37	47	22	30	38	24	32	40	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 2)	−1995	−1870	−1745	−1995	−1900	−1745	−1995	−1920	−1745	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{BB}	Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Input and output parameters vary 1:1 with V_{CC}.
2. All loading with 50 Ω to V_{CC} − 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 2)		> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay (Differential) $\overline{Q}$ (Differential) QHG, $\overline{QHG}$ (Single-Ended) $\overline{Q}$ (Single-Ended) QHG, $\overline{QHG}$	200 200 250 250	275 280 325 330	350 350 400 400	250 250 300 300	300 300 350 350	400 400 450 450	275 275 325 325	310 320 360 370	425 425 475 475	ps
t_{SKEW}	Duty Cycle Skew (Note 2)		5.0	20		5.0	20		5.0	20	ps
t_{JITTER}	Cycle-to-Cycle Jitter (Figure 3)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential) HG (Differential) $\overline{Q}$	25 150	800 800	1200 1200	25 150	800 800	1200 1200	25 150	800 800	1200 1200	mV
t_r t_f	Output Rise/Fall Times $\overline{Q}$ (20%−80%) QHG, $\overline{QHG}$	200 70	270 130	400 220	220 80	300 150	420 240	250 100	310 170	450 270	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.
1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

Figure 2. F$_{max}$/Jitter for QHG, $\overline{QHG}$ Output

Figure 3. F_{max}/Jitter for $\overline{Q}$ Output
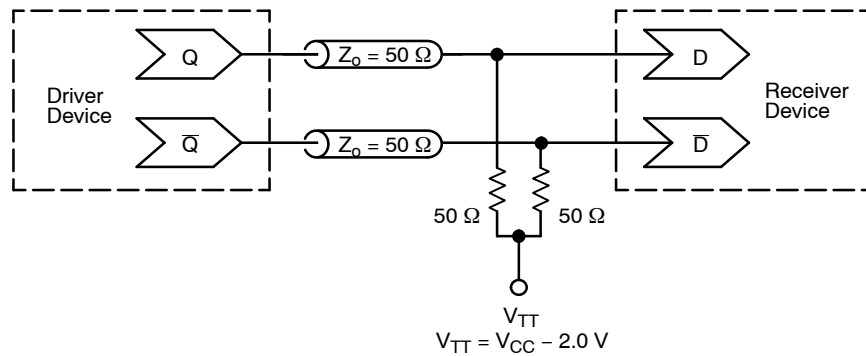
**Figure 4. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices)**

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices
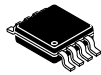
TSSOP 8
CASE 948R−02
ISSUE A

DATE 04/07/2000

SCALE 2:1

8x **K** REF

0.15 (0.006) T U Ⓢ

⊕ 0.10 (0.004) Ⓜ T U Ⓢ V Ⓢ

2X **L**/2

0.25 (0.010)

B

M

−U−

PIN 1 IDENT

0.15 (0.006) T U Ⓢ

A

F

−V−

DETAIL E

L

C

0.10 (0.004)

−T− SEATING PLANE

D

G

−W−

DETAIL E
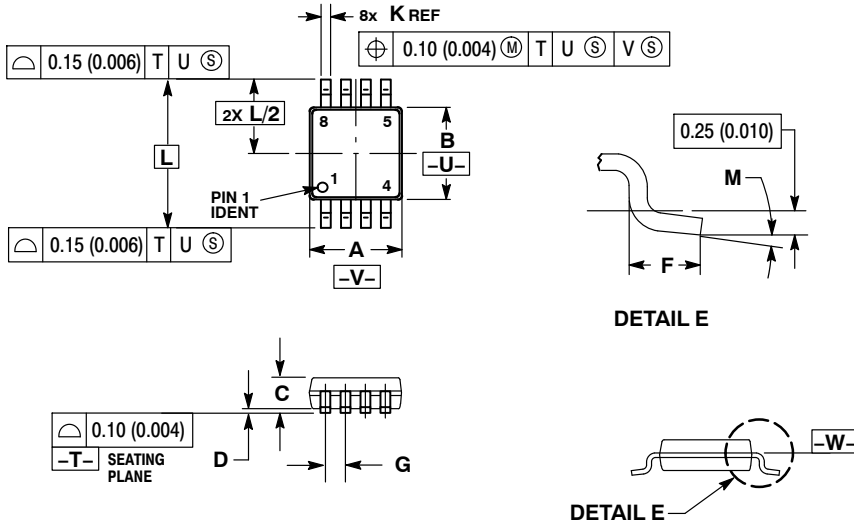
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0 °	6 °	0 °	6 °

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PUBLICATION ORDERING INFORMATION

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