

74AVC16836A

20-bit registered driver with inverted register enable and Dynamic Controlled Outputs; 3-state

Rev. 6 — 24 September 2018

Product data sheet

1. General description

The 74AVC16836A is a 20-bit universal bus driver. Data flow is controlled by output enable (\overline{OE}), latch enable (\overline{LE}) and clock inputs (CP).

This product is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient. See [Fig. 5](#) for typical curves.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce
- Power off disables 74AVC16836A outputs, permitting Live Insertion
- Integrated input diodes to minimize input overshoot and undershoot

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | Version |
| 74AVC16836ADGG | -40 °C to + 85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

4. Functional diagram

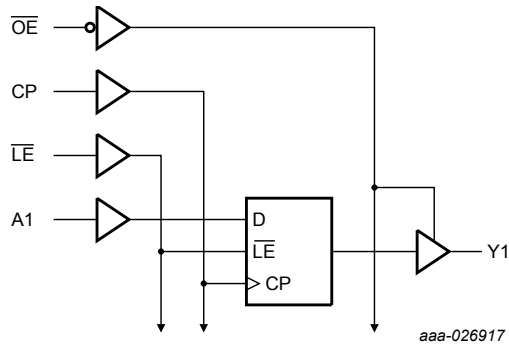


Fig. 1. Logic diagram

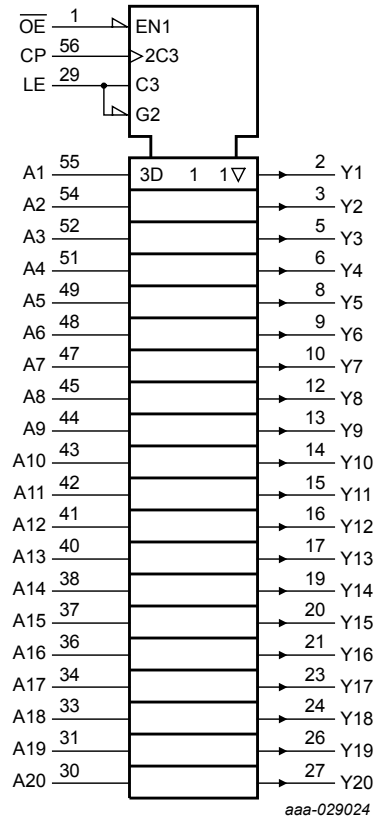


Fig. 2. Logic symbol (IEEE/IEC)

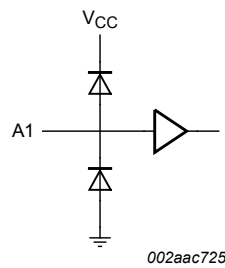


Fig. 3. Typical input (data or control)

5. Pinning information

5.1. Pinning

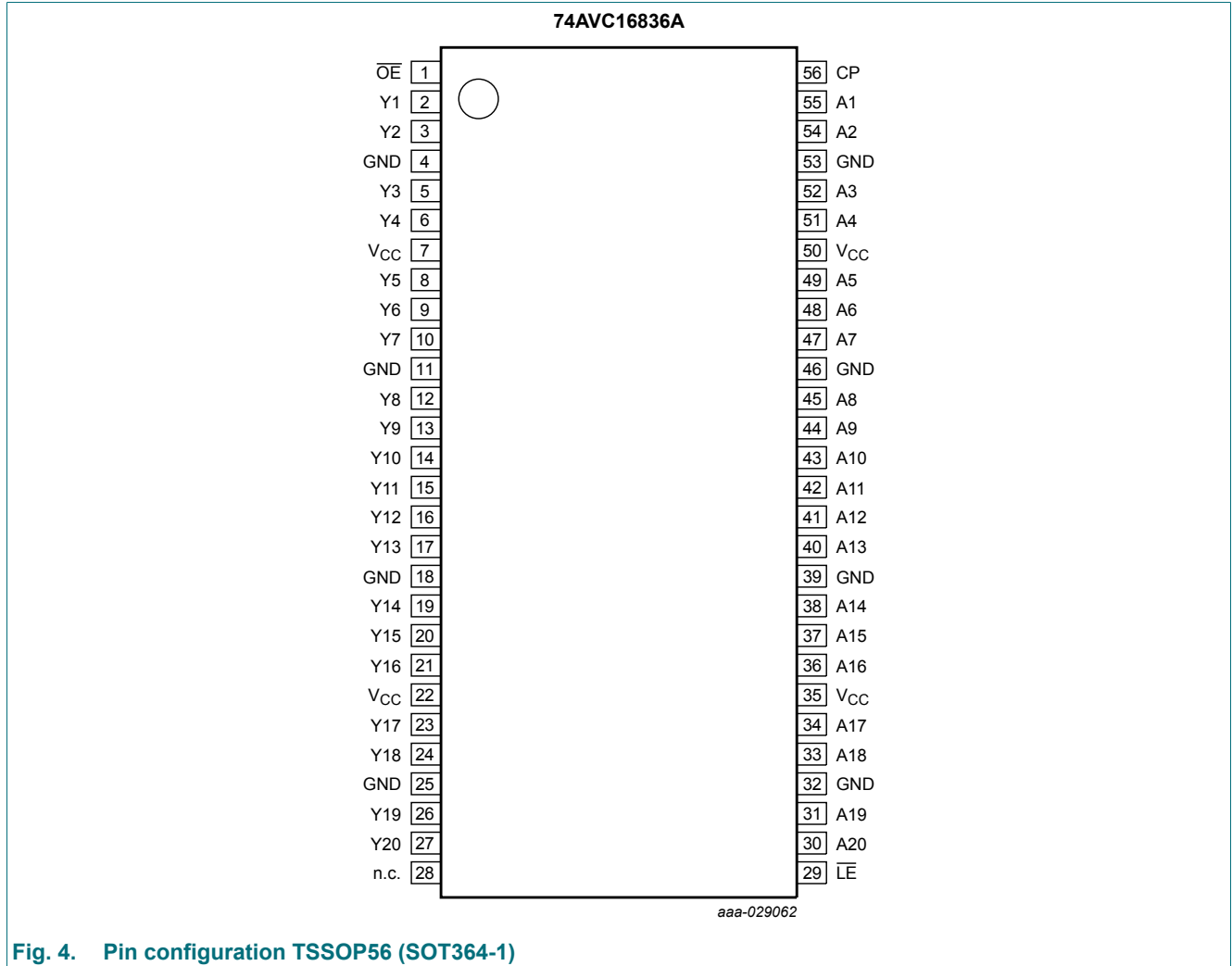


Fig. 4. Pin configuration TSSOP56 (SOT364-1)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|--|--|
| A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20 | 55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | data inputs |
| Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20 | 2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | data outputs |
| n.c. | 28 | not connected |
| $\overline{\text{LE}}$ | 29 | latch enable input (active LOW) |
| $\overline{\text{OE}}$ | 1 | output enable input (active LOW) |
| CP | 56 | clock input (LOW-to-HIGH, edge-triggered) |
| GND | 4, 11, 18, 25, 32, 39, 46, 53 | ground (0 V) |
| V _{CC} | 7, 22, 35, 50 | supply voltage |

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = high-impedance OFF-state; ↑ = LOW to HIGH level transition.

| Inputs | | | | Outputs |
|--------|----|----|----|--------------------|
| OE | LE | CP | An | Yn |
| H | X | X | X | Z |
| L | L | X | L | L |
| L | L | X | H | H |
| L | H | ↑ | L | L |
| L | H | ↑ | H | H |
| L | H | H | X | Y ₀ [1] |
| L | H | L | X | Y ₀ [2] |

[1] Output level before the indicated steady-state input conditions were established, provided that CP is high before $\overline{\text{LE}}$ goes low.

[2] Output level before the indicated steady-state input conditions were established.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|-----------------|-------------------------|--|------|------|-----------------------|---|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V | |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA | |
| V _I | input voltage | [1] | -0.5 | +4.6 | V | |
| I _{OK} | output clamping current | V _O > V _{CC} or V _O < 0 V | - | ±50 | mA | |
| V _O | output voltage | output HIGH or LOW | [1] | -0.5 | V _{CC} + 0.5 | V |
| | | output 3-state | [1] | -0.5 | +4.6 | V |
| I _O | output current | V _O = 0 V to V _{CC} | - | ±50 | mA | |

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| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|------|------|
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C to }+85\text{ °C}$ [2] | - | 600 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|--|------|-----|----------|------|
| V_{CC} | supply voltage | for low-voltage applications | 1.2 | - | 3.6 | V |
| | | according to JEDEC Low Voltage Standards | 1.65 | - | 1.95 | V |
| | | | 2.3 | - | 2.7 | V |
| | | | 3.0 | - | 3.6 | V |
| V_I | input voltage | 0 | - | 3.6 | V | |
| V_O | output voltage | output HIGH or LOW | 0 | - | V_{CC} | V |
| | | output 3-state | 0 | - | 3.6 | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65\text{ V to }2.3\text{ V}$ | 0 | - | 30 | ns/V |
| | | $V_{CC} = 2.3\text{ V to }3.0\text{ V}$ | 0 | - | 20 | ns/V |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 0 | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|----------|--------------------------|---|----------------------|--------|----------------------|------|
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.2\text{ V}$ | V_{CC} | - | - | V |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | 0.9 | - | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | 1.2 | - | V |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 2.0 | 1.5 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.2\text{ V}$ | - | - | GND | V |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | - | 0.9 | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | - | 1.2 | 0.7 | V |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | 1.5 | 0.8 | V |

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| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|------------------|---------------------------|---|------------------------|------------------------|------|------|
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V | V _{CC} - 0.20 | V _{CC} | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | V _{CC} - 0.45 | V _{CC} - 0.10 | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | V _{CC} - 0.55 | V _{CC} - 0.28 | - | V |
| | | I _O = -12 mA; V _{CC} = 3.0 V | V _{CC} - 0.70 | V _{CC} - 0.32 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V | - | GND | 0.20 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | 0.10 | 0.45 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | 0.26 | 0.55 | V |
| | | I _O = 12 mA; V _{CC} = 3.0 V | - | 0.36 | 0.70 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 3.6 V | - | 0.1 | 2.5 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 3.6 V; V _{CC} = 0 V | - | 0.1 | ±10 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND | | | | |
| | | V _{CC} = 1.65 V to 2.7 V | - | 0.1 | 5 | μA |
| | | V _{CC} = 3.0 V to 3.6 V | - | 0.1 | 10 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A | | | | |
| | | V _{CC} = 1.65 V to 2.7 V | - | 0.1 | 20 | μA |
| | | V _{CC} = 3.0 V to 3.6 V | - | 0.2 | 40 | μA |
| C _I | input capacitance | | - | 3.8 | - | pF |

[1] All typical values are measured at T_{amb} = 25 °C.

9.1. Dynamic Controlled Output graphs

A Dynamic Controlled Output (DCO) circuit is designed in. During the transition, it initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Fig. 5 shows V_{OL} vs. I_{OL} and V_{OH} vs. I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DCO circuit provides a maximum dynamic drive that is equivalent to a high drive standard output device.

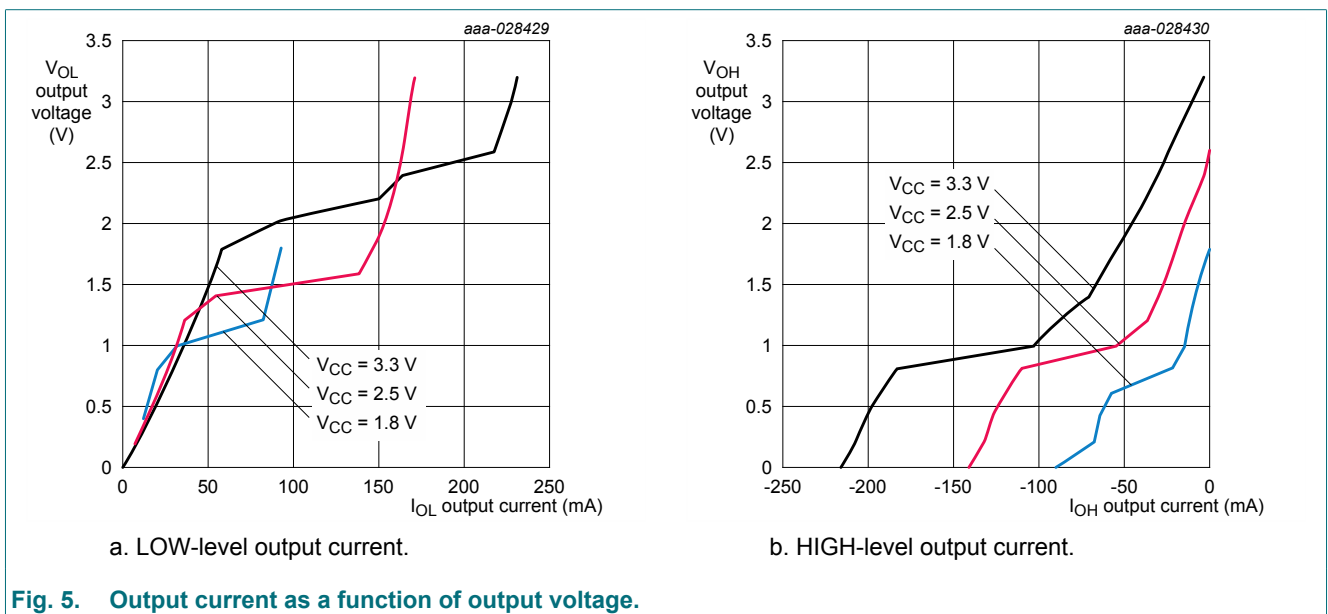


Fig. 5. Output current as a function of output voltage.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 12](#).

| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit |
|---|-------------------|--|-----|---------|-----|------|
| t_{pd} | propagation delay | An to Yn; see Fig. 6 [2] | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 4.7 | - | ns |
| | | $V_{CC} = 1.4\text{ V to }1.6\text{ V}$ | 2.0 | - | 5.3 | ns |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 1.0 | 2.4 | 4.4 | ns |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.8 | 1.7 | 3.2 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 0.7 | 1.5 | 2.7 | ns |
| | | \overline{LE} to Yn; see Fig. 7 [2] | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 5.0 | - | ns |
| | | $V_{CC} = 1.4\text{ V to }1.6\text{ V}$ | 2.0 | - | 5.6 | ns |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 1.5 | 2.7 | 5.0 | ns |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.0 | 2.1 | 3.5 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 0.7 | 1.7 | 3.4 | ns |
| | | CP to Yn; see Fig. 9 [2] | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 5.7 | - | ns |
| | | $V_{CC} = 1.4\text{ V to }1.6\text{ V}$ | 2.0 | - | 4.7 | ns |
| $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 1.2 | 2.3 | 4.1 | ns | | |
| $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.8 | 1.7 | 3.2 | ns | | |
| $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 0.7 | 1.6 | 3.0 | ns | | |
| t_{en} | enable time | \overline{OE} to Yn; see Fig. 11 [2] | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 6.0 | - | ns |
| | | $V_{CC} = 1.4\text{ V to }1.6\text{ V}$ | 2.5 | - | 6.8 | ns |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 1.5 | 3.0 | 5.4 | ns |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.0 | 2.4 | 4.0 | ns |
| $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 1.9 | 3.6 | ns | | |
| t_{dis} | disable time | \overline{OE} to Yn; see Fig. 11 [2] | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 6.6 | - | ns |
| | | $V_{CC} = 1.4\text{ V to }1.6\text{ V}$ | 2.5 | - | 7.6 | ns |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 1.5 | 3.7 | 7.5 | ns |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.0 | 2.1 | 4.7 | ns |
| $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 2.5 | 4.8 | ns | | |
| t_w | pulse width | CP HIGH or LOW; see Fig. 9 . | | | | |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 2.0 | - | - | ns |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.2 | - | - | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | - | - | ns |
| | | \overline{LE} HIGH; see Fig. 7 . | | | | |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 2.0 | - | - | ns |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.2 | - | - | ns |
| $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | - | - | ns | | |

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| Symbol | Parameter | Conditions | Min | Typ [1] | Max | Unit | |
|----------------------------------|-------------------------------|---|-----|---------|-----|------|--|
| t _{su} | set-up time | An to CP; see Fig. 10 | | | | | |
| | | V _{CC} = 1.2 V | - | 0.0 | - | ns | |
| | | V _{CC} = 1.4 V to 1.6 V | 0.3 | - | - | ns | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.2 | 0.0 | - | ns | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.3 | 0.0 | - | ns | |
| | | V _{CC} = 3.0 V to 3.6 V | 0.2 | 0.0 | - | ns | |
| | | An to $\overline{\text{LE}}$; see Fig. 8 | | | | | |
| | | V _{CC} = 1.2 V | - | 1.2 | - | ns | |
| | | V _{CC} = 1.4 V to 1.6 V | 1.3 | - | - | ns | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.9 | 0.4 | - | ns | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.6 | 0.2 | - | ns | |
| V _{CC} = 3.0 V to 3.6 V | 0.3 | 0.0 | - | ns | | | |
| t _h | hold time | An to CP; see Fig. 10 | | | | | |
| | | V _{CC} = 1.2 V | - | 0.1 | - | ns | |
| | | V _{CC} = 1.4 V to 1.6 V | 0.6 | - | - | ns | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.6 | 0.2 | - | ns | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.6 | 0.2 | - | ns | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.2 | 0.5 | - | ns | |
| | | An to $\overline{\text{LE}}$; see Fig. 8 | | | | | |
| | | V _{CC} = 1.2 V | - | -0.7 | - | ns | |
| | | V _{CC} = 1.4 V to 1.6 V | 0.2 | - | - | ns | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.4 | 0.0 | - | ns | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 0.1 | - | ns | |
| V _{CC} = 3.0 V to 3.6 V | 1.0 | 0.5 | - | ns | | | |
| f _{max} | maximum frequency | CP; see Fig. 9 | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 250 | - | - | MHz | |
| | | V _{CC} = 2.3 V to 2.7 V | 400 | - | - | MHz | |
| | | V _{CC} = 3.0 V to 3.6 V | 500 | - | - | MHz | |
| C _{PD} | power dissipation capacitance | per buffer; V _I = GND to V _{CC} [3] | | | | | |
| | | outputs enabled | - | 25 | - | pF | |
| | | outputs disabled | - | 6 | - | pF | |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit

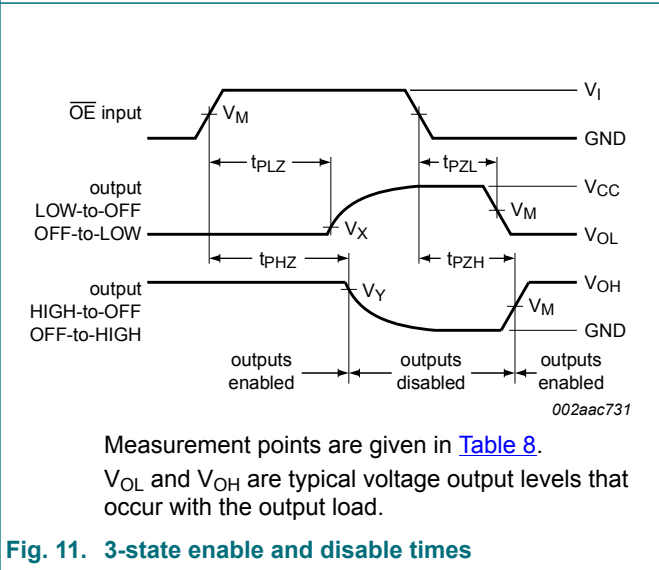
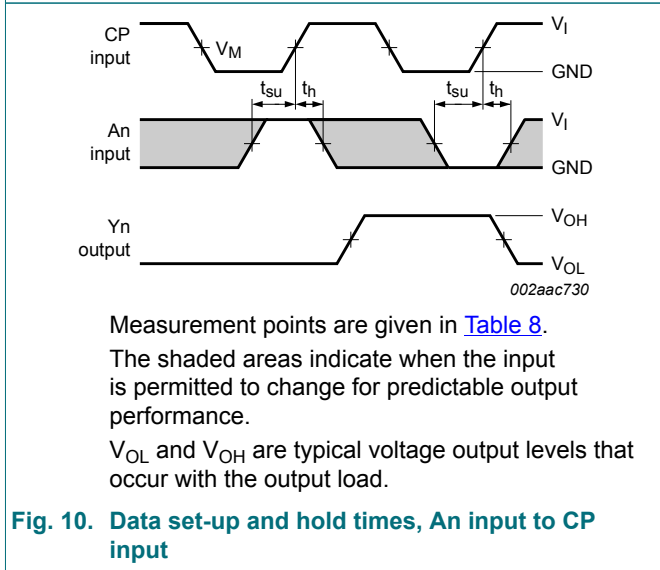
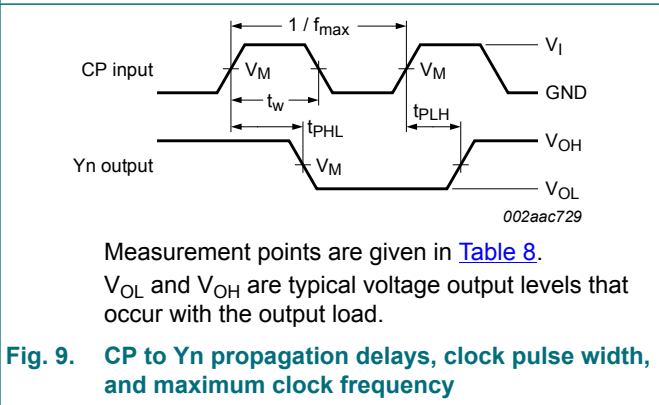
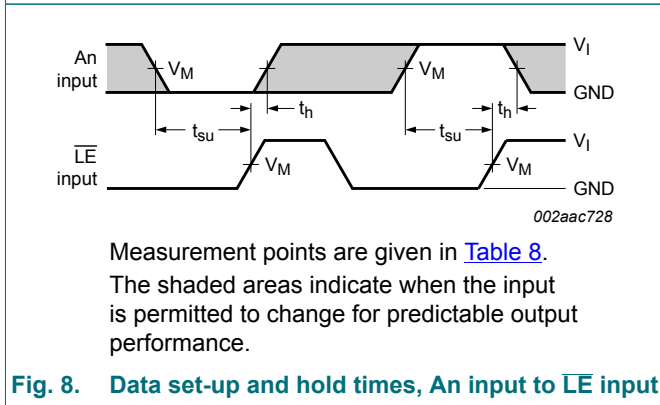
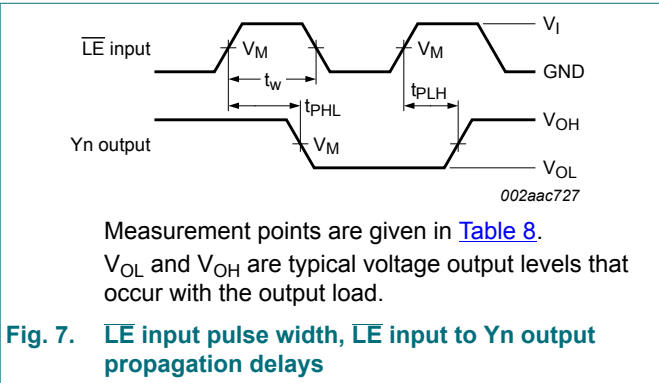
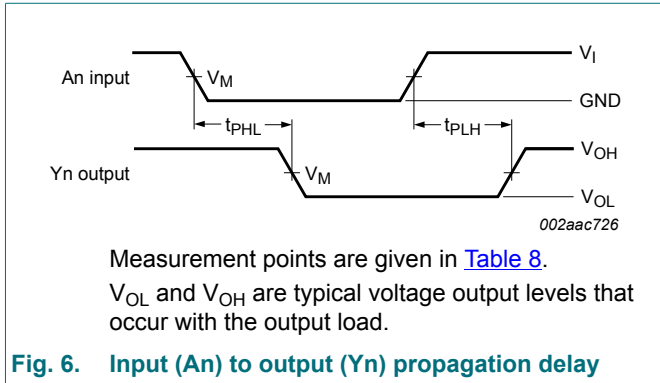
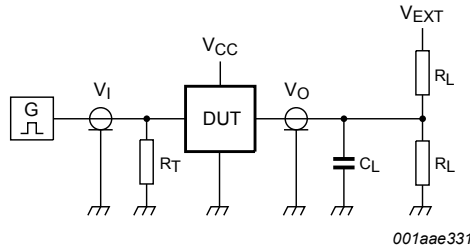
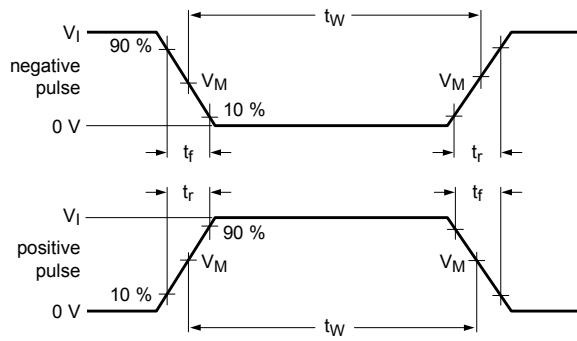


Table 8. Measurement points

| Supply voltage | Input | | Output | | |
|---------------------|----------|---------------------|---------------------|--------------------------|--------------------------|
| V_{CC} | V_I | V_M | V_M | V_X | V_Y |
| $\leq 2.3\text{ V}$ | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15\text{ V}$ | $V_{OH} - 0.15\text{ V}$ |
| 2.3 V to 2.7 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15\text{ V}$ | $V_{OH} - 0.15\text{ V}$ |
| 3.0 V to 3.6 V | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.3\text{ V}$ | $V_{OH} - 0.3\text{ V}$ |

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Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 12. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|----------------|----------|---------------|-------|---------------|--------------------|--------------------|--------------------|
| V_{CC} | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PLZ}, t_{PZL} | t_{PHZ}, t_{PZH} |
| ≤ 2.3 V | V_{CC} | ≤ 2.0 ns | 30 pF | 1000 Ω | open | $2 \times V_{CC}$ | GND |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 3.0 V to 3.6 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

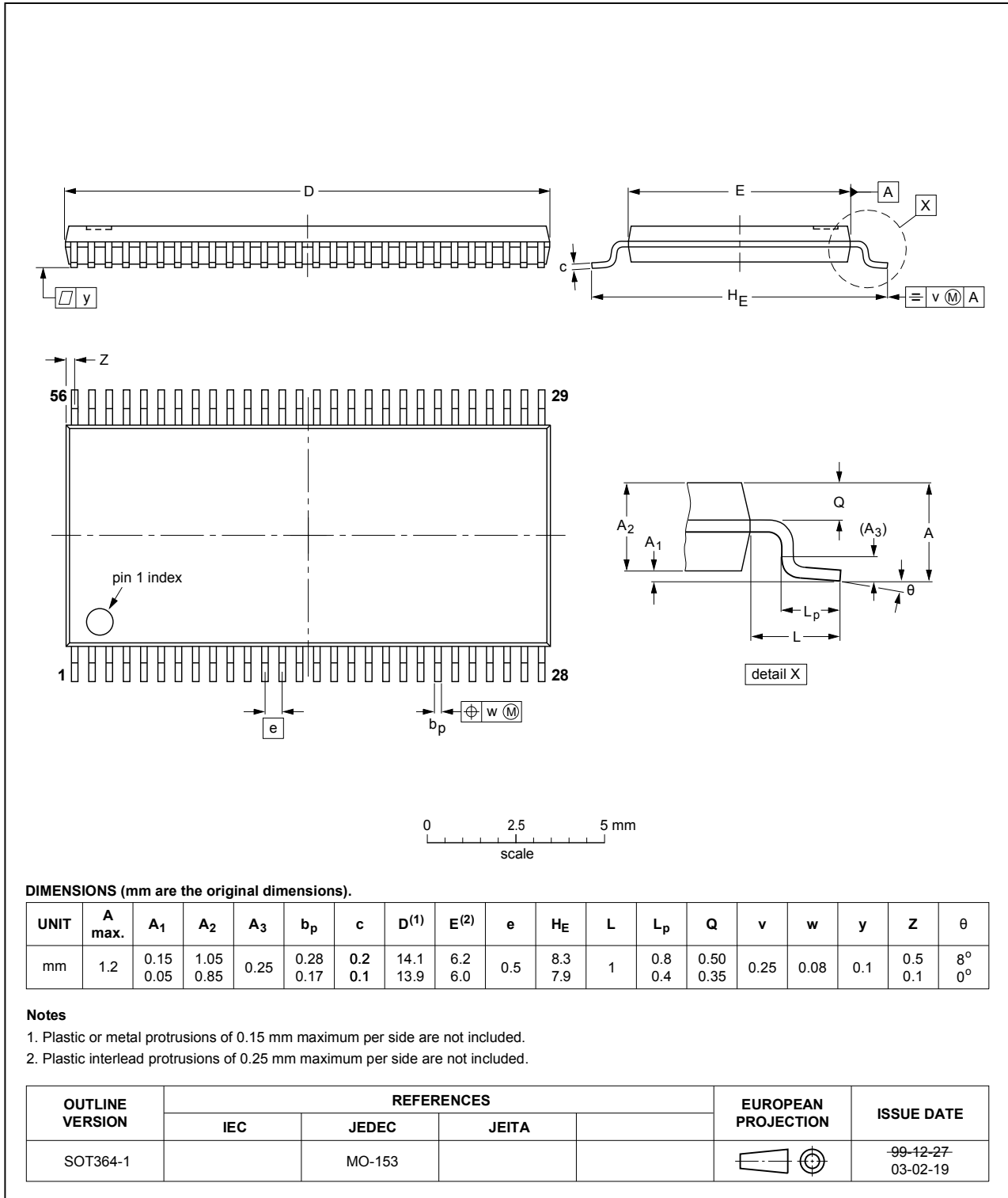


Fig. 13. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DCO | Dynamic Controlled Output |
| DUT | Device Under Test |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|---|---------------------------|---------------|---------------------|
| 74AVC16836A v.6 | 20180924 | Product data sheet | - | 74AVC16836A v.5 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74AVC16836ADGV (SOT481-2) removed. | | | |
| 74AVC16836A v.5 | 20020802 | Product data sheet | - | 74AVC16836A v.4 |
| 74AVC16836A v.4 | 20000803 | Product specification | - | 74AVC16836A v.3 |
| 74AVC16836A v.3 | 20000502 | Preliminary specification | - | 74AVC16836 v.2 |
| 74AVC16836 v.2 | 19990723 | Preliminary specification | - | 74AVC_AVCH16836 v.1 |
| 74AVC_AVCH16836 v.1 | 19981207 | Objective specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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