

FEATURES

- 2.1 Ω on resistance
- 0.5 Ω maximum on-resistance flatness at 25°C
- Up to 390 mA continuous current
- Fully specified at +12 V, ± 15 V, ± 5 V
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- 8-lead MSOP and 8-lead, 3 mm \times 2 mm LFCSP

APPLICATIONS

- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Relay replacements
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communication systems

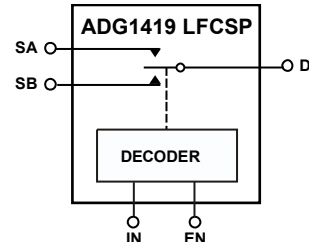
GENERAL DESCRIPTION

The [ADG1419](#) is a monolithic *i*CMOS® device containing a single-pole/double-throw (SPDT) switch. An EN input on the LFCSP is used to enable or disable the device. When disabled, all channels are switched off.

The industrial CMOS (*i*CMOS) modular manufacturing process combines high voltage, complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has achieved. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

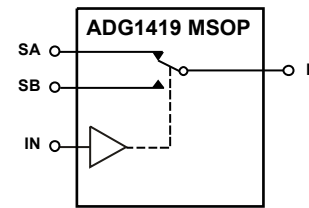
The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. The *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC 0 INPUT.

Figure 1. 8-Lead LFCSP (CP-8-4)



SWITCHES SHOWN FOR A LOGIC 0 INPUT.

Figure 2. 8-Lead MSOP (RM-8)

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. The [ADG1419](#) exhibits break-before-make switching action for use in multiplexer applications.

PRODUCT HIGHLIGHTS

1. 2.4 Ω maximum on resistance at 25°C.
2. Minimum distortion.
3. 3 V logic-compatible digital inputs: $V_{INH} = 2.0$ V, $V_{INL} = 0.8$ V.
4. No V_L logic power supply required.
5. 8-lead MSOP and 8-lead, 3 mm \times 2 mm LFCSP.

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REVISION HISTORY

6/2016—Rev. 0 to Rev. A

Changes to Table 7.....	8
Deleted Table 9; Renumbered Sequentially	8
Change to Figure 6	9

10/2009—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	2.1			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 22
	2.4	2.8	3.2	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.05			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.2	0.25	0.3	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.4			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.5	0.6	0.65	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.5	± 2	± 75	nA max	$V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 23
Drain Off Leakage, I_D (Off)	± 0.2			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 23
	± 0.6	± 3	± 100	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.2			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 24
	± 1	± 3	± 100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	130			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	155	190	220	ns max	$V_S = +10\text{ V}$; see Figure 25
t_{ON} (EN)	85			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	110	125	140	ns max	$V_S = 10\text{ V}$; see Figure 27
t_{OFF} (EN)	115			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	140	160	180	ns max	$V_S = 10\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_D	15			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			8	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 26
Charge Injection	-16			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 28
Off Isolation	-64			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 29
Channel-to-Channel Crosstalk	-64			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 30
Total Harmonic Distortion Plus Noise (THD + N)	0.016			% typ	$R_L = 10\text{ k}\Omega$, 5 V rms , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 32
-3 dB Bandwidth	135			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 31
Insertion Loss	0.16			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 31
C_S (Off)	19			pF typ	$f = 1\text{ MHz}$; $V_S = 0\text{ V}$
C_D (Off)	44			pF typ	$f = 1\text{ MHz}$; $V_S = 0\text{ V}$
C_D , C_S (On)	114			pF typ	$f = 1\text{ MHz}$; $V_S = 0\text{ V}$

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
I_{DD}	0.002		1.0	μA typ μA max	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ Digital inputs = 0 V or V_{DD}
I_{DD} , 8-Lead MSOP	58		95	μA typ μA max	Digital inputs = 5 V
I_{DD} , 8-Lead LFCSP	120		190	μA typ μA max	Digital inputs = 5 V
I_{SS}	0.002		1.0	μA typ μA max	Digital inputs = 0 V, 5 V, or V_{DD}
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	Ground = 0 V

¹ Guaranteed by design, not subject to production test.

+12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	4			Ω typ	$V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$; see Figure 22
On-Resistance Match Between Channels, ΔR_{ON}	4.6 0.08	5.5	6.2	Ω max Ω typ	$V_{DD} = +10.8\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.25 1.2 1.5	0.3 1.75	0.35 1.9	Ω max Ω typ Ω max	$V_S = 0\text{ V}$ to 10 V, $I_S = -10\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1 ± 0.5	± 2	± 75	nA typ nA max	$V_{DD} = +13.2\text{ V}$, $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 23
Drain Off Leakage, I_D (Off)	± 0.2 ± 0.6	± 3	± 100	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 23
Channel On Leakage, I_D , I_S (On)	± 0.2 ± 1	± 3	± 100	nA typ nA max	$V_S = V_D = 1\text{ V}$ or 10 V; see Figure 24
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	200 255	265	370	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 25
t_{ON} (EN)	145 190	220	245	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 27
t_{OFF} (EN)	130 170	205	220	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 8\text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_D	55		33	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 8\text{ V}$; see Figure 26
Charge Injection	13			pC typ	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 28
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 29

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 30
-3 dB Bandwidth	95			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 31
Insertion Loss	0.3			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 31
C_S (Off)	32			pF typ	$f = 1 \text{ MHz}$; $V_S = 6 \text{ V}$
C_D (Off)	72			pF typ	$f = 1 \text{ MHz}$; $V_S = 6 \text{ V}$
C_D , C_S (On)	123			pF typ	$f = 1 \text{ MHz}$; $V_S = 6 \text{ V}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = 13.2 \text{ V}$ Digital inputs = 0 V or V_{DD}
I_{DD} , 8-Lead MSOP	58		1.0	μA max	Digital inputs = 5 V
I_{DD} , 8-Lead LFCSOP	120		95	μA max	Digital inputs = 5 V
V_{DD}			190	μA max	Ground = 0 V, $V_{SS} = 0 \text{ V}$
			5/16.5	V min/max	

¹ Guaranteed by design, not subject to production test.

±5 V DUAL SUPPLY

$V_{DD} = +5 \text{ V} \pm 10\%$, $V_{SS} = -5 \text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	4.5			Ω typ	$V_S = \pm 4.5 \text{ V}$, $I_S = -10 \text{ mA}$; see Figure 22
	5.2	6.2	7	Ω max	$V_{DD} = +4.5 \text{ V}$, $V_{SS} = -4.5 \text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	$V_S = \pm 4.5 \text{ V}$, $I_S = -10 \text{ mA}$
	0.3	0.35	0.4	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.3			Ω typ	$V_S = \pm 4.5 \text{ V}$, $I_S = -10 \text{ mA}$
	1.6	1.85	2	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.1			nA typ	$V_{DD} = +5.5 \text{ V}$, $V_{SS} = -5.5 \text{ V}$ $V_S = \pm 4.5 \text{ V}$, $V_D = \mp 4.5 \text{ V}$; see Figure 23
	± 0.5	± 2	± 75	nA max	
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = \pm 4.5 \text{ V}$, $V_D = \mp 4.5 \text{ V}$; see Figure 23
	± 0.6	± 3	± 100	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 4.5 \text{ V}$; see Figure 24
	± 1	± 3	± 100	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{\text{TRANSITION}}$	310			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	410	495	560	ns max	$V_S = 3 \text{ V}$; see Figure 25
$t_{\text{ON}} (\text{EN})$	230			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	305	355	390	ns max	$V_S = 3 \text{ V}$; see Figure 27
$t_{\text{OFF}} (\text{EN})$	220			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	290	335	365	ns max	$V_S = 3 \text{ V}$; see Figure 27
Break-Before-Make Time Delay, t_D	65			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
			31	ns min	$V_{S1} = V_{S2} = 3 \text{ V}$; see Figure 26
Charge Injection	59			pC typ	$V_S = 0 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 28
Off Isolation	-60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 29
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 30
Total Harmonic Distortion Plus Noise	0.04			% typ	$R_L = 10 \text{ k}\Omega$, 5 V p-p , $f = 20 \text{ Hz to } 20 \text{ kHz}$; see Figure 32
-3 dB Bandwidth	105			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 31
Insertion Loss	0.28			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 31
C_S (Off)	26			pF typ	$V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$
C_D (Off)	62			pF typ	$V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$
C_D , C_S (On)	128			pF typ	$V_S = 0 \text{ V}$, $f = 1 \text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{\text{DD}} = +5.5 \text{ V}$, $V_{\text{SS}} = -5.5 \text{ V}$ Digital inputs = 0 V or V_{DD}
I_{SS}	0.001		1.0	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
$V_{\text{DD}}/V_{\text{SS}}$			$\pm 4.5/\pm 16.5$	V min/max	Ground = 0 V

¹ Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL¹					
$\pm 15 \text{ V Dual Supply}$					$V_{\text{DD}} = +13.5 \text{ V}$, $V_{\text{SS}} = -13.5 \text{ V}$
8-Lead MSOP ($\theta_{\text{JA}} = 206^\circ\text{C/W}$)	215	135	80	mA maximum	
8-Lead LFCSP ($\theta_{\text{JA}} = 50.8^\circ\text{C/W}$)	390	215	100	mA maximum	
$+12 \text{ V Single Supply}$					$V_{\text{DD}} = 10.8 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$
8-Lead MSOP ($\theta_{\text{JA}} = 206^\circ\text{C/W}$)	175	115	70	mA maximum	
8-Lead LFCSP ($\theta_{\text{JA}} = 50.8^\circ\text{C/W}$)	320	185	95	mA maximum	
$\pm 5 \text{ V Dual Supply}$					$V_{\text{DD}} = +4.5 \text{ V}$, $V_{\text{SS}} = -4.5 \text{ V}$
8-Lead MSOP ($\theta_{\text{JA}} = 206^\circ\text{C/W}$)	165	110	70	mA maximum	
8-Lead LFCSP ($\theta_{\text{JA}} = 50.8^\circ\text{C/W}$)	310	180	95	mA maximum	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	-0.3 V to +25 V
V_{SS} to GND	+0.3 V to -25 V
Analog Inputs ¹	$V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Digital Inputs ¹	GND - 0.3 V to $V_{DD} + 0.3$ V or 30 mA, whichever occurs first
Peak Current, S or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	
8-Lead MSOP (4-Layer Board)	400 mA
8-Lead LFCSP	600 mA
Continuous Current per Channel, S or D	Data in Table 4 + 15% mA
Operating Temperature Range	
Industrial	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260°C

¹ Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 6. Thermal Resistance

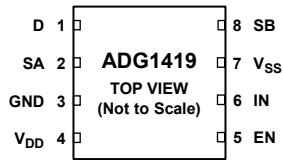
Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (4-Layer Board)	206	44	°C/W
8-Lead LFCSP	50.8		°C/W

ESD CAUTION



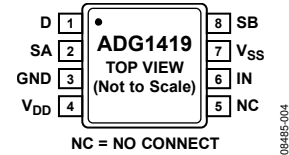
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS} .

Figure 3. 8-Lead LFCSP Pin Configuration



NC = NO CONNECT

Figure 4. 8-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.		Mnemonic	Description
LFCSP	MSOP		
1	1	D	Drain Terminal. This pin can be an input or output.
2	2	SA	Source Terminal. This pin can be an input or output.
3	3	GND	Ground (0 V) Reference.
4	4	V_{DD}	Most Positive Power Supply Potential.
5	Not applicable	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the IN logic input determines which switch is turned on.
Not applicable	5	NC	No Connect.
6	6	IN	Logic Control Input.
7	7	V_{SS}	Most Negative Power Supply Potential.
8	8	SB	Source Terminal. This pin can be an input or output.
0	Not applicable	EPAD	Exposed Pad. Exposed pad tied to substrate, V_{SS} .

Table 8. 8-Lead LFCSP Truth Table

EN	IN	Switch A	Switch B
0	X	Off	Off
1	0	On	Off
1	1	Off	On

Table 9. 8-Lead MSOP Truth Table

IN	Switch A	Switch B
0	On	Off
1	Off	On

TYPICAL PERFORMANCE CHARACTERISTICS

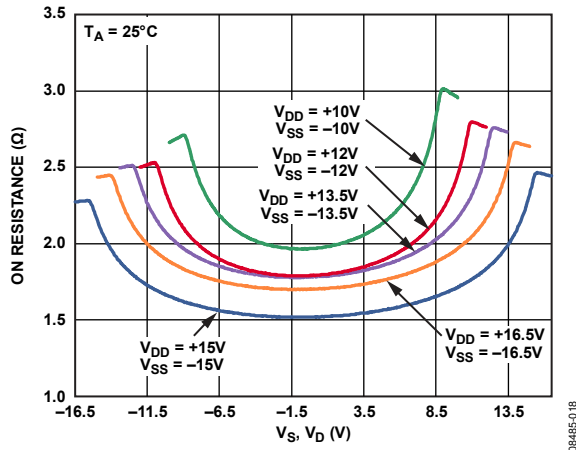


Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

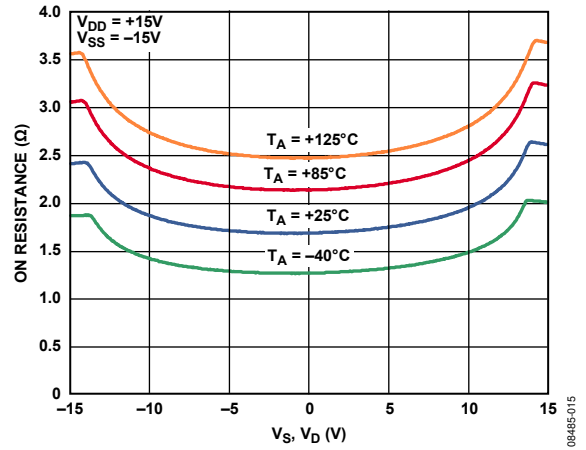


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, ± 15 V Dual Supply

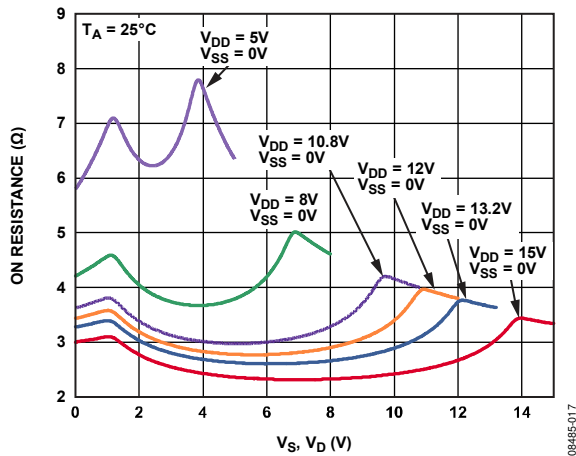


Figure 6. On Resistance as a Function of V_D (V_S) for Single Supply

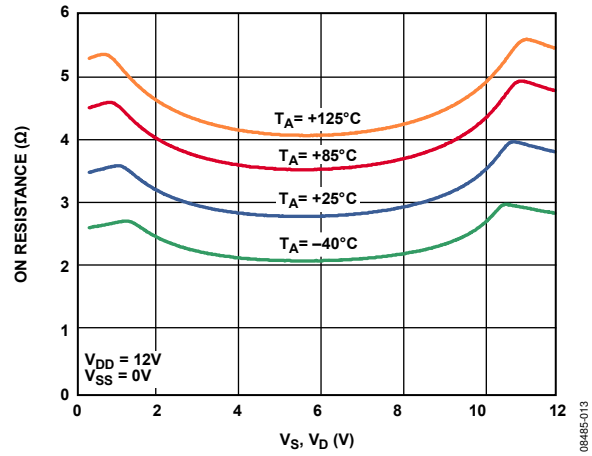


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, +12 V Single Supply

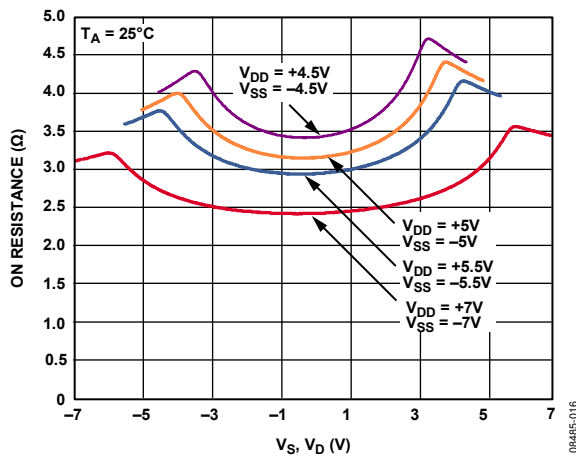


Figure 7. On Resistance as a Function of V_D (V_S) for Dual Supply

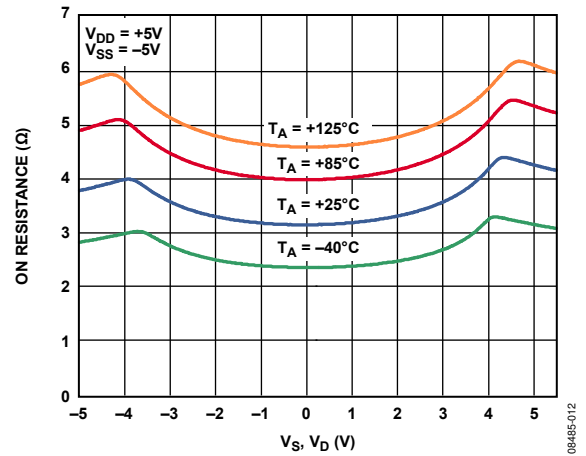


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, ± 5 V Dual Supply

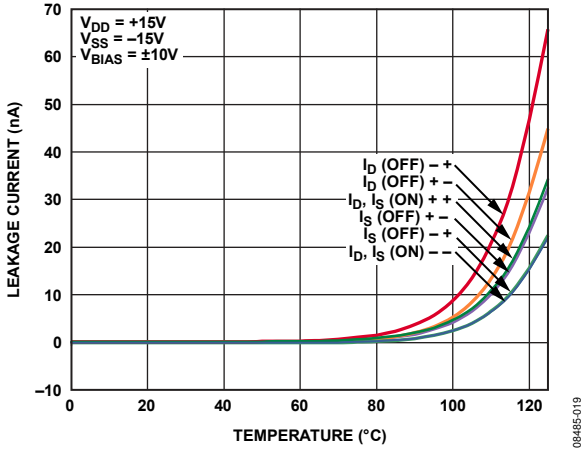


Figure 11. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

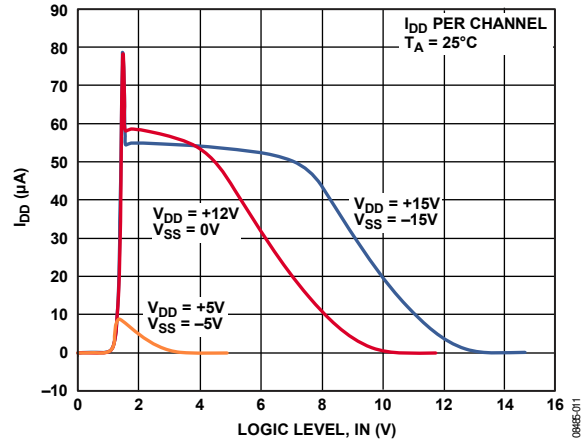


Figure 14. I_{DD} vs. Logic Level

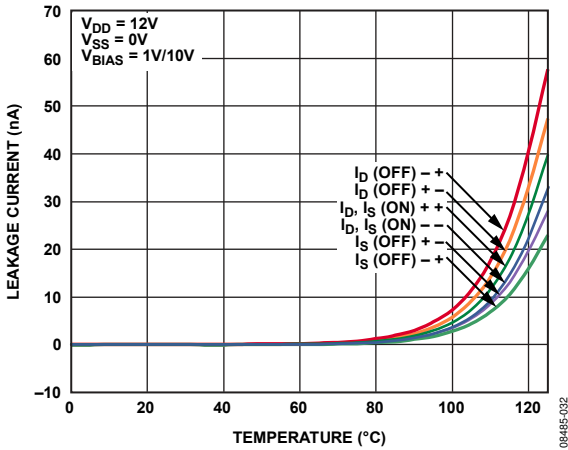


Figure 12. Leakage Currents as a Function of Temperature, +12 V Single Supply

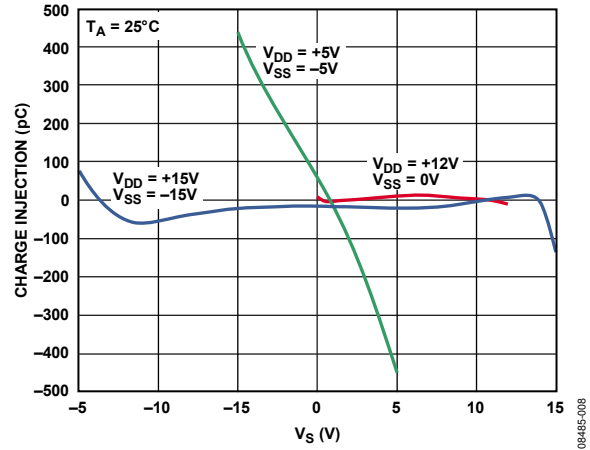


Figure 15. Charge Injection vs. Source Voltage

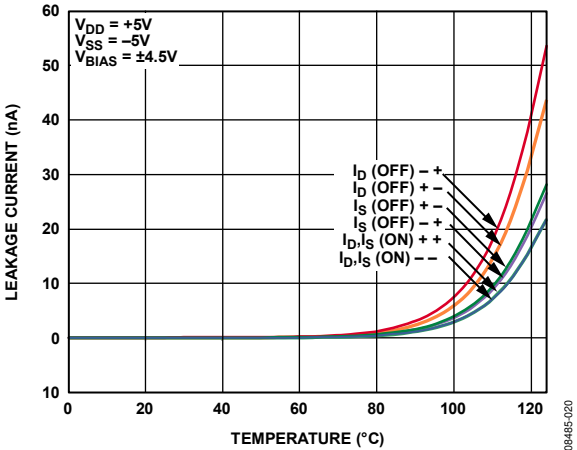


Figure 13. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

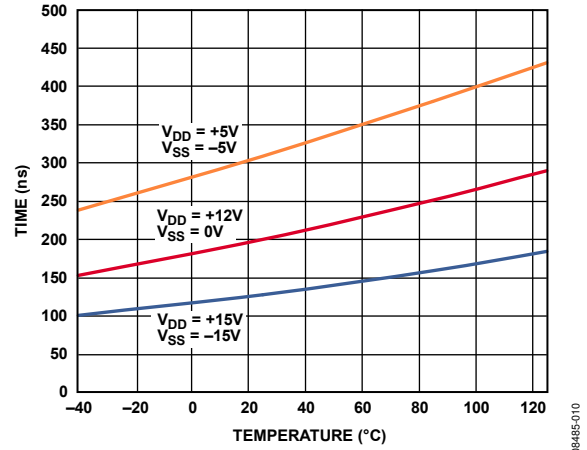


Figure 16. $t_{TRANSITION}$ Times vs. Temperature

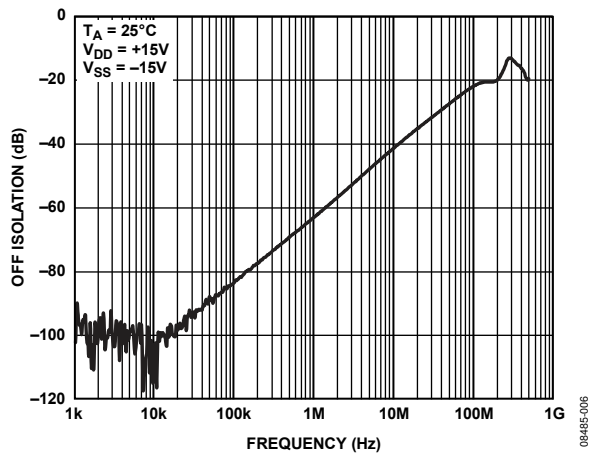


Figure 17. Off Isolation vs. Frequency

08485-006

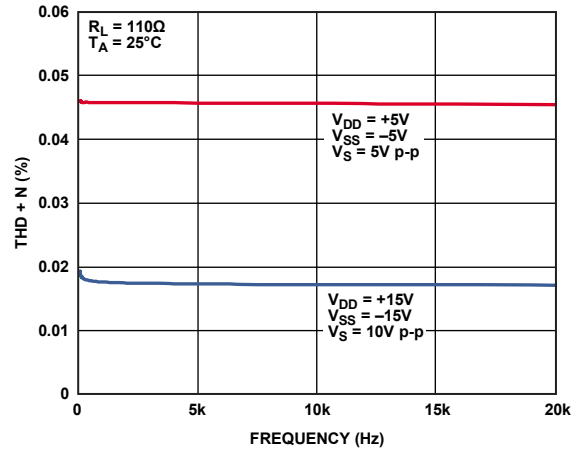


Figure 20. THD + N vs. Frequency

08485-009

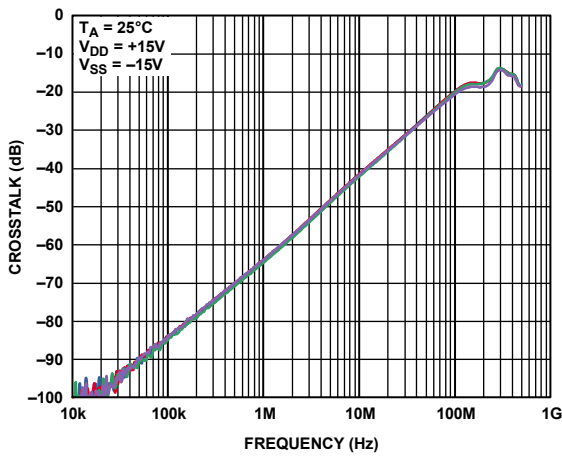


Figure 18. Crosstalk vs. Frequency

08485-033

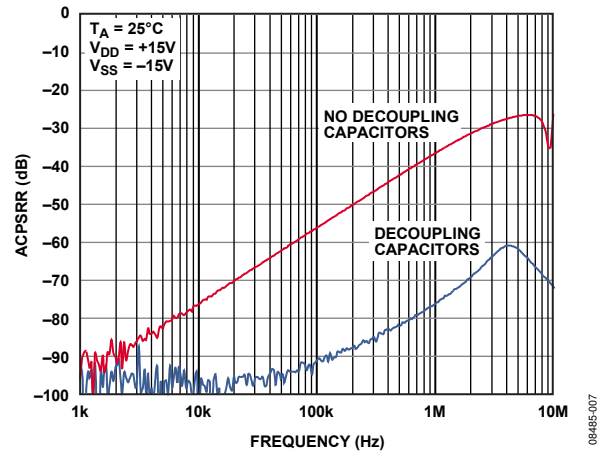


Figure 21. ACPSRR vs. Frequency

08485-007

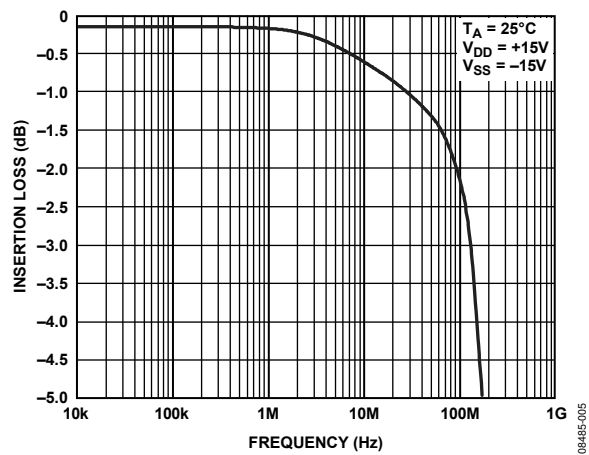


Figure 19. On Response vs. Frequency

08485-005

TEST CIRCUITS

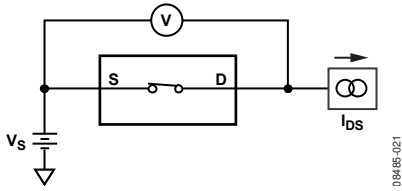


Figure 22. On Resistance

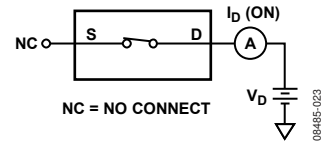


Figure 24. On Leakage

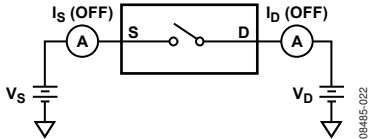


Figure 23. Off Leakage

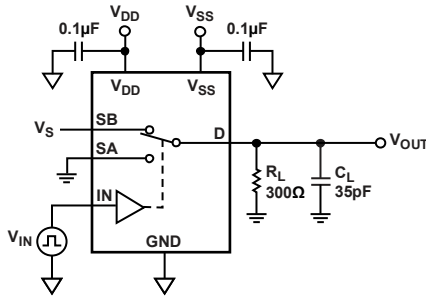


Figure 25. Switching Times, t_{ON} and t_{OFF}

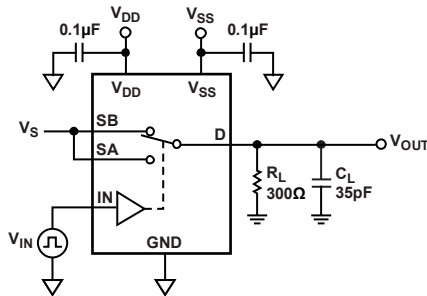
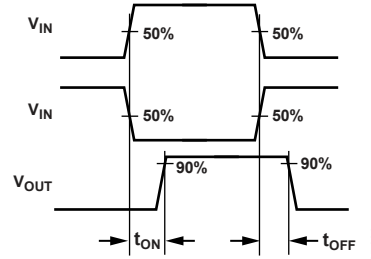


Figure 26. Break-Before-Make Time Delay

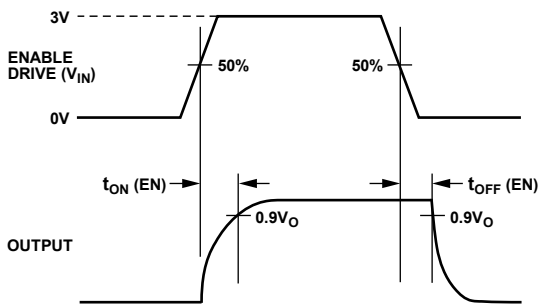
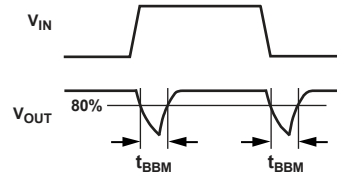
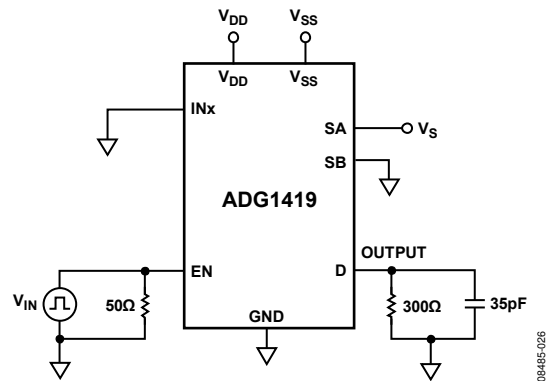


Figure 27. Enable Delay, $t_{ON} (EN)$, $t_{OFF} (EN)$



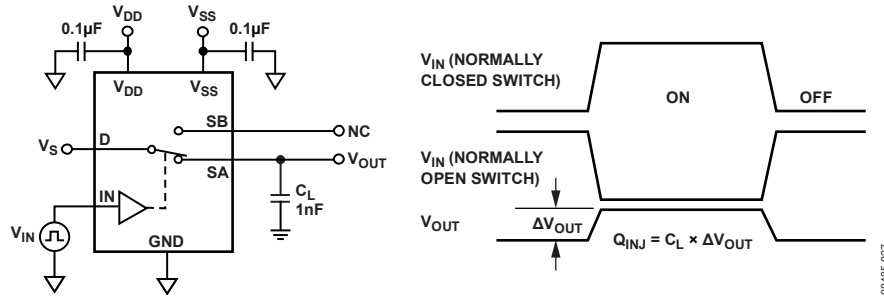


Figure 28. Charge Injection

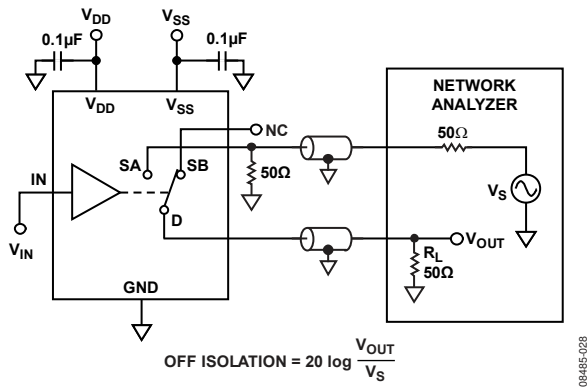


Figure 29. Off Isolation

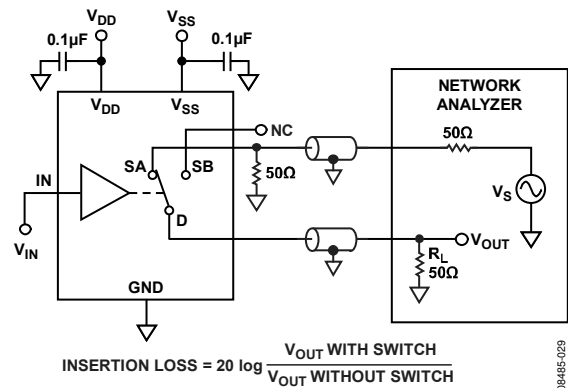


Figure 31. Bandwidth

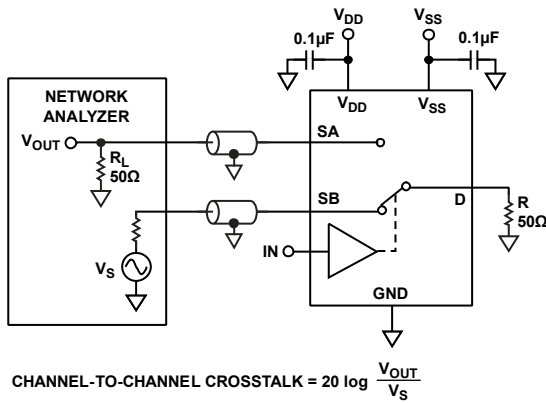


Figure 30. Channel-to-Channel Crosstalk

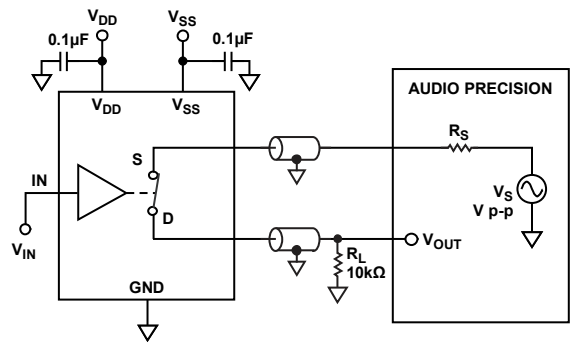
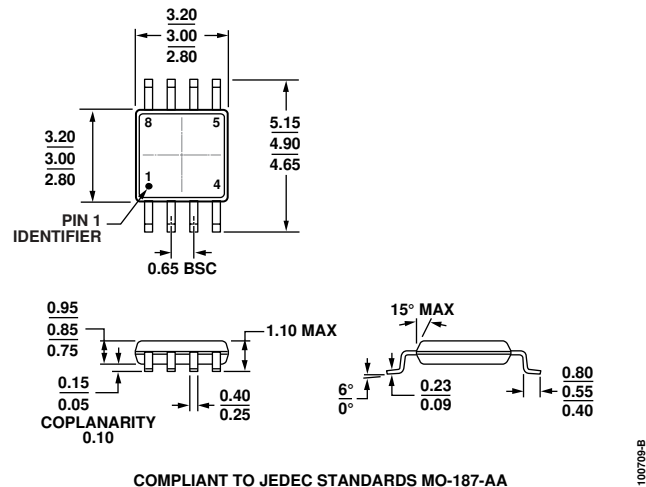


Figure 32. THD + N

TERMINOLOGY

I_{DD}	The positive supply current.	t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch on condition. See Figure 27.
I_{SS}	The negative supply current.	t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch off condition. See Figure 27.
V_D (V_S)	The analog voltage on Terminal D and Terminal S.	t_{TRANSITION}	Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.
R_{ON}	The ohmic resistance between Terminal D and Terminal S.	T_{BBM}	Off time measured between the 80% point of both switches when switching from one address state to another. See Figure 26.
R_{FLAT} (ON)	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching. See Figure 28.
I_S (Off)	The source leakage current with the switch off.	Off Isolation	A measure of unwanted signal coupling through an off switch. See Figure 29.
I_D (Off)	The drain leakage current with the switch off.	Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See Figure 30.
I_D, I_S (On)	The channel leakage current with the switch on.	Bandwidth	The frequency at which the output is attenuated by 3 dB. See Figure 31.
V_{INL}	The maximum input voltage for Logic 0.	On Response	The frequency response of the on switch.
V_{INH}	The minimum input voltage for Logic 1.	Insertion Loss	The loss due to the on resistance of the switch. See Figure 31.
I_{INL} (I_{INH})	The input current of the digital input.	THD + N	The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See Figure 32.
C_S (Off)	The off switch source capacitance, measured with reference to ground.	AC Power Supply Rejection Ratio (ACPSRR)	ACPSRR measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR. See Figure 21.
C_D (Off)	The off switch drain capacitance, measured with reference to ground.		
C_D, C_S (On)	The on switch capacitance, measured with reference to ground.		
C_{IN}	The digital input capacitance.		

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 33. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

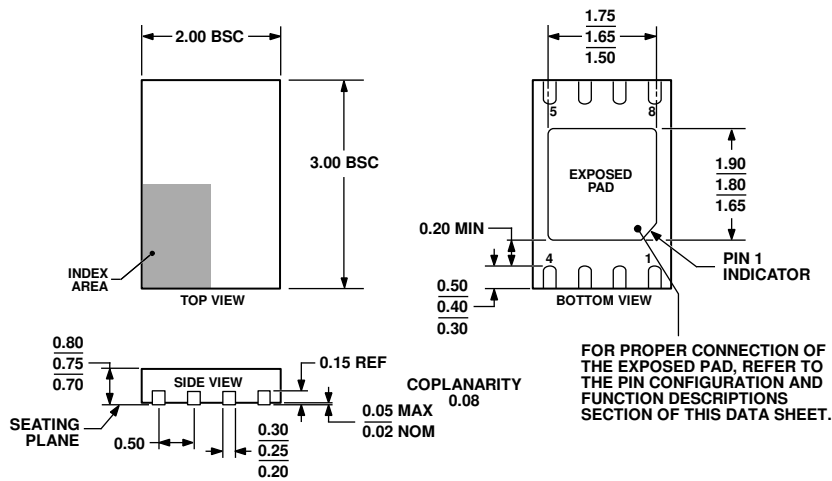


Figure 34. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]

3 mm x 2 mm Body, Very Very Thin, Dual Lead

(CP-8-4)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG1419BRMZ	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1L
ADG1419BRMZ-REEL7	-40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	S1L
ADG1419BCPZ-REEL7	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-4	1C

¹ Z = RoHS Compliant Part.

NOTES