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# Preface

## About This User Guide

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This User Guide describes the features and applications of the SOC VoIP-I-4K Product Details on the I/O interfaces and the corresponding components are provided.

## Related Documents

### Datasheets of IP Cores

- [Datasheet - H.265 Encoder IP Cores](#)
- [Datasheet - H.265 Decoder IP Cores](#)
- [Datasheet - H.264 Encoder IP Cores](#)
- [Datasheet - H.264 Decoder IP Cores](#)
- [Datasheet – MPEG-2 Encoder IP Cores](#)
- [Datasheet – MPEG-2 Decoder IP Cores](#)
- [Datasheet – H.264-to-H.265 Transcoder IP Cores](#)
- [Datasheet – H.265-to-H.264 Transcoder IP Cores](#)
- [Datasheet - MPEG2-to-H.264 Transcoder IP Cores](#)
- [Datasheet - H.264-to-MPEG2 Transcoder IP Cores](#)

### Integration Sheets of IP Cores

- [Integration Sheet - H.265 Encoder IP Cores](#)
- [Integration Sheet - H.265 Decoder IP Cores](#)
- [Integration Sheet - H.264 Encoder IP Cores](#)
- [Integration Sheet - H.264 Decoder IP Cores](#)
- [Integration Sheet - H.265 4K Encoder IP Cores](#)
- [Integration Sheet - H.265 4K Decoder IP Cores](#)
- [Integration Sheet - H.264 4K Encoder IP Cores](#)
- [Integration Sheet - H.264 4K Decoder IP Cores](#)
- [Integration Sheet - MPEG-2 Encoder IP Cores](#)
- [Integration Sheet - MPEG-2 Decoder IP Cores](#)
- [Integration Sheet - H.264-to-MPEG2 Transcode IP Cores](#)
- [Integration Sheet - MPEG2-to-H264 Transcoder IP Cores](#)

### Datasheets of Codec Modules

- [Datasheet - MPEG Video-Audio Codec Modules - Standard Version](#)
- [Datasheet - MPEG Video-Audio Codec Modules - NET version](#)

### Datasheets of Codec Chipsets

- [Datasheet - H.264 Encoder Chipsets](#)
- [Datasheet - H.264 Decoder Chipsets](#)

## VoIP-I-4K Board

### 1. Overview

The SOC VoIP-I-4K is a versatile FPGA board designed for multiple functions/products. Customers can use the VoIP-I-4K for their products directly (OEM Product), or as a product development platform. SOC customizes the firmware based on customer requests to enable easy customer product development. SOC also ships pre-configured VoIP-I-4K as H.264/H.265/MPEG-2 video encoders/transmitters (over IP networks), receivers/decoders, and transcoders. The applications of the VoIP-I-4K are described in the next Section of this document.

The VoIP-I-4K has its own FPGA chip, the Intel Arria-10 SX660, which controls the I/Os and also houses the SOC codec IP cores. The VoIP-I-4K has 16Gbits DDR3 memories of 64 bits data for the FPGA logics and 8Gbits of DDR3 memories of 32 bits data for the ARM processor. The VoIP-I-4K provides one HDMI2.0 input port and one HDMI2.0 output port. It also has two 12G SDI ports with each can be configured into either input or output. The SDI port are also backward compatible with 6G or 3G. The VoIP-I-4K has one tri-speed Ethernet port (10/100/1000Mbps) with the UDP/RTP/IP compatibilities (firmware preinstalled). The VoIP-I-4K Board is shown in Figure 1 (top view) and Figure 2 (bottom view). A block diagram of the VoIP-I-4K schematics is provided in Section 3.1.

#### **Key Features**

- Intel Arria-10 SX660 FPGA
- 8Gbit DDR3 memory for ARM (32bits), 16Gbit DDR3 for FPGA (64bits)
- One HDMI2.0 input and one HDMI2.0 output
- Two 12G SDI ports (each can be configured into either input or output independently)
- Tri-speed Ethernet (10/100/1000 Mbps)
- Mini USB as an URAT port
- Two Razer-Beam Extension Connectors, allows two VoIP-I-4K to be connected together for 8K videos
- SD memory Card
- JTAG for on board FPGA configurations.

### Dimension

The dimension of the VoIP-I-4K is 107mm x 87mm x 20mm

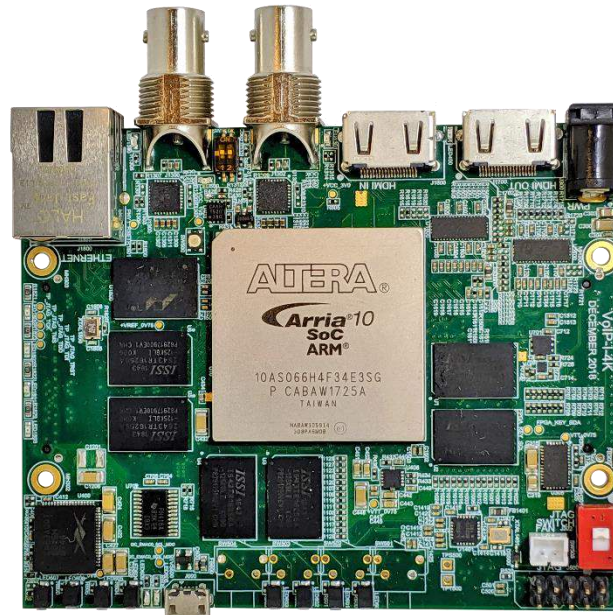


Fig.1 VoIP-I-4K Top View

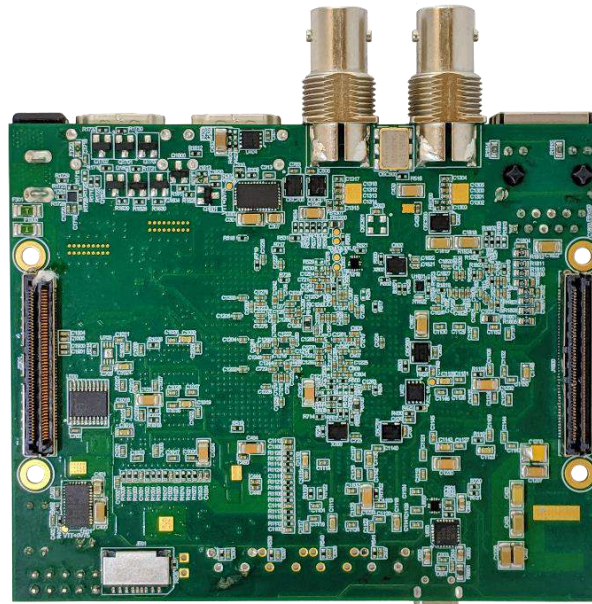


Fig. 2 VoIP-I-4K bottom View



## 2. Applications of the VoIP-I-4K

### 2.1 OEM MPEG Video Codec Products

The VoIP-I-4K, with an H.264 or H.265 (or MPEG-2) encoder or a decoder IP core, is a ready-to-use H.264 (or H.265 or MPEG-2) video/audio over the Internet (IP) or wireless (connected to a wireless transponder) 4k@30/60 transmitter or receiver which is offered as an OEM product by SOC. The VoIP-I-4K can also be configured into multi-channel HD video/audio transmitters, receivers, or transponders. Standard products include:

1. Single-channel 4K@60 H.264 video encoder and transmitter (over IP networks)
2. Dual-channel 4K@30 H.264 video encoder and transmitter (over IP networks)
3. Single-channel 4K@60 H.265 video encoder and transmitter (over IP networks)
4. Dual-channel 4K@30 H.265 video encoder and transmitter (over IP networks)
5. Single-channel 4K@60 H.264 video decoder and receiver (over IP networks)
6. Dual-channel 4K@30 H.264 video decoder and receiver (over IP networks)
7. Single-channel 4K@60 H.265 video decoder and receiver (over IP networks)
8. Dual-channel 4K@30 H.265 video decoder and receiver (over IP networks)
9. The above products connecting to WIFI or radio transponders for wireless video communications.
10. The above devices with customizations based on customer requirements

Fig. 3 shows an example of two VoIP-I-4K boards for 4K video over IP application. In the example, one VoIP-I-4K is configured into a 4K transmitter and the second is configured into a 4K receiver. The VoIP-I-4K can also be used for bidirectional 4K video communications (4K video conferencing), as shown in Fig. 4.

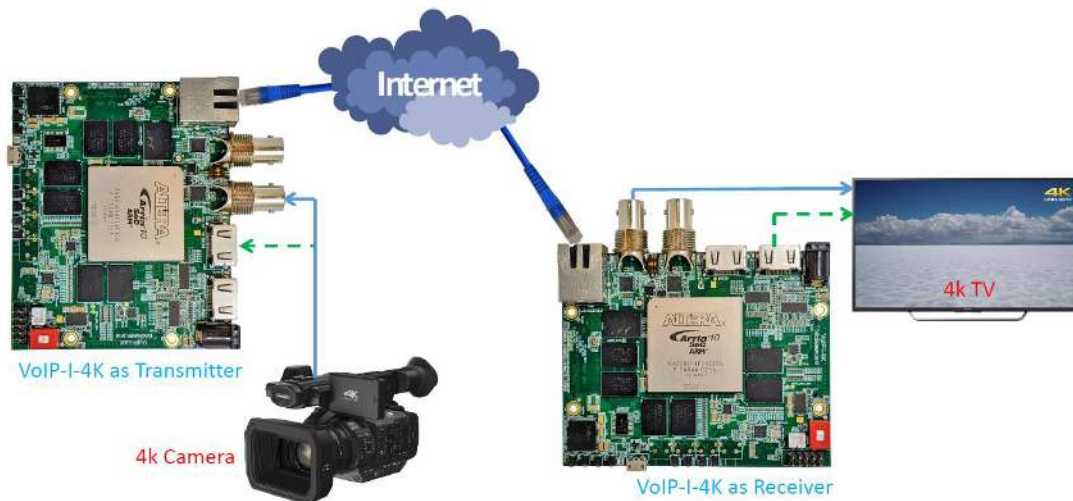


Fig. 3 The VoIP-I-4K is used for 4K video-over-IP

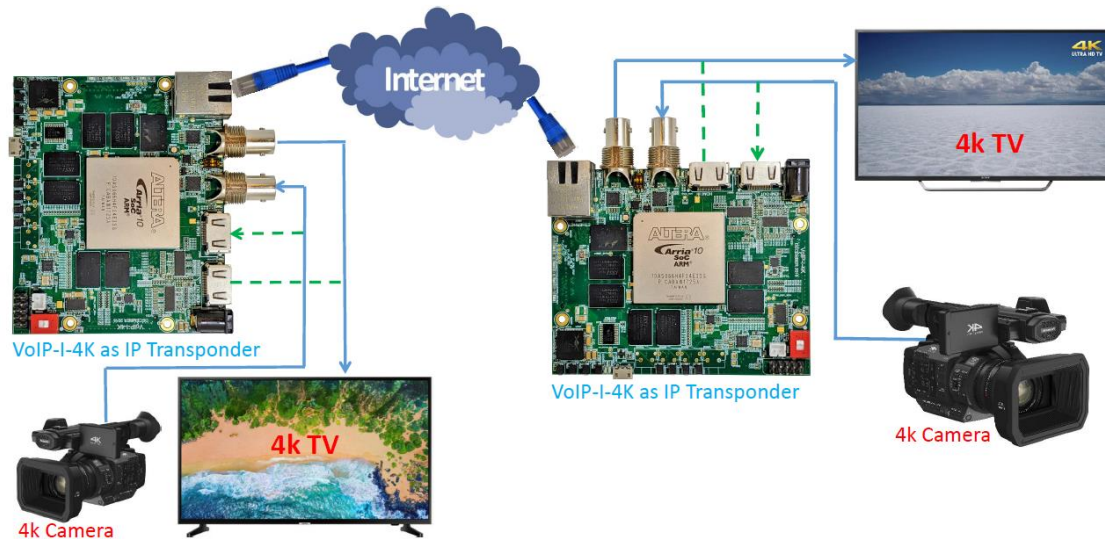


Fig. 4 The VoIP-I-4K is used for 4K video conferencing

## 2.2 Product Development Platform based on the SOC Codec IP Cores

The VoIP-I-4K is a versatile platform for product development, based on the SOC MPEG codec IP cores, for end-user product development. SOC supplies the MPEG codec IP cores, including H.264, H.265, or MPEG-2 encoder, decoder, or transcoder cores.

SOC also provides (under licensing agreement) “netlist” IP cores for all the I/O ports, including the network (UDP/IP over Ethernet) stack for the VoIP-I-4K, so that the users can drop them into their own designs without having to implement the I/O drivers.

Design templates of the I/O drivers and the network stack IP cores are available for licensing. These can greatly speed up the development process.

The PDF schematics design of the VoIP-I-4K is available under IP core licensing agreement or with the purchase of the VoIP-I-4Kboard, which provides the details information for using the board for product development. Users can also purchase the full PCB design files (e.g. Gerber file) from SOC, which can be used as a reference for the user PCB once the product is developed. Contact SOC sales ([sales@soctechnologies.com](mailto:sales@soctechnologies.com)) for details.



## 2.3 Evaluation Kit for SOC 4K@30/60 Codec IP cores, and Chipsets

The VoIP-I-4K is preloaded with firmware for evaluating the SOC 4K@30/60 MPEG codec IP cores. It is a plug-and-play system that allows the user to connect the I/O devices to start the evaluation.

For encoder evaluation, the 4K@30/60 input video source is sent to the VoIP-I-4K via the 12G SDI port (configured to input); the encoded stream is sent to the computer through the Ethernet port. Users can decode the encoded streams by using standard software decoders, refer to Fig. 5.

It is noted that due to the latency caused by the computer, this setup cannot be used to test the latency of the SOC encoder and the VoIP-I-4K. The setup showing in Fig. 7 can be used for testing both the video quality and the latency.

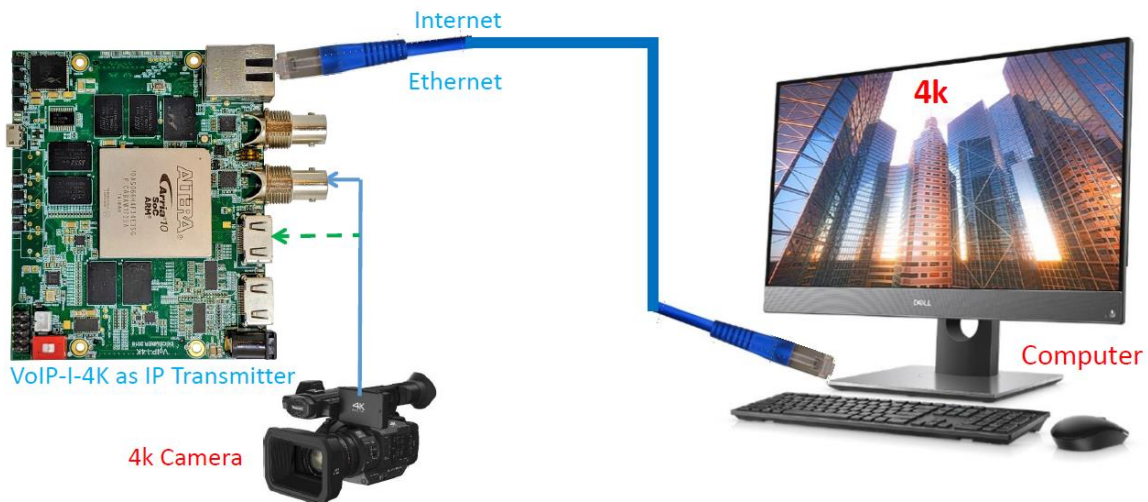


Fig. 5 Setup for evaluating the SOC encoder IP core using one VoIP-I-4K and a computer

For decoder evaluation, a computer can be used to send the compressed streams to the VoIP-I-4K through the Ethernet. The software for sending the streams is provided as part of the VoIP-I-4K package. The decoded 4K video and audio data are sent to display via the 12G SDI output port, as shown in Fig. 6.

Same as the encoder evaluation using a computer, the setup of Fig. 6 cannot be used to test the decoder latency due to the computer decoding latency.

Fig. 7 shows a setup for testing the glass-to-glass latency of SOC encoder and decoder latency. The end-to-end latency is less than 1 frame time, without transmitter and receiver synchronization. With the transmitter and receiver synchronization, the latency can reach as low as 10ms. The transmitter

and receiver synchronization is achieved by a controllable oscillator and control firmware on the receiver, which synchronizes the clock of the receiver with the transmitter clock (compensates the clock drifting).

The end-to-end latency of encoding, the network, and decoding can be measured by observing the time difference of the input video on the transmitter side (loop back video) versus the output video on the decoder side. A digital clock with millisecond accuracy can be put in front of the camera, which allows the clock display on both the loop back TV and the TV on the decoder side.

The setup of Fig. 7 can also be used for simultaneous evaluation of the 4K encoder and 4K decoder, Detailed instructions for evaluating the SOC encoders and decoders using the VoIP-I-4K are provided in “Instruction Sheet of Using the VoIP-I-4K to Evaluate SOC Codec Modules and IP cores”.

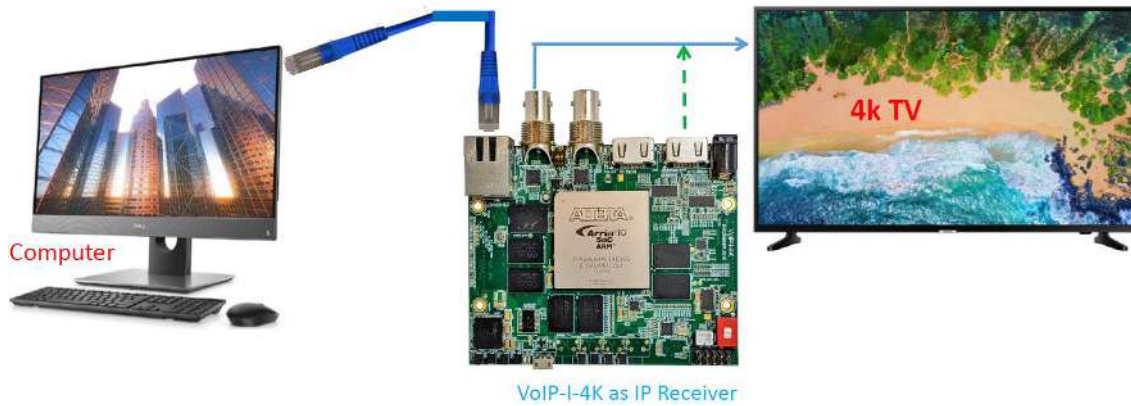


Fig. 6 Setup for evaluating the SOC decoder IP core using a computer and one VoIP-I-4K

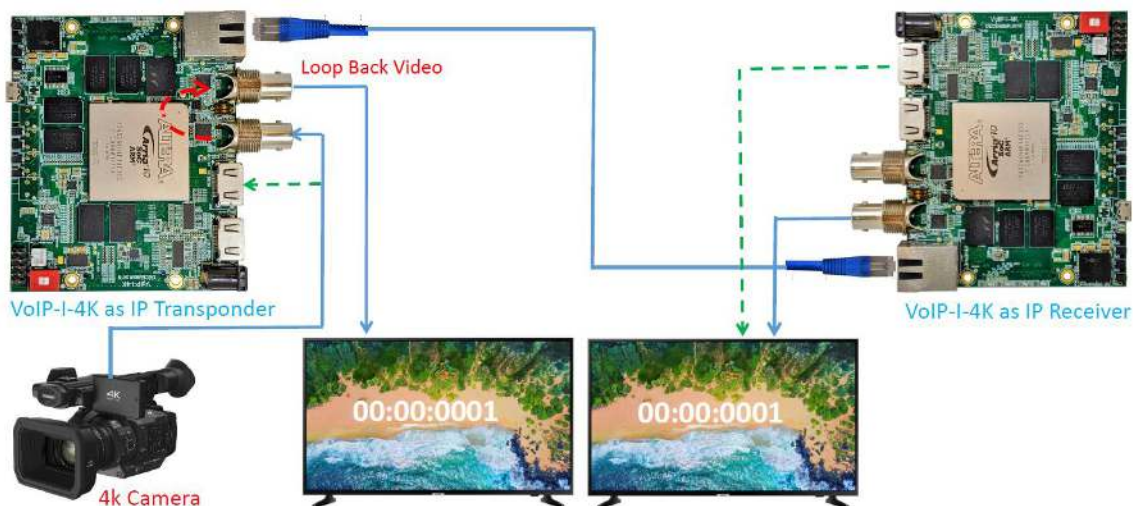


Fig. 7 Setup for testing the SOC encoder and decoder glass-to-glass latency

### 3. Hardware Descriptions

#### 3.1 Block Diagram

Fig.8 shows a block diagram of the VoIP-I-4K board.

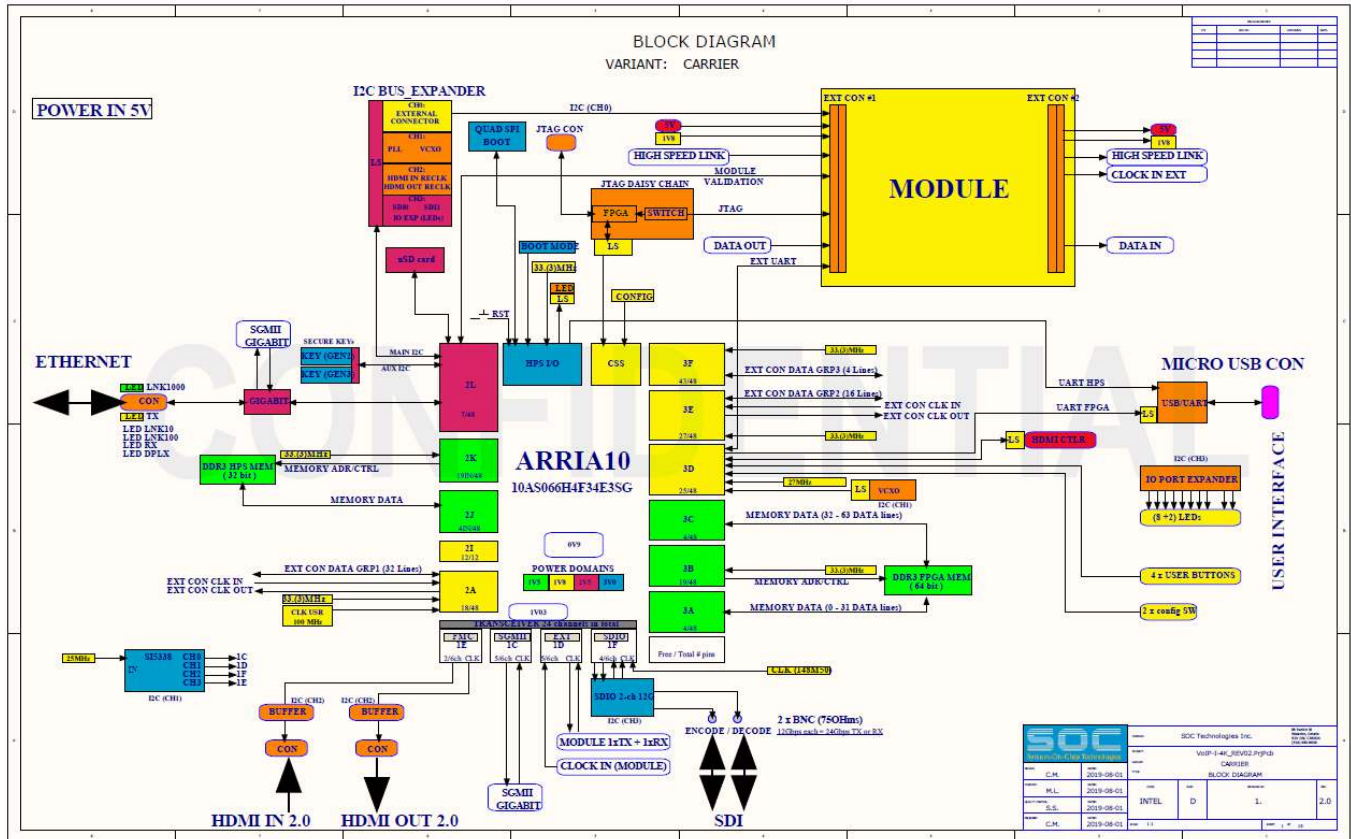


Fig. 8 Block diagram of VoIP-I-4K board

#### 3.2 Key Components

Table-1 lists the components on the VoIP-I-4K that are important to users. Refer to the schematics of the VoIP-I-4K for the circuit design and the auxiliary components, if needed. The PCB schematics can be licensed from SOC.

The following Sections describe the components listed in Table-1. Refer to the datasheets of the components for further details.

**Table-1 Major components on the VoIP-I-4K**

Item	Part Name	Description	Manufacturer
1	10AS066H4F34	FPGA, Intel Arria-10	Intel
2	IS43TR16256AL-125KBL	DDR3 Memory	ISSI
3	PI3HDX1204-BZHEX	HDMI2.0 Receiver Equalizer (input)	Diodes Incorporated
4	PI3HDX1204-BZHEX	HDMI2.0 Transmitter (output)	Diodes Incorporated
5	LMH1297	12G UHD-SDI Bidirectional I/O with Integrated Reclocker	TI
6	88E1111_BAB1C000	Gigabit Ethernet Transceiver, 10/100/1000	Marvell
7	CP2103	SINGLE-CHIP USB TO UART BRIDGE	Silicon Labs
8	MT25QL01GBBB8E12-OSIT	1Gb, Flash Memory	MICRON
13	MM80-204B1	CONN 204POS DDR3 SDRAM SODIMM	JAE Electronics
14	DS28C36Q+T	IP PROTECTED EEPROM	MAXIM

### 3.2.1 FPGA

The FPGA on the VoIP-I-4K is the Intel Arria-10 10AS066H4F34. Refer to the Data Sheet of the FPGA for further details.

### 3.2.2 DDR3 Memories

The VoIP-I-4K is equipped with 16Gbits of DDR3 memories of 64 data lines for the FPGA logics side, and 8Gbits of DDR3 (32 bits data) for the ARM processor. The part number of the memory chip is IS43TR16256AL-125KBL for both the FPGA logic and the ARM processor.

### 3.2.3 HDMI Receiver

The HDMI2.0 receiver IP core is inside the FPPA. A Receiver Equalizer is on the PCB at the physical level, which is the PI3HDX1204-BZHEX by Diodes Incorporated.

### 3.2.4 HDMI Transmitter

The HDMI2.0 transmitter IP core is also inside the FPGA. A transmitter line driver is placed on the PCB to drive the signal to the SDI connector. The manufacture part number of the HDMI2.0 line driver is PI3HDX1204-BZHEX which is also a product of Diodes Incorporated.

### 3.2.5 12G SDI Transmitter/ Receiver

The SOC VoIP-I-4K has two 12G SDI ports, each is connected to a TI 12G liner driver/equalizer, part number LMH1297, which can be configured into an input or output. The 12G SDI IP core is located inside the FPGA, which is also configurable for input or output.

The SDI ports are backward compatible to 6G or 3G, which are configured by the SDI IP core.

### 3.2.6 Gigabit Ethernet

The Ethernet PHY is the 88E1111\_BAB1C000 by Marvel. It can be used for 10Mbps/100Mbps/1000Mbps. The configuration file is included in the I/O package. The network stack IP core can be licensed from SOC. An Ethernet MAC core is a part of the Ethernet/UDP/IP network stack which can be licensed separately from the UP/IP network stack. For evaluations, the networks stack is preloaded to allow a plug-and-play system.

### 3.2.7 Mini USB

The VoIP-I-4K has a mini USB connector which is used as an UART port. The CP2103, single-chip USB to UART bridge, is used as the interface chip.

### 3.2.8 Flash Memory

The flash memory, MT25QL01G BBB8E12-0SIT is used to store the firmware of the FPGA. Two of the MT25QL01G BBB8E12-0SIT chips are cascaded into 2Gb flash memory. For evaluation, the I/O drivers and the Ethernet/UDP/IP network stack are pre-stored in the MT25QL01G BBB8E12-0SIT. When the VoIP-I-4K is booted, the firmware stored in the MT25QL01G BBB8E12-0SIT will configure the FPGA and make the board a plug-and-play device to facilitate the evaluations of the SOC MPEG codec modules.

After the evaluation, users can store their own firmware into the MT25QL01G BBB8E12-0SIT for product development. For product development purposes, the I/O driver and the Ethernet/UDP/IP network stack IP cores in “netlist” format are available for licensing. The method of downloading the firmware into the MT25QL01G BBB8E12-0SIT is detailed in Evaluation Instruction Manual.

## 4. Ordering Information

The VoIP-I-4K can be ordered from SOC directly or through the distributors of SOC. Refer to the SOC web site, [www.soctechnologies.com](http://www.soctechnologies.com), for distributor locations and contact information.

**SOC contacts:**

E-mail: [sales@soctechnologies.com](mailto:sales@soctechnologies.com)

Telephone: 1-519-880-8609

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
01/08/2019	SOC initial Release	1.0

**Note:**

**The PCB Schematics and full PCB design in Altium of the VoIP-I-4K can be licensed from SOC. Contact: [sales@soctechnologies.com](mailto:sales@soctechnologies.com)**