Product Brief

≫ HX6537/39/40-A
WE-I Plus ASIC
Preliminary version 01 February, 2020

Revision History

February, 2020

Version	Date	Description of changes
01	2020/02/03	New setup.

HX6537/39/40-A
WE-I Plus ASIC

Himax Technologies, Inc.
http://www.himax.com.tw

Preliminary Version 01

February, 2020

1. General Description

The HX6537/39/40-A is an ultra-low power, high performance microcontroller designed for battery-powered TinyML applications.

The HX6537/39/40-A is embedded with a powerful 400MHz ARC EM9D DSP core with Floating Point Unit and XY local data memory architecture to accelerate convolution operation of neural network algorithm. There are internal 2 MB ultra-low-leakage SRAMs for system and program usage. With the benefit of DSP instruction and XY memory architecture, HX6537/39/40-A can operate at lower clock speed to achieve the same application performance for lower power consumption.

Besides traditional interrupt-based trigger wakeup mechanism from deep-sleep or shutdown mode, HX6537/39/40-A provides a new multi-layer power management scheme to wakeup CMOS sensor periodically for ultra-low power applications. The multi-layer power management is controlled by hardware state machine, and the trigger condition of power layer change is the result of "Vision" detection. The EM9D core is placed in 2nd power layer to save main power consumption. Normally, EM9D core is in power shut-off state until 1st layer detection completed. There are hardware image accelerators in 1st layer to provide pre-processing of vision tasks and provide a wake-up trigger when event is detected. It can lower power consumption and maintain required response time and accuracy in "always-on" Computer Vision applications.

Security is a key consideration in Internet of Things and other embedded applications. HX6537/39/40-A provides hardware secure engine for secure boot, secure OTA firmware update, and secure meta data output with minimum processing latency. HX6537/39/40-A also provides rich peripheral interfaces for application need, including CMOS sensor interface, audio I^2S and PDM interface, and peripheral interfaces of UART, I^2C, SPI, GPIO and ADC.
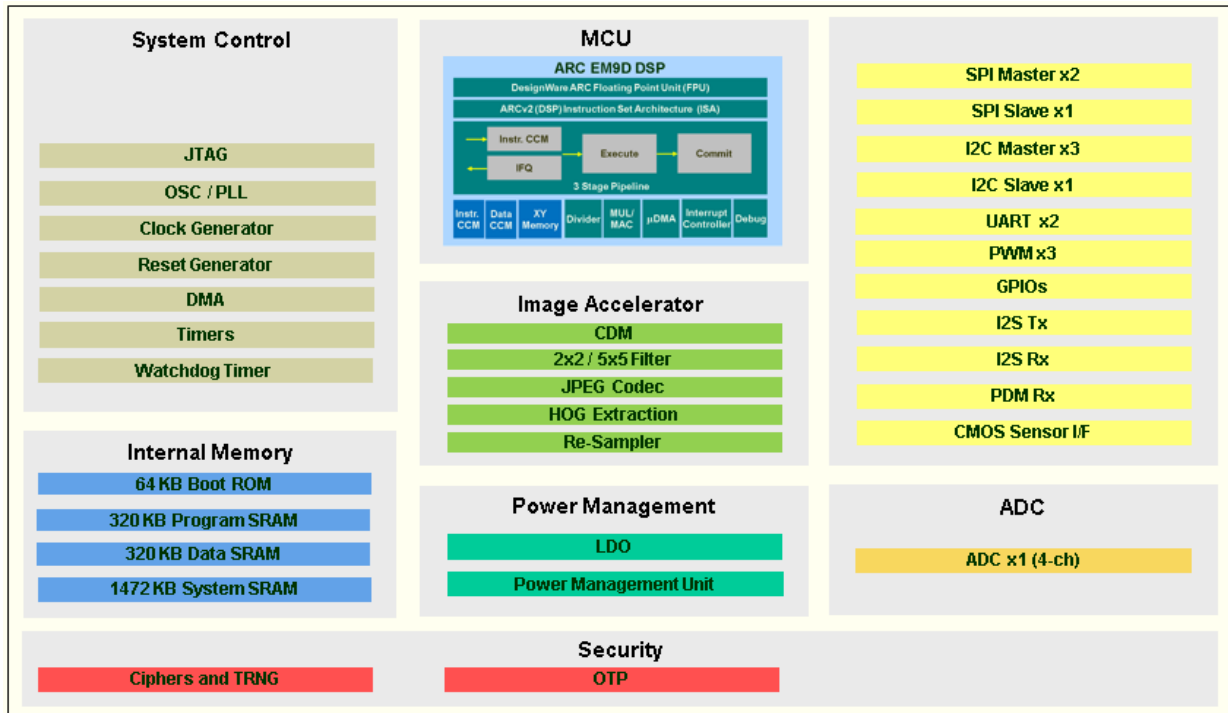
2. Features

- Ultra-low power and high-performance ARC EM9D DSP with FPU
  - 320 kB program ICCM local memory
  - 320 kB data DCCM/XCCM/YCCM local memory
  - 1472 kB system memory
  - 64 kB boot ROM
  - SIP 1MB/2MB Flash (LQFP/QFN packages only)
  - Frequency up to 400MHz
- Image hardware accelerators
  - Motion detection – Change Detection Module
  - 2x2 sub-sampler and filter
  - 5x5 de-mosaic and filter
  - JPEG codec
  - HOG extraction
  - Programmable re-sampler
- Security
  - True random number generator
  - Secure boot, secure OTA, secure meta data output
- Sensor input interface
  - 1/4/8-bit sensor interface
  - Up to 60fps@VGA
- Audio interface
  - PDM Rx for mono and stereo audio microphone input
  - I²S Rx/Tx for audio input and output
- Peripheral interfaces
  - 2x 1/2/4-bit SPI master, up to 50MHz
  - 1x SPI slave, up to 50MHz
  - 3x I²C master, up to 1MHz
  - 1x I²C slave, up to 1MHz
  - 2x UART interface with Tx and Rx FIFO
  - 3x PWM
  - GPIOs
- ADC interface
  - Up to 4-channels
  - 1x 12-bit 1 MSPS ADC
- Power management
  - Low power modes – Active, Standby, Sleep and Shutdown
  - Hardware Power Management Unit
  - SRAM retention to reduce EM9D startup time
- Debug mode
  - Two-wire JTAG interface
- Clock, reset and supply management
  - 1.8 V supply for core
  - 1.8 V to 3.3 V supply for I/Os
  - POR and BOR
  - 24 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Internal 36 MHz factory-trimmed RC oscillator
  - Internal 32 kHz RC oscillator with calibration

- Package
  - HX6537-A: QFN-72: 8 mm x 8 mm
  - HX6539-A: LQFP-128: 16 mm x 16 mm
  - HX6540-A: WLCSP-38: 4.695 mm x 1.604 mm

3. Block Diagram

Below diagram shows the functional modules in HX6537/39/40-A.

4. Information

Website:
https://www.himax.com.tw/products/intelligent-sensing/always-on-smart-sensing/

General information:
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