18 V, 12 A Step-Down Regulator with Programmable Current Limit

Data Sheet

ADP2389/ADP2390

FEATURES

- Input voltage: 4.5 V to 18 V
- Continuous output current: 12 A
- Integrated MOSFETs: 17 mΩ high-side/4.5 mΩ low-side
- 0.6 V ± 0.5% reference voltage
- Programmable switching frequency range: 200 kHz to 2200 kHz
- Enhanced transient response
- Programmable current limit with ±10% accuracy
- Precision enable and power good
- External compensation and soft start
- PFM mode (ADP2390 only)
- Start up into a precharged output
- Supported by the ADIsimPower design tool

APPLICATIONS

- Communication infrastructure
- Networking and servers
- Industrial and instrumentation
- Healthcare and medical
- Intermediate power rail conversions
- DC-to-DC point of load applications

TYPICAL APPLICATIONS CIRCUIT

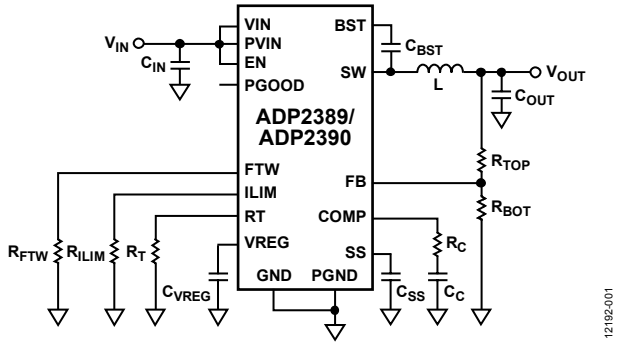

Figure 1.

GENERAL DESCRIPTION

The ADP2389/ADP2390 are current mode control, synchronous step-down, dc-to-dc regulators. They integrate a 17 mΩ high-side power MOSFET and a 4.5 mΩ synchronous rectifier MOSFET to provide a high efficiency solution. The ADP2390 operates in pulse frequency modulation (PFM) mode to improve the system efficiency at light load. The ADP2389/ADP2390 run from an input voltage of 4.5 V to 18 V and can deliver up to 12 A of output current. The output voltage can be adjusted to 0.6 V and the switching frequency can be programmed between 200 kHz to 2200 kHz.

The ADP2389/ADP2390 target high performance applications that require high efficiency and design flexibility. External compensation and soft start provide design flexibility. The power-good output and precision enable input provide simple and reliable power sequencing. An enhanced transient response feature improves the load transient performance, which reduces the output capacitance. Programmable current limit allows the user to optimized the inductor design and provide a compact solution.

Other key features include undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown (TSD).

The ADP2389/ADP2390 operates over a −40°C to +125°C junction temperature range and is available in 32-lead, 5 mm × 5 mm LFCSP package.

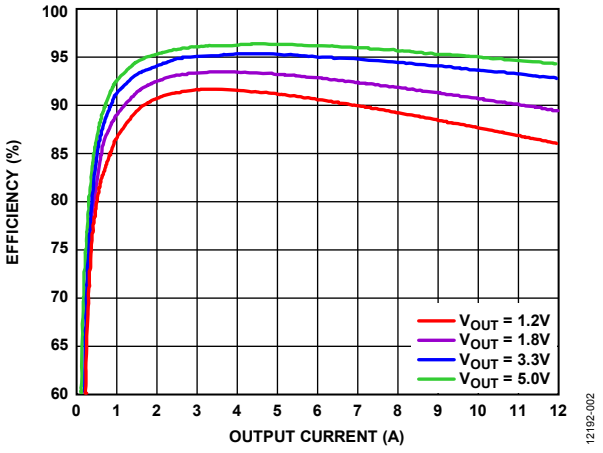

Figure 2. ADP2389 Efficiency vs. Output Current, V_{IN} = 12 V, f_{SW} = 300 kHz

Rev. 0 Document Feedback

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REVISION HISTORY

8/15—Revision 0: Initial Version

DETAILED FUNCTIONAL BLOCK DIAGRAM

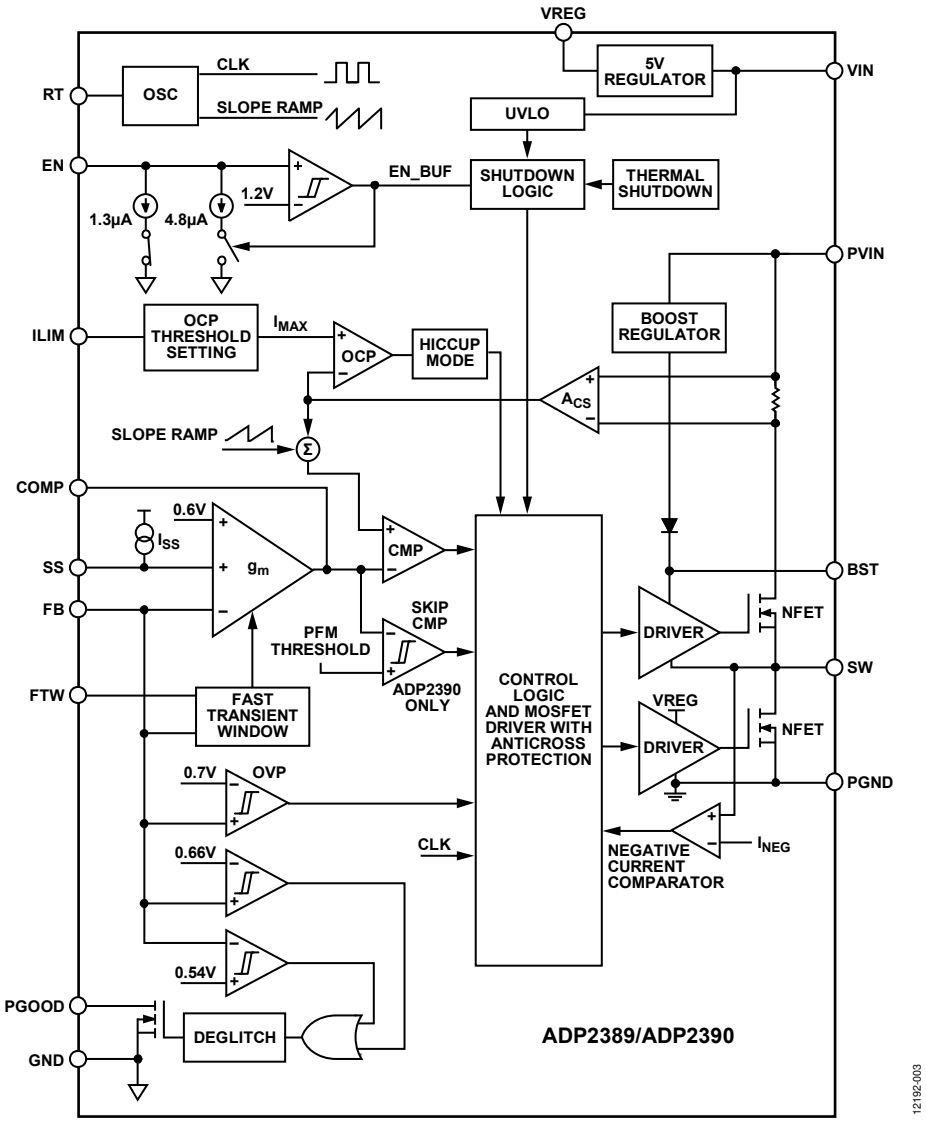

Figure 3. ADP2389/ADP2390 Detailed Functional Block Diagram

SPECIFICATIONS

V_{PVIN} = V_{VIN} = 12 V, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
SUPPLY VOLTAGE (PVIN AND VIN)						
PVIN Voltage Range	V_{PVIN}		4.5		18	V
VIN Voltage Range	V_{VIN}		4.5		18	V
Quiescent Current	I_Q	No switching		1.16	1.5	mA
Shutdown Current	I_{SHDN}	EN = GND		7.5	20	µA
VIN Undervoltage Lockout Threshold	UVLO	VIN rising		4.2	4.4	V
		VIN falling	3.5	3.7		V
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB}	0°C < T_J < 85°C	0.597	0.6	0.603	V
		−40°C < T_J < +125°C	0.594	0.6	0.606	V
FB Bias Current	I_{FB}			0.01	0.1	µA
ERROR AMPLIFIER (EA)						
Transconductance	g_m		450	500	550	µS
EA Source Current	I_{SOURCE}		40	50	60	µA
EA Sink Current	I_{SINK}		40	50	60	µA
INTERNAL REGULATOR (VREG)						
VREG Voltage	V_{VREG}	I_{VREG} = 10 mA	4.8	5	5.2	V
Dropout Voltage		I_{VREG} = 50 mA		355		mV
Regulator Current Limit				100		mA
SWITCH NODE (SW)						
On Resistance[1]						
High-Side	R_{DSON_H}	V_{BOOT} = 5 V		17	30	mΩ
Low-Side	R_{DSON_L}	V_{VREG} = 5 V		4.5	9	mΩ
SW Minimum On Time[2]	t_{MIN_ON}			100		ns
SW Minimum Off Time[2]	t_{MIN_OFF}			150		ns
CURRENT LIMIT						
ILIM Voltage	V_{ILIM}			0.592		V
ILIM Current Range	I_{ILIM}		1.8		12	µA
High-Side Peak Current Limit	I_{OCP}	R_{ILIM} = 59 kΩ	15	16.8	18.6	A
Low-Side Negative Current Limit[2]				4		A
BST						
Bootstrap Voltage	V_{BOOT}		4.6	5	5.4	V
OSCILLATOR (RT)						
Switching Frequency	f_{SW}	R_T = 100 kΩ	540	600	660	kHz
Switching Frequency Range			200		2200	kHz
FAST TRANSIENT WINDOW (FTW)						
Fast Transient Response Window		R_{FTW} = 100 kΩ		±2		%
Minimum Fast Transient Response Window[2]				±1		%
SS						
SS Pin Pull-Up Current	I_{SS}		2.7	3.4	4.1	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
PGOOD						
FB Threshold						
Rising			106	110	114	%
Falling			86	90	94	%
FB Hysteresis						
Rising				5		%
Falling				5		%
Power-Good Deglitch Time		PGOOD from low to high		16		Cycles
		PGOOD from high to low		16		Cycles
PGOOD Leakage Current		V_{PGOOD} = 5 V		0.01	0.1	µA
PGOOD Output Low Voltage		I_{PGOOD} = 1 mA		150	260	mV
EN						
EN Rising Threshold				1.2	1.28	V
EN Falling Threshold			1.02	1.1		V
EN Source Current		EN voltage < 1.1 V		6.1		µA
		EN voltage > 1.2 V		1.3		µA
THERMAL						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				25		°C

[1] Pin-to-pin measurement.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, VIN, EN, PGOOD	−0.3 V to +22 V
SW	−1 V to +22 V
BST	V_{SW} + 6 V
FB, SS, COMP, RT, ILIM, FTW, VREG	−0.3 V to +6 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Unless otherwise specified, all other voltages are referenced to GND.

THERMAL INFORMATION

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board (4-layer, JEDEC standard board) for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	41	2.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

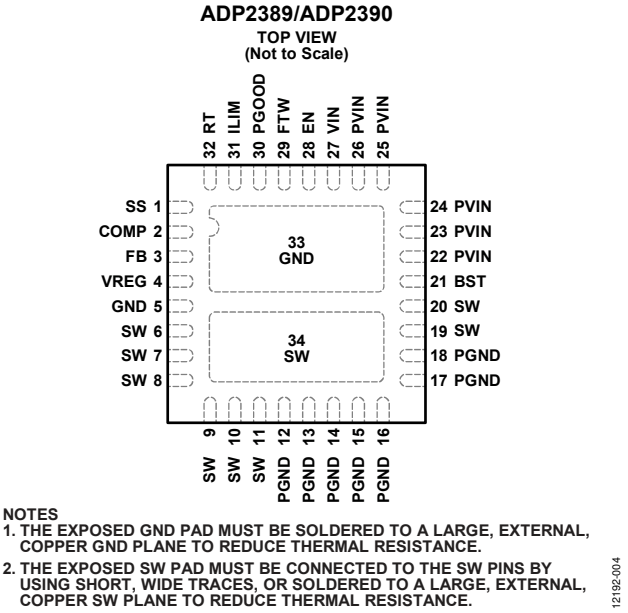

Figure 4. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SS	Soft Start Control. Connect a capacitor from the SS pin to GND to program the soft start time.
2	COMP	Error Amplifier Output. Connect an RC network from the COMP pin to GND.
3	FB	Feedback Voltage Sense Input. Connect this pin to a resistor divider from the output voltage, V_{OUT}.
4	VREG	Output of the Internal 5 V Regulator. The control circuits are powered from this voltage. Place a 1 µF, X7R or X5R ceramic capacitor between this pin and GND.
5	GND	Analog Ground.
6 to 11, 19, 20	SW	Switch Node. Connect this pin to an inductor.
12 to 18	PGND	Power Ground. Return of the low-side MOSFET.
21	BST	Supply Rail for the High-Side Gate Drive. Place a 0.1 µF, X7R or X5R capacitor between SW and BST.
22 to 26	PVIN	Power Input. Connect PVIN to the input power source and connect a bypass capacitor between this pin and PGND.
27	VIN	Power Input for Control Circuitry. Bypass VIN to GND with a low equivalent series resistance (ESR) capacitor as close to the device as possible. Connect VIN to PVIN directly.
28	EN	Precision Enable. Use an external resistor divider to set the turn on threshold. To enable the device automatically, connect the EN pin to PVIN.
29	FTW	Fast Transient Response Window Setting. Connect a resistor between the FTW pin and GND to set the fast transient response window.
30	PGOOD	Power-Good Output (Open-Drain). Connecting a 10 kΩ to 100 kΩ pull-up resistor from PGOOD to a pull-up voltage is recommended.
31	ILIM	Current-Limit Threshold Setting. Connect a resistor from the ILIM pin to GND to program the current-limit threshold.
32	RT	Frequency Setting. Connect a resistor between the RT pin and GND to program the switching frequency between 200 kHz to 2.2 MHz.
33	EP, GND	Exposed GND Pad. The exposed GND pad must be soldered to a large, external, copper GND plane to reduce thermal resistance.
34	EP, SW	Exposed SW Pad. The exposed SW pad must be connected to the SW pins by using short, wide traces, or soldered to a large, external, copper SW plane to reduce thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{PVIN} = V_{VIN} = 12 V, V_{OUT} = 1.8 V, L = 1 µH, C_{OUT} = 5 × 100 µF, f_{SW} = 500 kHz, unless otherwise noted.

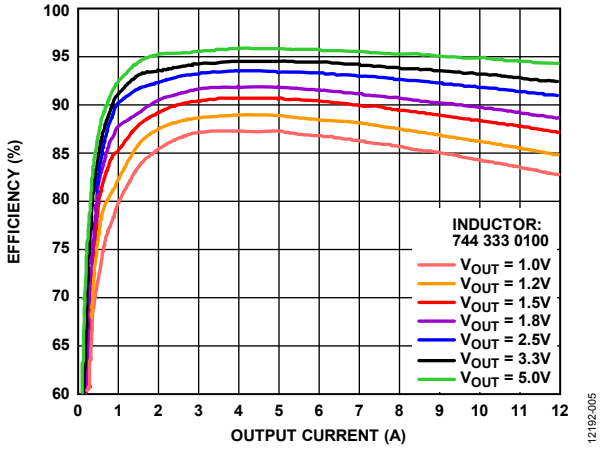

Figure 5. ADP2389 Efficiency at V_{PVIN} = 12 V, f_{SW} = 600 kHz

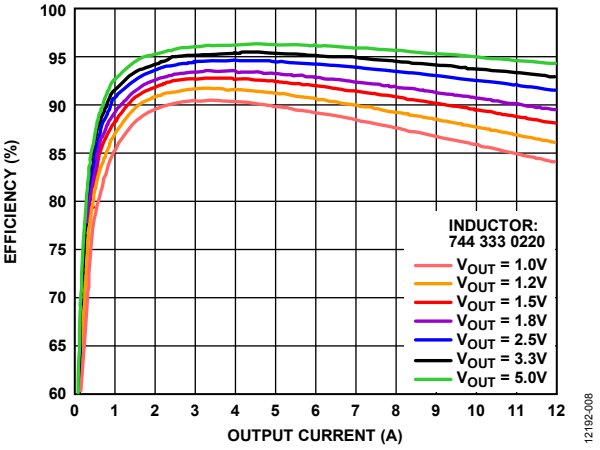

Figure 8. ADP2389 Efficiency at V_{PVIN} = 12 V, f_{SW} = 300 kHz

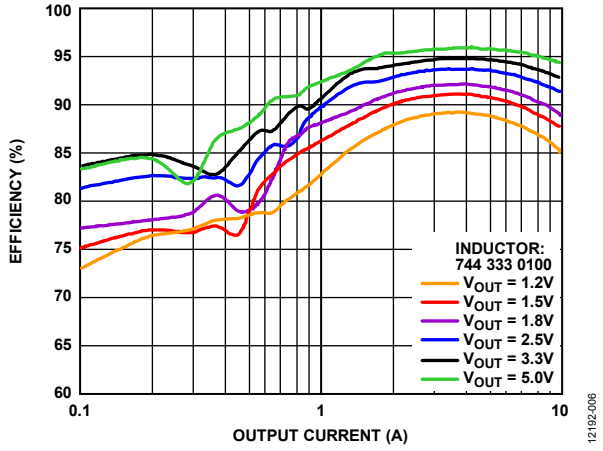

Figure 6. ADP2390 Efficiency at V_{PVIN} = 12 V, f_{SW} = 600 kHz

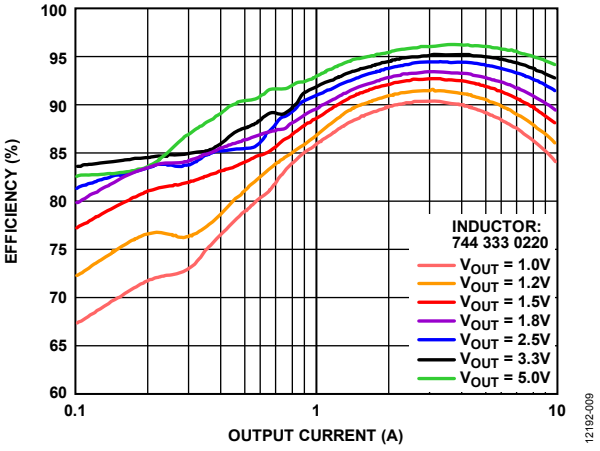

Figure 9. ADP2390 Efficiency at V_{PVIN} = 12 V, f_{SW} = 300 kHz

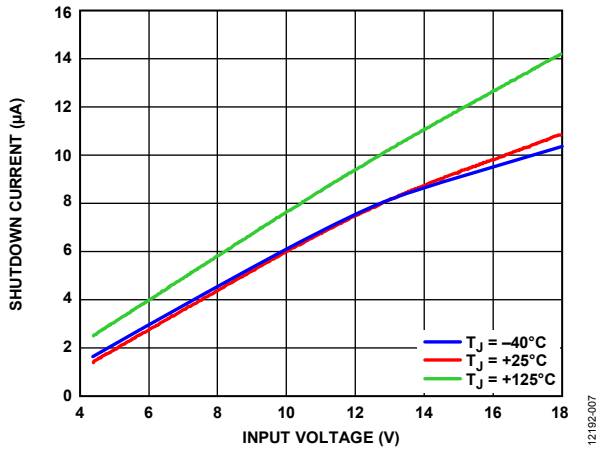

Figure 7. Shutdown Current (I_{SHDN}) vs. Input Voltage

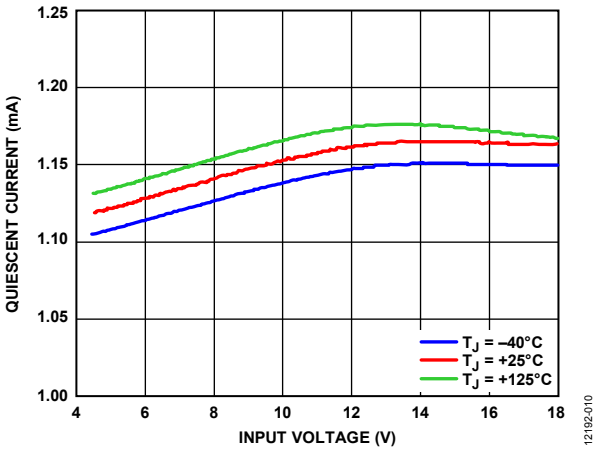

Figure 10. Quiescent Current (I_Q) vs. Input Voltage

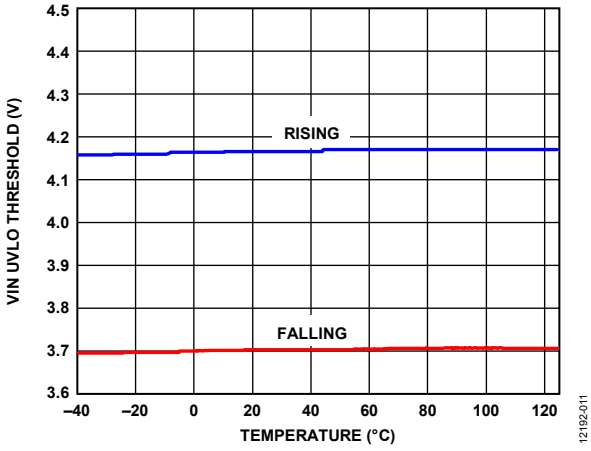

Figure 11. VIN UVLO Threshold vs. Temperature

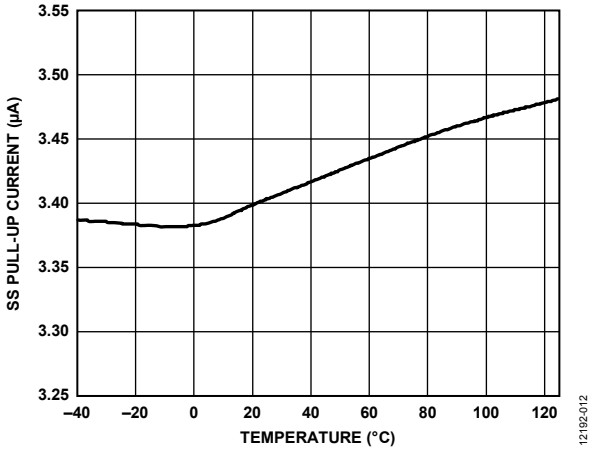

Figure 12. SS Pin Pull-Up Current vs. Temperature

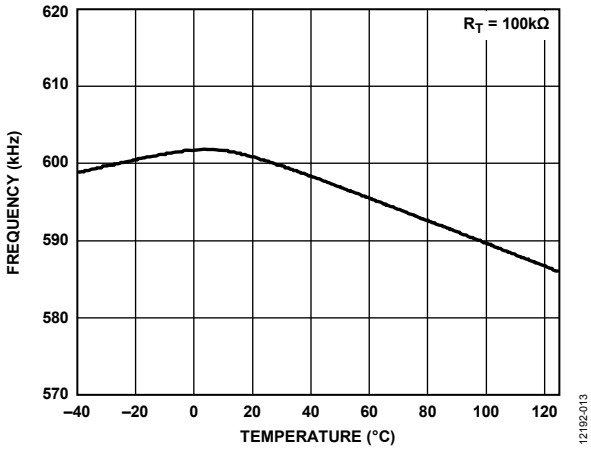

Figure 13. Frequency vs. Temperature

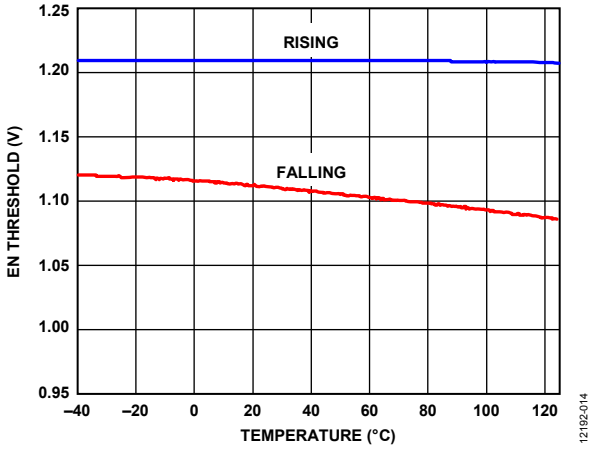

Figure 14. EN Threshold vs. Temperature

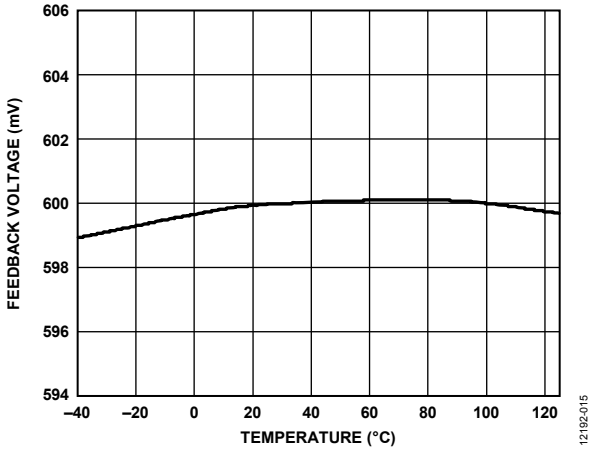

Figure 15. Feedback Voltage vs. Temperature

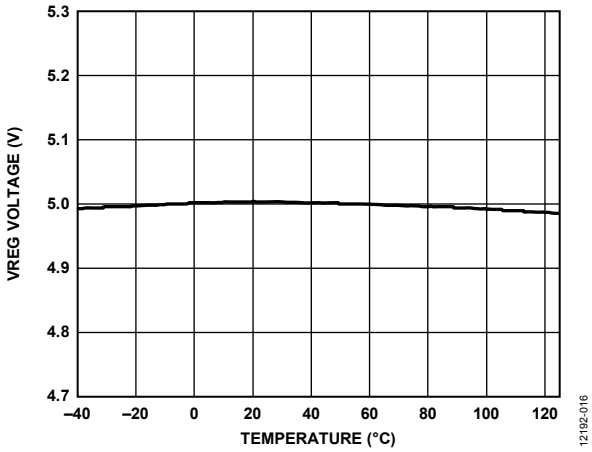

Figure 16. VREG Voltage vs. Temperature

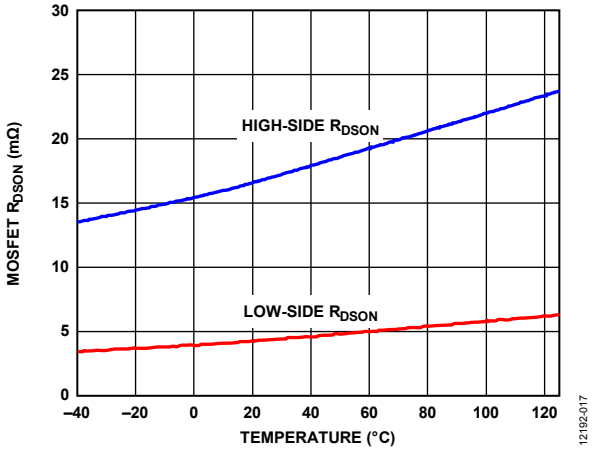

Figure 17. MOSFET R_{DSON} vs. Temperature

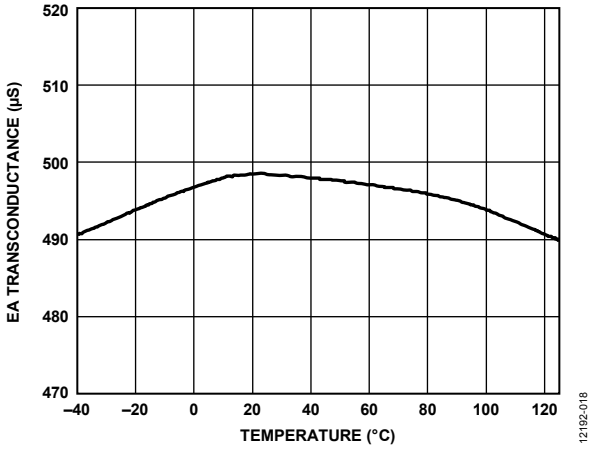

Figure 18. EA Transconductance vs. Temperature

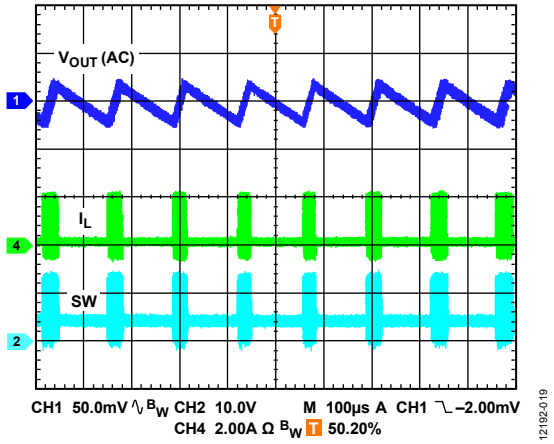

Figure 19. PFM Mode Waveform (ADP2390)

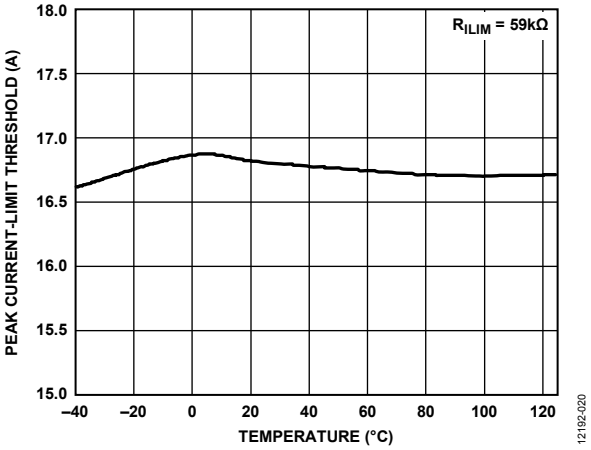

Figure 20. Peak Current-Limit Threshold vs. Temperature

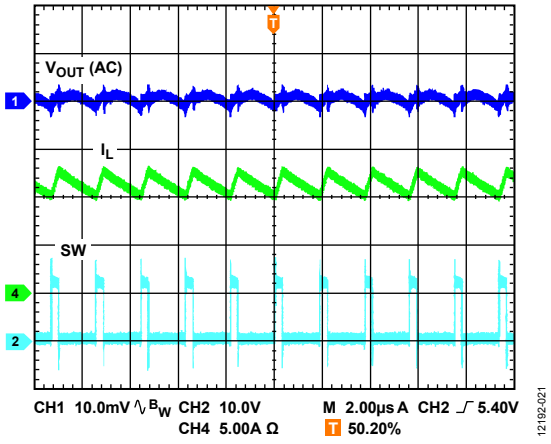

Figure 21. Continuous Conduction Mode (CCM) Waveform

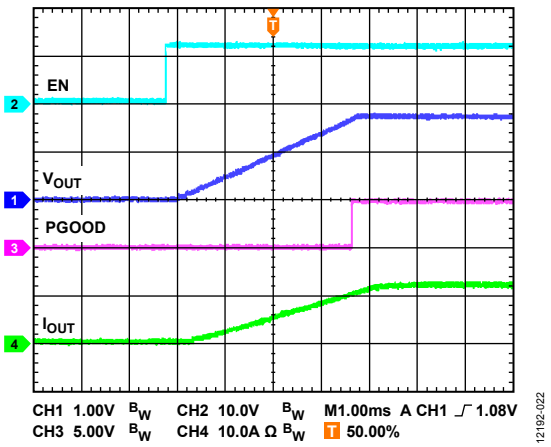

Figure 22. Soft Start with Full Load

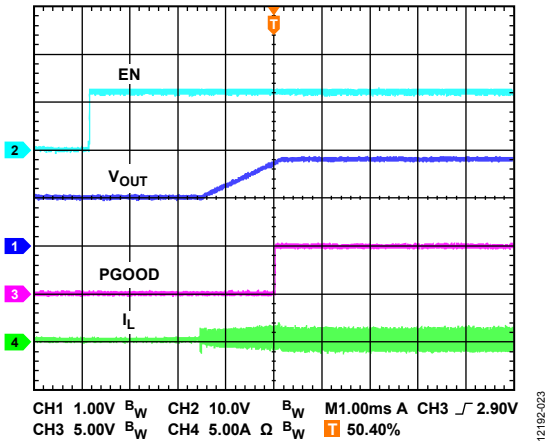

Figure 23. Precharged Output

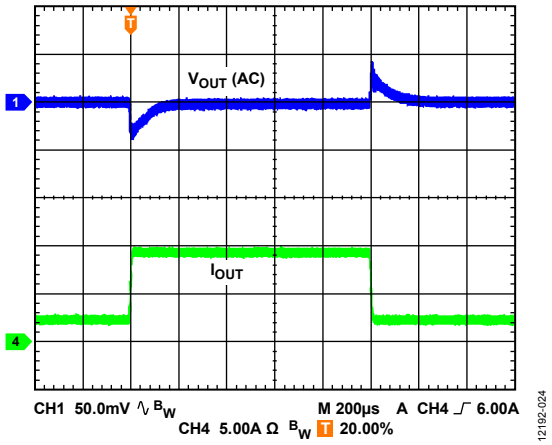

Figure 24. Load Transient Response with Fast Transient Enable, I_{OUT} = 2.4 A to 9.6 A

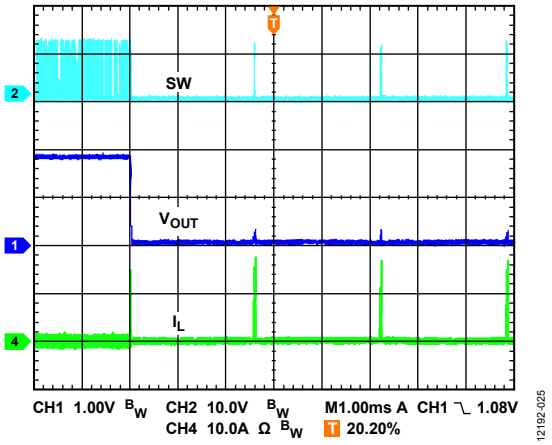

Figure 25. Output Short Entry

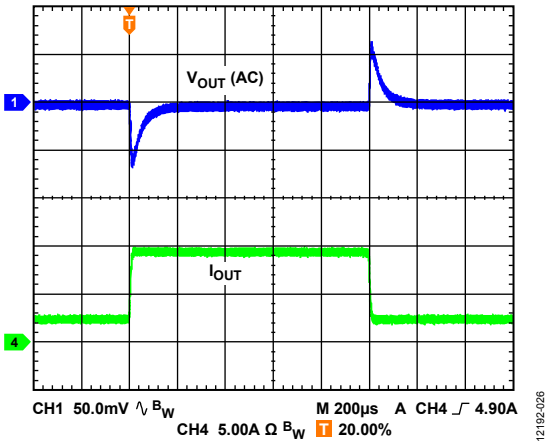

Figure 26. Load Transient Response, I_{OUT} = 2.4 A to 9.6 A

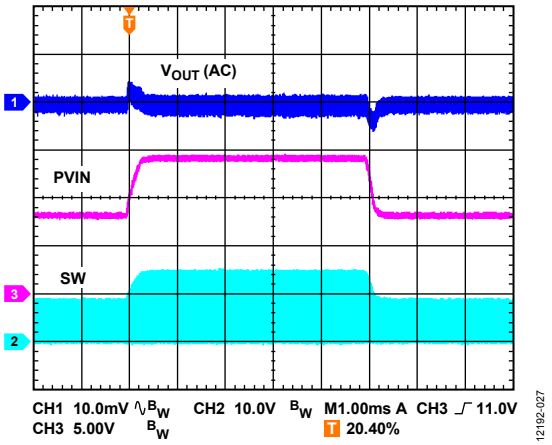

Figure 27. Line Transient Response, V_{PVIN} from 8 V to 14 V, I_{OUT} = 12 A

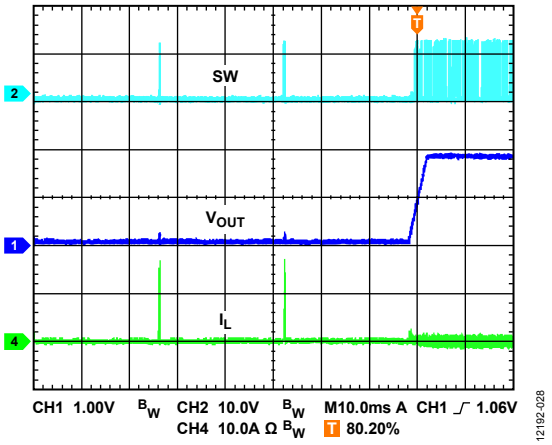

Figure 28. Output Short Recovery

THEORY OF OPERATION

The ADP2389/ADP2390 are synchronous step-down, dc-to-dc regulators. These devices use a current-mode control architecture with an integrated high-side power switch and a low-side synchronous rectifier. The regulators target high performance applications that require high efficiency and design flexibility.

The ADP2389/ADP2390 can operate with an input voltage from 4.5 V to 18 V and can regulate the output voltage to 0.6 V. Additional features added for design flexibility include programmable switching frequency, programmable soft start, programmable current limit, external compensation, precision enable, and a power-good output.

CONTROL SCHEME

The ADP2389/ADP2390 use a fixed frequency, peak current mode pulse-width modulation (PWM) control architecture. At the start of each oscillator cycle, the high-side MOSFET turns on, adding a positive voltage across the inductor. The current in the inductor (I_L) increases until the current sense signal crosses the peak inductor current threshold that turns off the high-side MOSFET and turns on the low-side MOSFET. This action adds a negative voltage across the inductor, causing the inductor current to decrease. The low-side MOSFET remains on for the rest of cycle.

PFM MODE (ADP2390 ONLY)

The ADP2390 can work in PFM mode during a light load. When the COMP pin voltage is below the PFM threshold voltage, the device enters PFM mode. In PFM mode, the device monitors the FB voltage to regulate the output voltage. Because the high-side and low-side MOSFETs are turned off, the load current discharges the output capacitor, causing the output voltage to drop. When the FB voltage drops below 0.605 V, the device begins switching and the output voltage increases as the output capacitor is charged by the inductor current. When the FB voltage exceeds 0.62 V, the device turns off both the high-side and low-side MOSFETs until the FB voltage drops to 0.605 V. In the PFM mode, the output voltage ripple is greater than the ripple in the PWM mode.

PRECISION ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.2 V (typical) with 100 mV of hysteresis. When the enable pin (EN) voltage exceeds 1.2 V, the regulator turns on; when it falls below 1.1 V (typical), the regulator turns off. To force the regulator to start automatically when input power is applied, connect the EN pin to PVIN.

The precision EN pin has an internal pull-down current source (5 µA) that provides a default turn off when the EN pin is open.

When the EN pin voltage exceeds 1.2 V (typical), the ADP2389/ADP2390 are enabled and the internal pull-down current source at the EN pin decreases to 1 µA, which allows users to program the PVIN UVLO and hysteresis.

INTERNAL REGULATOR (VREG)

The on-board regulator provides a stable supply for the internal circuits. Place a 1 µF, X7R or X5R ceramic capacitor between the VREG pin and GND. The internal regulator includes a current-limit circuit to protect the output if the maximum external load current is exceeded.

BOOTSTRAP CIRCUITRY

The ADP2389/ADP2390 include a boot strap regulator to provide the gate drive voltage for the high-side MOSFET. The boot strap regulator uses differential sensing to generate a 5 V bootstrap voltage between the BST pin and the SW pin.

Place a 0.1 µF, X7R or X5R ceramic capacitor between the BST pin and the SW pin.

OSCILLATOR

The switching frequency of the ADP2389/ADP2390 (f_{SW}) is controlled by the RT pin. A resistor (R_T) from the RT pin to GND can program the switching frequency according to the following equation:

$$f_{SW}\,(\text{kHz}) = \frac{67{,}000}{R_T\,(\text{k}\Omega) + 12}$$

A 100 kΩ resistor sets the switching frequency to 600 kHz, and a 44.2 kΩ resistor sets the switching frequency to 1.2 MHz. Figure 29 shows the typical relationship between f_{SW} and R_T.

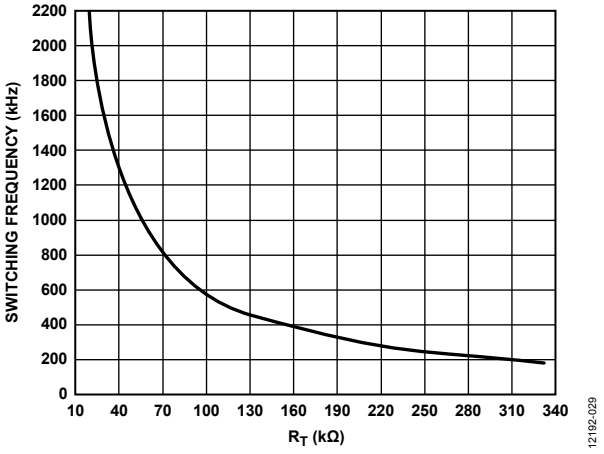

Figure 29. Switching Frequency (f_{SW}) vs. R_T

SOFT START

The SS pin programs the soft start time. Place a capacitor between the SS pin and GND; an internal current charges this capacitor to establish the soft start ramp. Calculate the soft start time using the following equation:

$$t_{SS} = \frac{0.6\ V \times C_{SS}}{I_{SS}}$$

where:
C_{SS} is the soft start capacitance.
I_{SS} is the soft start pull-up current (3.4 µA).

If the output voltage is precharged before power-up, the ADP2389/ADP2390 prevent the low-side MOSFET from turning on until the soft start voltage exceeds the voltage on the FB pin.

FAST TRANSIENT RESPONSE

The ADP2389/ADP2390 use the FTW pin to set the fast transient response window. Place a resistor (R_{FTW}) between the FTW pin and GND to program the window. Calculate the window threshold using the following equation:

$$Window\ Threshold = \frac{200}{R_{FTW}(\text{k}\Omega) + 1}\%$$

If the output voltage is greater than the setting window, the fast transient response is enabled. The fast transient response function is disabled if the FTW pin is open and the minimum window is 1%.

To avoid false trigger of the fast transient, the window threshold must be 2× greater than the output ripple.

POWER GOOD

The power-good (PGOOD) pin is an active high, open-drain output that requires an external resistor to pull it up to a voltage. A logic high on the PGOOD pin indicates that the voltage at the FB pin (and thus the output voltage) is within ±10% of the desired value, and there is a 16 cycle waiting period before PGOOD is pulled high. A logic low indicates that the voltage at the FB pin is out of ±10% of the desired value, and there is a 16-cycle waiting period before PGOOD is pulled low.

PEAK CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2389/ADP2390 have a cycle-by-cycle peak current-limit protection circuit to prevent current runaway. A resistor (R_{ILIM}) from the ILIM pin to GND programs the peak current-limit threshold according to the following equation:

$$I_{OCP}\ (\text{A}) = \frac{1000}{R_{ILIM}(\text{k}\Omega) + 0.5}$$

For protection against heavy loads, the ADP2389/ADP2390 use a hiccup mode for overcurrent protection. When the inductor T turns off and the low-side MOSFET turns on until the next cycle. The overcurrent counter increments during this process. If the overcurrent counter reaches four or the FB pin voltage falls to 0.2 V after the soft start, the device enters hiccup mode. During hiccup mode, the high-side MOSFET and the low-side both turn off. The device remains in this mode for seven soft start times and then attempts to restart from soft start. If the current-limit fault is cleared, the device resumes normal operation; otherwise, it reenters hiccup mode.

In some cases, the input voltage (PVIN) ramp rate is too slow, or the output capacitor is too large for the output to reach regulation during the soft start process, which causes the regulator to enter hiccup mode. To avoid such cases, use a resistor divider at the EN pin to program the input voltage UVLO, or use a longer soft start time.

OVERVOLTAGE PROTECTION (OVP)

The ADP2389/ADP2390 include an OVP feature that protects the regulator against an output short to a higher voltage supply or against a strong load disconnect transient. If the feedback voltage increases to 0.7 V, the internal high-side MOSFET and low-side MOSFET turn off until the voltage at FB decreases to 0.63 V. At that time, the ADP2389/ADP2390 resumes normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout (UVLO) threshold is 4.2 V with a 0.5 V hysteresis, which prevents power-on glitches from occurring. When the VIN voltage rises above 4.2 V, the device enables and the soft start period initiates. When the VIN voltage drops below 3.7 V, the device turns off.

THERMAL SHUTDOWN

In the event that the ADP2389/ADP2390 junction temperatures rises above 150°C, the internal thermal shutdown circuit turns off the regulator for self protection. Extreme junction temperatures can be the result of high current operation, poor circuit board thermal design, and/or high ambient temperature. A 25°C hysteresis is included in the thermal shutdown circuit so that if an overtemperature event occurs, the ADP2389/ADP2390 does not return to normal operation until the on-chip temperature drops below 125°C. Upon recovery, a soft start initiates before normal operation.

APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input. This capacitor must be a ceramic type in the range of 10 µF to 47 µF. Place the capacitor close to the PVIN pin. Keep the loop composed by this input capacitor, high-side MOSFET and low-side MOSFET as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor must be larger than the value calculated from the following equation:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

where:
I_{OUT} is the output current.
D is the duty cycle.

OUTPUT VOLTAGE SETTING

An external resistor divider sets the output voltages of the ADP2389/ADP2390. Calculate the resistor values using the following equation:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

where :
R_{TOP} is the top feedback resistor.
R_{BOT} is the bottom feedback resistor.

To limit output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} is less than 30 kΩ.

Table 5 gives the recommended resistor divider for various output voltages.

Table 5. Resistor Divider for Difference Output Voltage

V_{OUT} (V)	R_{TOP}, ±1% (kΩ)	R_{BOT}, ±1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21
5.0	22	3

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, the input voltage, output voltage, and inductor ripple current. Using a small inductor leads to a faster transient response; however, it degrades efficiency due to its larger inductor ripple current. Using a large inductor value leads to smaller ripple current and better efficiency but results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L, is typically set to one third of the maximum load current. Calculate the inductor value using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
D is the duty cycle.
ΔI_L is the inductor ripple current.
f_{SW} is the switching frequency.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The peak inductor current (I_{PEAK}) is calculated using

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be greater than the peak inductor current. For the ferrite core inductors with a quick saturation characteristic, the saturation current rating (I_{SAT}) of the inductor must be greater than the current-limit threshold of the switch to prevent the inductor from being saturated.

Calculate the rms current of the inductor (I_{RMS}) from the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low electromagnetic interference (EMI). Table 6 lists recommended inductors.

Table 6. Recommended Inductors

Vendor	Device No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)
CoilCraft	XAL7030-102ME	1	21.8	16.1	4.55
	XAL7030-152ME	1.5	11.9	23.5	7.6
	XAL7030-222ME	2.2	10	18	13.7
Toko	FDUE1040D-H-R22M	0.22	32	32	0.64
	FDUE1040D-H-R45M	0.45	27	24	1.02
	FDU1040D-H-R68M	0.68	21	20	1.7
	FDUE1040D-H-1R0M	1.0	18	16	2.35
	FDA1254-H-1R2M	1.2	20.2	18.4	2.6
Würth Elektronik	744 333 0022	0.22	60	21.5	0.6
	744 333 0047	0.47	47	20	0.8
	744 333 0068	0.68	38	20	1.35
	744 333 0082	0.82	36	20	1.35
	744 332 0100	1.0	27.5	20	1.35
	744 325 120	1.2	25	20	1.8
	744 333 0150	1.5	27	18	2.5
	744 333 0220	2.2	22	16	3.7

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output ripple voltage and the loop dynamics of the regulator.

During a step load transient, for instance, when the load is suddenly increased, the output capacitor supplies the load until the control loop ramps up the inductor current. The delay caused by the control loop causes the output to undershoot. Use the following equation to calculate the output capacitance required to satisfy the voltage droop requirement:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor; the typical setting is K_{UV} = 2.
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

When a load is suddenly removed from the output and the energy stored in the inductor rushes into the output capacitor, the output overshoots. Calculate the output capacitance required to meet the overshoot requirement using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{OUT} - \Delta V_{OUT\_OV}) - V_{OUT}}$$

where:
K_{OV} is a factor; the typical setting is K_{OV} = 2.
ΔI_{STEP} is the load step.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The output ripple is determined by the ESR and the value of the capacitance. Use the following equations to select a capacitor that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

where ΔV_{OUT_RIPPLE} is the allowable output ripple voltage.

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where R_{ESR} is the equivalent series resistance of the output capacitor in ohms.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple performance.

The selected output capacitor voltage rating must be greater than the output voltage. The rms current rating of the output capacitor must be greater than the value calculated using the following equation:

$$I_{COUT\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

PROGRAMMING INPUT VOLTAGE UVLO

The ADP2389/ADP2390 have a precision enable input that programs the UVLO threshold of the input voltage, as shown in Figure 30.

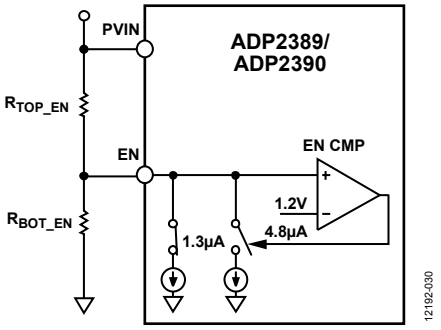

Figure 30. Programming the Input Voltage UVLO

Use the following equations to calculate R_{TOP_EN} and R_{BOT_EN}:

$$R_{TOP\_EN} = \frac{1.1\ \text{V} \times V_{IN\_RISING} - 1.2\ \text{V} \times V_{IN\_FALLING}}{1.1\ \text{V} \times 6.1\ \mu\text{A} - 1.2\ \text{V} \times 1\ \mu\text{A}}$$

where:
V_{IN_RISING} is the V_{IN} rising threshold.
$V_{IN\_FALLING}$ is the V_{IN} falling threshold.

$$R_{BOT\_EN} = \frac{1.2\ \text{V} \times R_{TOP\_EN}}{V_{IN\_RISING} - R_{TOP\_EN} \times 6.1\ \mu\text{A} - 1.2\ \text{V}}$$

COMPENSATION DESIGN

For peak current mode control, the power stage can be simplified as a voltage controlled current source supplying current to the output capacitor and load resistor. It is composed of one domain pole and a zero contributed by the output capacitor ESR. The control to output transfer function is shown with the following equations:

$$G_{VD}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_Z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_P}\right)}$$

where:
G_{VD} is the control to output transfer function.
A_{VI} = 20 A/V.
R is the load resistance.
f_Z is the zero of G_{VD}.
f_P is the domain pole of G_{VD}.

$$f_Z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

where:
R_{ESR} is the equivalent series resistance of the output capacitor.
C_{OUT} is the output capacitance.

$$f_P = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

The ADP2389/ADP2390 use a transconductance amplifier for the error amplifier and to compensate the system. Figure 31 shows the simplified, peak current mode control, small signal circuit.

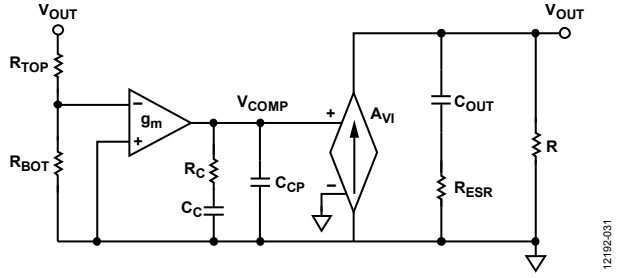

Figure 31. Simplified Peak Current Mode Control, Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero and the optional C_{CP} and R_C contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_P} \times s\right)} \times G_{VD}(s)$$

The following design guideline shows how to select the compensation components R_C, C_C, and C_{CP} for ceramic output capacitor applications.

1. Determine the cross frequency, f_C. Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6\ \text{V} \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole, f_P, and determine C_C by

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. Use C_{CP} to cancel the zero caused by the ESR of the output capacitor.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

DESIGN EXAMPLE

This section provides the procedures of selecting the external components based on the example specifications listed in Table 7. The schematic of this design example is shown in Figure 32.

Table 7. Step-Down DC-to-DC Regulator Requirements

Parameter	Specification
Input Voltage	12.0 V ± 10%
Output Voltage	1.2 V
Output Current	12 A
Output Voltage Ripple	12 mV
Load Transient	±5%, 3 A to 9 A, 2 A/µs
Switching Frequency	500 kHz

OUTPUT VOLTAGE SETTING

Select a 10 kΩ resistor as the top feedback resistor (R_{TOP}) and calculate the bottom feedback resistor (R_{BOT}) using the following equation:

$$R_{BOT} = R_{TOP} \times \left(\frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 1.2 V, the resistors values are R_{TOP} = 10 kΩ and R_{BOT} = 10 kΩ.

FREQUENCY SETTING

Use the following equation to calculate the value of R_T:

$$R_T(\text{k}\Omega) = \frac{67,000}{f_{SW}(\text{kHz})} - 12$$

Thus, when f_{SW} = 500 kHz, the value of R_T = 122 kΩ.

Select the standard resistor value of 121 kΩ for R_T.

INDUCTOR SELECTION

The peak-to-peak inductor ripple current, ΔI_L, is set to 33% of the maximum output current. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} = 12.0 V
V_{OUT} = 1.2 V
D = 10%
ΔI_L = 4 A
f_{SW} = 500 kHz

This results in L = 0.54 µH. Select the standard inductor value of 0.68 µH.

Calculate the peak-to-peak inductor ripple current using the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

This results in ΔI_L = 3.176 A.

Calculate the peak inductor current with the following equation:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

This results in I_{PEAK} = 13.588 A.

Calculate the rms current flowing through the inductor by the following equation:

$$I_{RMS} = \sqrt{{I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}}$$

This results in I_{RMS} = 12.035 A.

According to the calculated current value, select an inductor with a minimum rms current rating of 12.035 A and a minimum saturation current rating of 13.588 A.

However, to protect the inductor from reaching its saturation point under a current-limit condition, the inductor must be rated for at least a 20 A saturation current for reliable operation.

Based on these requirements, select a 0.68 µH inductor, such as the 7443330068 from Würth Elektronik, which has 1.35 mΩ dc resistance (DCR) and a 38 A saturation current.

OUTPUT CAPACITOR SELECTION

The output capacitor must meet both the output voltage ripple requirement and load transient response.

To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance value of the output capacitor:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

This results in C_{OUT_RIPPLE} = 66 µF and R_{ESR} = 3.78 mΩ.

To meet the ±5% overshoot and undershoot transient requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_OV} = \frac{K_{OV} \times {\Delta I_{STEP}}^2 \times L}{2 \times (V_{OUT} - \Delta V_{OUT\_OV}) - V_{OUT}}$$

$$C_{OUT\_UV} = \frac{K_{UV} \times {\Delta I_{STEP}}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
$K_{OV} = K_{UV}$ = 2, and are the coefficients for estimation purpose.
ΔI_{STEP} = 6 A, and is the load transient step.
ΔV_{OUT_OV} = 5% × V_{OUT} and, is the overshoot voltage.
ΔV_{OUT_UV} = 5% × V_{OUT}, and is the undershoot voltage.

This results in C_{OUT_OV} = 332 µF and C_{OUT_UV} = 38 µF.

According to the calculations for C_{OUT_RIPPLE}, C_{OUT_OV}, and C_{OUT_UV}, the output capacitance must be greater than 332 µF and the ESR of the output capacitor must be less than 3.78 mΩ. It is recommended that five 100 µF, X5R, 6.3 V ceramic capacitors be used, such as the GRM32ER60J107ME20 from Murata, with an ESR of 2 mΩ.

COMPENSATION COMPONENTS

For better load transient and stability performance, set the cross frequency, f_C, to $f_{SW}/10$. In this case, f_{SW} is running at 500 kHz; therefore, set f_C to 50 kHz.

The 100 µF ceramic output capacitors have a derated value of 62 µF.

$$R_C = \frac{2 \times \pi \times 1.2\ \text{V} \times 5 \times 62\ \mu\text{F} \times 50\ \text{kHz}}{0.6\ \text{V} \times 500\ \mu\text{S} \times 20\ \text{A/V}} = 19.47\ \text{k}\Omega$$

$$C_C = \frac{(0.1\ \Omega + 0.002\ \Omega) \times 5 \times 62\ \mu\text{F}}{19.47\ \text{k}\Omega} = 1623\ \text{pF}$$

$$C_{CP} = \frac{0.002\ \Omega \times 5 \times 62\ \mu\text{F}}{19.47\ \text{k}\Omega} = 31.8\ \text{pF}$$

Choose the following standard components: R_C = 20 kΩ, C_C = 1500 pF, and C_{CP} = 33 pF.

SCHEMATIC FOR DESIGN EXAMPLE

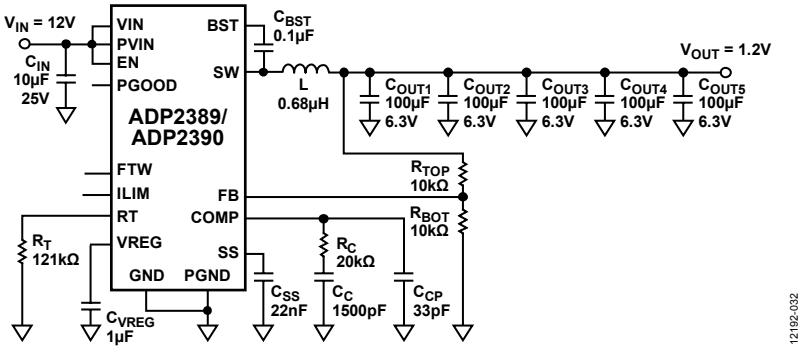

Figure 32. Schematic for Design Example

SOFT START TIME PROGRAM

The soft start feature ramps up the output voltage in a controlled manner, eliminating output voltage overshoot during soft start, and limiting the inrush current. Set the soft start time to 4 ms.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{0.6\ \text{V}} = \frac{4\ \text{ms} \times 3.4\ \mu\text{A}}{0.6\ \text{V}} = 22.67\ \text{nF}$$

Choose a standard component value of C_{SS} = 22 nF.

INPUT CAPACITOR SELECTION

Place a minimum 10 µF ceramic capacitor near the PVIN pin. In this application, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

EXTERNAL COMPONENTS RECOMMENDATION

Table 8. Recommended External Components for Typical Applications with 10 A Output Current

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	C_{CP} (pF)
300	12	1	0.82	680	10	15	21	2700	330
	12	1.2	1	470	10	10	18	2700	270
	12	1.5	1	5 × 100	15	10	15	2700	39
	12	1.8	1.2	5 × 100	20	10	18	2700	33
	12	2.5	1.5	3 × 100	47.5	15	15	2700	22
	12	3.3	2.2	3 × 100	10	2.21	20	2700	18
	12	5	2.2	100	22	3	10	2700	10
	5	1	0.68	470	10	15	15	2700	330
	5	1.2	0.82	470	10	10	18	2700	270
	5	1.5	0.82	5 × 100	15	10	12	2700	39
	5	1.8	1	4 × 100	20	10	15	2700	33
	5	2.5	1	2 × 100	47.5	15	10	2700	22
	5	3.3	1	2 × 100	10	2.21	12	2700	18
600	12	1.2	0.47	4 × 100	10	10	18	1200	27
	12	1.5	0.47	3 × 100	15	10	18	1200	22
	12	1.8	0.68	3 × 100	20	10	21	1200	18
	12	2.5	0.82	2 × 100	47.5	15	20	1200	12
	12	3.3	1	100	10	2.21	12	1200	10
	12	5	1.2	100	22	3	20	1200	6.8
	5	1	0.47	5 × 100	10	15	20	1200	33
	5	1.2	0.47	4 × 100	10	10	18	1200	27
	5	1.5	0.47	3 × 100	15	10	18	1200	22
	5	1.8	0.47	2 × 100	20	10	14	1200	18
	5	2.5	0.47	100	47.5	15	10	1200	12
	5	3.3	0.47	100	10	2.21	12	1200	10
1200	12	2.5	0.47	100	47.5	15	20	680	6.8
	12	3.3	0.47	47	10	2.21	12	680	4.7
	12	5	0.68	47	22	3	18	680	3.3
	5	1	0.13	2 × 100	10	15	15	680	12
	5	1.2	0.24	2 × 100	10	10	18	680	12
	5	1.5	0.24	2 × 100	15	10	22.1	680	10
	5	1.8	0.24	100	20	10	14	680	8.2
	5	2.5	0.24	47	47.5	15	9.1	680	6.8
	5	3.3	0.24	47	10	2.21	12	680	4.7

[1] 680 µF: 6.3 V, KEMET T530X687M006ATE010; 470 µF: 6.3 V, KEMET T520X477M006ATE010; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; 47 µF: 6.3 V, X5R, Murata GRM32ER60J476ME20.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good printed circuit board (PCB) layout is essential for obtaining the best performance from the ADP2389/ADP2390. Poor PCB layout can degrade the output regulation, as well as the EMI and electromagnetic compatibility (EMC) performance. Figure 34 shows an example of a good PCB layout for the ADP2389/ADP2390. For optimum layout, refer to the following guidelines:

- Use separate analog ground planes and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to the analog ground. In addition, connect the ground reference of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed GND pad of the ADP2389/ADP2390.
- Place the input capacitor, the inductor, and the output capacitor as close as possible to the IC, and use short traces.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane.
  In addition, ensure that the high current path from the power ground plane through the inductor and output capacitor back to the power ground plane is as short as possible by tying the PGND pins of the ADP2389/ADP2390 to the PGND plane as close as possible to the input and output capacitors.
- Connect the exposed GND pad of the ADP2389/ADP2390 to a large, external copper ground plane to maximize its power dissipation capability and minimize junction temperature. In addition, connect the exposed SW pad to the SW pins of the ADP2389/ADP2390, using short, wide traces, or connect the exposed SW pad to a large copper plane of the switching node for high current flow to reduce thermal resistance.
- Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To reduce noise pickup further, place an analog ground plane on either side of the FB trace and ensure that the trace is as short as possible to reduce the parasitic capacitance pickup.

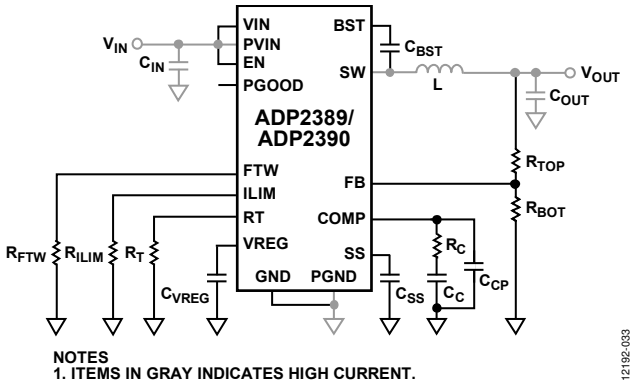

Figure 33. High Current Path in the PCB Circuit

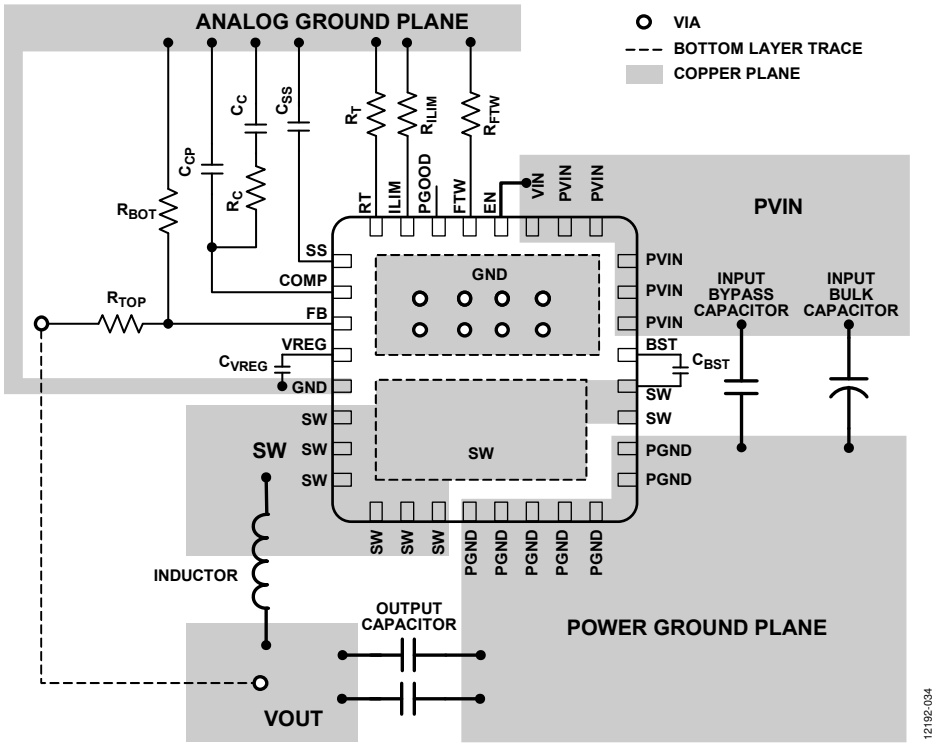

Figure 34. Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

Figure 35 through Figure 37 show some typical application circuits of the ADP2389/ADP2390 for user information.

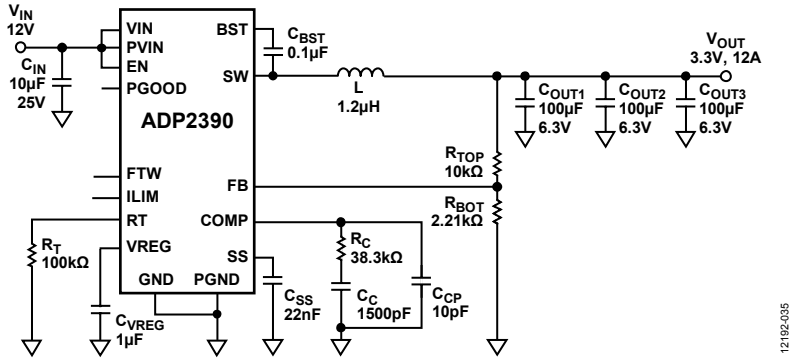

Figure 35. V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 12 A, f_{SW} = 600 kHz with PFM Mode

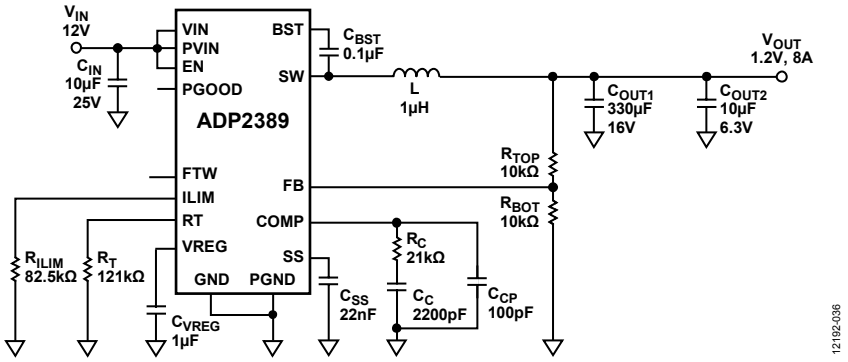

Figure 36. V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 8 A, f_{SW} = 500 kHz with Programmable Current Limit

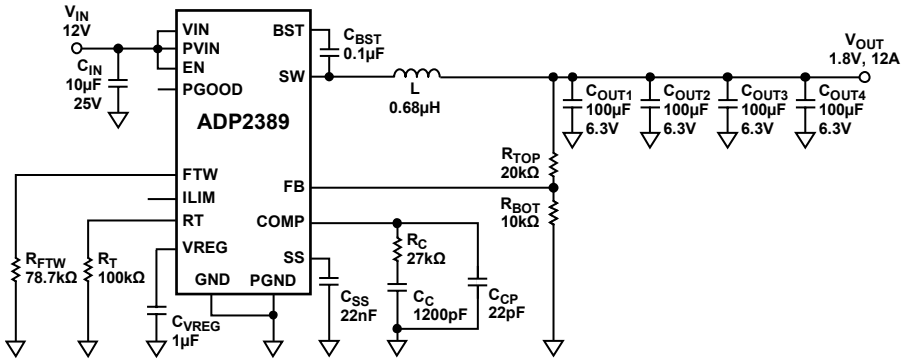

Figure 37. V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 12 A, f_{SW} = 600 kHz with Fast Transient

OUTLINE DIMENSIONS

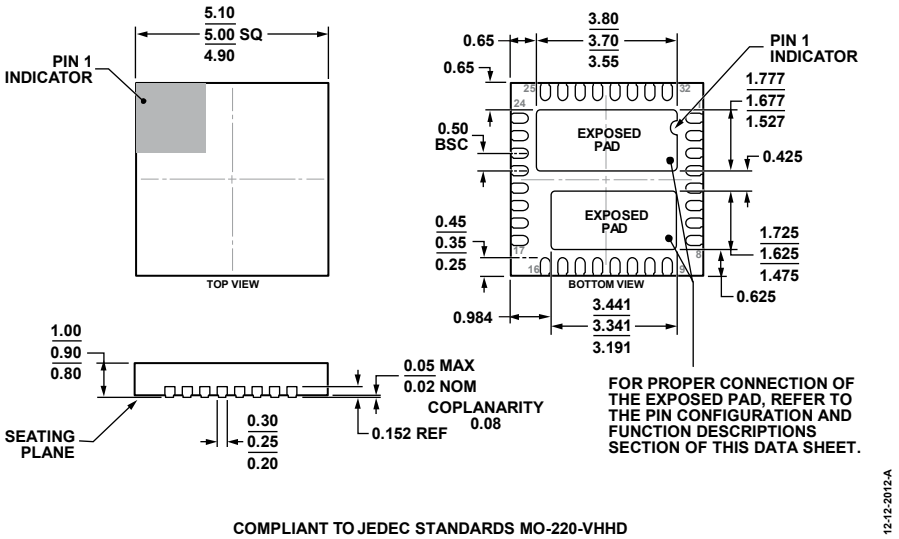

Figure 38. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-19)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage	Package Description	Package Option
ADP2389ACPZ-R7	−40°C to +125°C	Adjustable	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-19
ADP2390ACPZ-R7	−40°C to +125°C	Adjustable	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-19
ADP2389-EVALZ			Evaluation Board	
ADP2390-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.