



High-Speed, Low Power CMOS 10-Bit Bus Switches

QS3L384

2

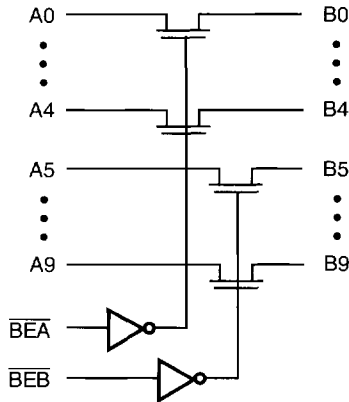
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Direct bus connection when switches on
- Zero propagation delay
- Ultra low power with 0.2 μA typical I_{cc}
- Two enables control five bits each
- Zero ground bounce
- Available in 24-pin DIP, SOIC (SO), QSOP and HQSOP

DESCRIPTION

The QS3L384 provides a set of ten high-speed CMOS TTL-compatible bus switches. The low ON resistance of the QS3L384 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The Bus Enable (\overline{BE}) signals turn the switches on. Two bus enable signals are provided, one for each of the upper and lower five bits of the two 10-bit buses.

FUNCTIONAL BLOCK DIAGRAM

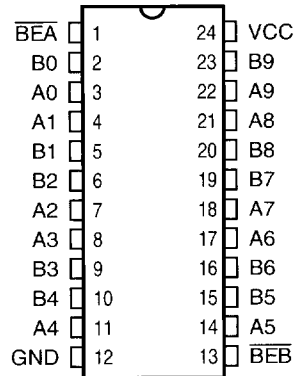


PIN DESCRIPTION

Name	I/O	Function
A9-A0	I/O	Bus A
B9-B0	I/O	Bus B
\overline{BEA} , \overline{BEB}	1	Bus Switch Enable

**PIN CONFIGURATION
(All Pins Top View)**

PDIP, SOIC (SO), QSOP, HQSOP



FUNCTION TABLE

\overline{BEA}	\overline{BEB}	B4-B0	B9-B5	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A4-A0	Hi-Z	Connect
H	L	Hi-Z	A9-A5	Connect
L	L	A4-A0	A9-A5	Connect

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	-0.5V to +7.0V
DC Switch Voltage V_s	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{IN} = 0V$, $V_{OUT} = 0V$

Pins	SOIC		QSOP		PDIP		HQSO		Unit
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Control Pins	3	4	3	4	4	5	6	7	pF
QuickSwitch Channels	7	8	7	8	8	9	10	11	pF

Note: Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$ Military: $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

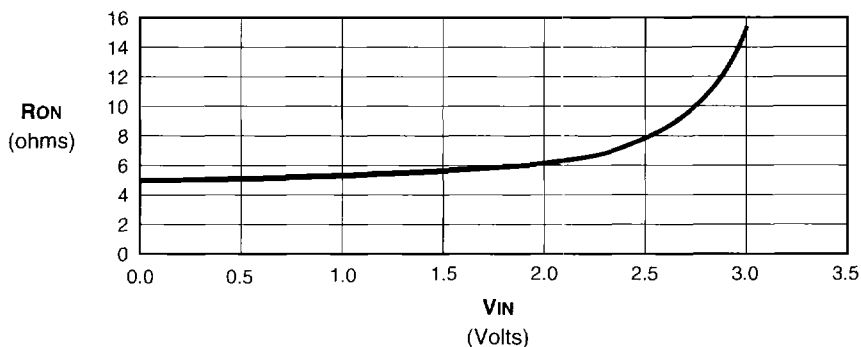
Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit	
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V	
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V	
$ I_{IN} $	Input Leakage Current ⁽²⁾	$0 \leq V_{IN} \leq V_{CC}$	—	—	1	μA	
$ I_{OZ} $	Off-State Current (Hi-Z)	$0 \leq A, B \leq V_{CC}$	—	.001	1	μA	
I_{OS}	Short Circuit Current ⁽³⁾	$A(B) = 0\text{V}$, $B(A) = V_{CC}$	—	300	—	mA	
R_{ON}	Switch ON Resistance ^(4,5)	$V_{CC} = \text{Min.}$, $V_{IN} = 0.0\text{V}$ $I_{ON} = 30\text{ mA}$	Com.	—	5	7	Ω
			Mil.	—	10	12	
R_{ON}	Switch ON Resistance ^(4,5)	$V_{CC} = \text{Min.}$, $V_{IN} = 2.4\text{V}$ $I_{ON} = 15\text{ mA}$	Com.	—	10	15	Ω
			Mil.	—	15	20	

2

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
2. During input/output leakage, testing all pins are at a HIGH or LOW state, and the \overline{BE} control is HIGH.
3. Not more than one output should be used to test this high power condition and the duration is ≤ 1 second.
4. Measured by voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A,B) pins.
5. Max. value R_{ON} guaranteed but not tested.

Typical ON Resistance vs V_{IN} at 4.75 Vcc



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ	Max	Unit
I _{CCQ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0	0.2	3.0	μA
ΔI _{CC}	Power Supply Current per Input HIGH ⁽²⁾	V _{CC} = Max., V _{IN} = 3.4V, f = 0 per Control Input	—	2.5	mA
Q _{CCD}	Dynamic Power Supply Current per MHz ⁽³⁾	V _{CC} = Max., A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	—	0.25	mA/MHz

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
- Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to I_{CC}.
- This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% Military: T_A = -55°C to 125°C, V_{CC} = 5.0V ± 10%
 C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description ⁽¹⁾		QS3L384			Unit
			Min	Typ	Max	
t _{PLH}	Data Propagation Delay ^(2,4)	COM	—	—	0.25 ⁽³⁾	ns
t _{PHL}	Ai to Bi, Bi to Ai	MIL	—	—	0.75 ⁽³⁾	
t _{PZL}	Switch Turn-on Delay ⁽¹⁾	COM	1.5	—	6.5	ns
t _{PZH}	\overline{BEA} , \overline{BEB} to Ai, Bi	MIL	1.5	—	7.5	
t _{PLZ}	Switch Turn-off Delay ^(1,2)	COM	1.5	—	5.5	ns
t _{PHZ}	BEA, BEB to Ai, Bi	MIL	1.5	—	6.5	
Q _{CI}	Charge Injection ⁽⁵⁾	COM	—	1.5	—	pC
		MIL	—	1.5	—	

Notes:

- See Test Circuit and Waveforms. Minimums guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The time constant for the switch alone is of the order of 0.25 ns for 50 pF.
- The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at I = 0.0V.
- Characterized parameter but not production tested.