SLG59M1746C

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm² WLCSP Load Switch with Controlled Inrush Current

General Description

The SLG59M1746C is a high-performance 1 A capable, single-channel load switch designed for high-side power control applications up to 1 A. This feature-rich nFET load switch has been optimized for all small form-factor, single-cell Li-ion applications including smartphone, fitness bands, and watches.

Operating from 2.7 V to 3.6 V supplies, the SLG59M1746C's RDS_{ON} is 17.6 mΩ and exhibits an input voltage range that extends from 0.25 V to 1.5 V. The SLG59M1746C's novel nFET architecture achieves very low supply current operation, controlled V_{IN} inrush current profile, and world-class V_{IN} range to rival the performance of many general-purpose nFET and pFET load switches on the market.

Using Renesas's proprietary MOSFET IP, the SLG59M1746C achieves a stable RDS_{ON} as a function of both the supply and input voltages. Fully specified over the -40 °C to 85 °C temperature range, this advanced nFET load switch is available in 6-lead WLCSP measuring 0.71 mm x 1.16 mm x 0.5 mm with 0.35 mm pitch. The SLG59M1746C consumes less than 1 µA after start up. There are no protection features such as over temperature or over current shutdown, etc.

Features

- High-performance nFET Design:
  - Low Typical RDS_{ON}: 17.6 mΩ
- Steady-state Operating Current: 1 A
- Small Inrush Current
- Very Low Supply current after startup: < 1µA
- Operating V_{DD} Range: 2.7 V ≤ V_{DD} ≤ 3.6 V
- Operating V_{IN} Range: 0.25 V ≤ V_{IN} ≤ 1.5 V
- Fast V_{OUT} Discharge
- ON/OFF Control: Active HIGH
- Operating Temperature: -40 °C to 85 °C
- Pb-Free / Halogen-Free / RoHS compliant WLCSP
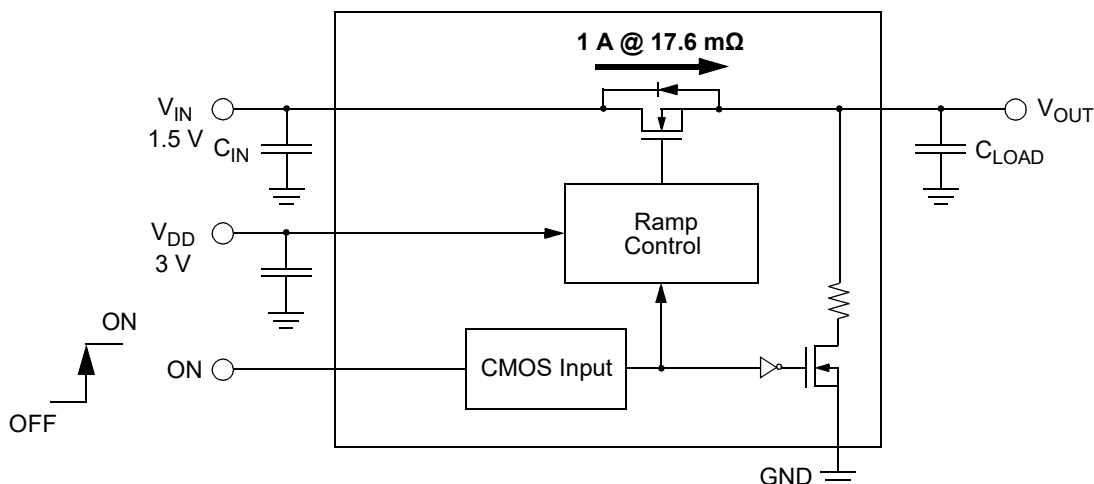 - 6 lead 0.71 mm x 1.16 mm, 0.35 mm pitch

Pin Configuration
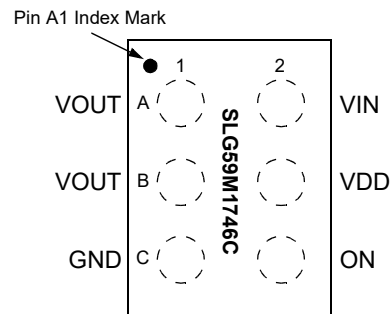
6L WLCSP
(Laser Marking View)

Applications

- Smartphones
- Fitness Bands
- Watches
- Tablet PCs

Block Diagram

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP Load Switch with Controlled Inrush Current

Pin Description

Pin #	Pin Name	Type	Pin Description
B2	VDD	Power	VDD supplies the power for the operation of the load switch and the internal control circuitry. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor.
A2	VIN	MOSFET	Drain terminal connection of the n-channel MOSFET. Connect a 1 µF (or larger) low-ESR capacitor from this pin to ground.
A1, B1	VOUT	MOSFET	Source terminal connections of the n-channel MOSFET. Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C$_{LOAD}$ range.
C2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1746C's state machine. ON is an asserted HIGH, level-sensitive CMOS input with ON_V$_{IL}$ < 0.3 V and ON_V$_{IH}$ > 0.85 V. As the ON pin input circuit has an internal 8 MΩ pull-down, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
C1	GND	VOUT	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1746C	WLCSP 6L	Industrial, -40 °C to 85 °C
SLG59M1746CTR	WLCSP 6L (Tape and Reel)	Industrial, -40 °C to 85 °C

SLG59M1746C

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V$_{DD}$ to GND	Power Supply Voltage to GND		-0.3	--	5	V
V$_{IN}$ to GND	Load Switch Input Voltage to GND		-0.3	--	5	V
V$_{OUT}$ to GND	Load Switch Output Voltage to GND		-0.3	--	5	V
ON to GND	ON Pin Voltage to GND		-0.3	--	5	V
T$_S$	Storage Temperature		-65	--	150	°C
T$_J$	Junction Temperature		-40	--	150	°C
ESD$_{HBM}$	ESD Protection	Human Body Model	3000	--	--	V
ESD$_{CDM}$	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level			1		
θ$_{JA}$	Package Thermal Resistance, Junction-to-Ambient	0.71 x 1.16 mm 6L WLCSP; Determined using 0.25 in^2, 1 oz .copper pads under each VIN and VOUT terminal and FR4 pcb material.	--	88	--	°C/W
T$_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET IDS$_{PK}$	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

2.7 V ≤ V$_{DD}$ ≤ 3.6 V; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; T$_A$ = -40 °C to 85 °C, unless otherwise noted. Typical values are at T$_A$ = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V$_{DD}$	Power Supply Voltage		2.7	--	3.6	V
V$_{IN}$	Load Switch Input Voltage		0.25	--	1.5	V
I$_{DD\_Q1}$	V$_{DD}$ Quiescent Supply Current during startup	V$_{DD}$ = 2.7 V; ON = V$_{DD}$; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.4	20.9	µA
		V$_{DD}$ = 2.7 V; ON = 1.8 V; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.4	20.9	µA
		V$_{DD}$ = 3.0 V; ON = V$_{DD}$; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.4	20.9	µA
		V$_{DD}$ = 3.0 V; ON = 1.8 V; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.4	20.9	µA
		V$_{DD}$ = 3.3 V; ON = V$_{DD}$; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.5	20.9	µA
		V$_{DD}$ = 3.3 V; ON = 1.8 V; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.6	20.9	µA
		V$_{DD}$ = 3.6 V; ON = V$_{DD}$; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.7	21.5	µA
		V$_{DD}$ = 3.6 V; ON = 1.8 V; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; No Load	--	15.8	21.5	µA
I$_{DD\_Q2}$	V$_{DD}$ Quiescent Supply Current after startup / Power FET fully turned on	2.7 V ≤ V$_{DD}$ ≤ 3.6 V; ON = V$_{DD}$ after startup; No Load	--	--	0.5	µA

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Load Switch with Controlled Inrush Current

Electrical Characteristics (continued)

2.7 V ≤ V$_{DD}$ ≤ 3.6 V; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; T$_A$ = -40 °C to 85 °C, unless otherwise noted. Typical values are at T$_A$ = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I$_{SHDN}$	OFF Mode Supply Current	2.7 V ≤ V$_{DD}$ ≤ 3.6 V; ON = LOW; No Load	--	--	0.33	µA
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	1	A
IDS$_{INRUSH}$	MOSFET Drain to Source Inrush Current	Inrush current during startup with C$_{LOAD}$ up to 30 µF when zero load current	--	9	20	mA
RDS$_{ON}$	ON Resistance	T$_A$ = 25 °C; V$_{DD}$ = 3.0 V; V$_{IN}$ = 1.5 V; I$_{DS}$ = 0.1 A	--	17.6	22	mΩ
		T$_A$ = 85 °C; V$_{DD}$ = 3.0 V; V$_{IN}$ = 1.5 V; I$_{DS}$ = 0.1 A	--	22	25	mΩ
I$_{FET\_OFF}$	MOSFET OFF Leakage Current	2.7 V ≤ V$_{DD}$ ≤ 3.6 V; V$_{IN}$ = 1.5 V, V$_{OUT}$ = 0 V; ON = LOW	--	0.01	1	µA
T$_{ON\_Delay}$	ON Delay Time	50% ON to 10% V$_{OUT}$ ↑; V$_{DD}$ = 2.7 V; V$_{IN}$ = 1.5 V, R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	--	0.59	0.98	ms
		50% ON to 10% V$_{OUT}$ ↑; V$_{DD}$ = 3.6 V; V$_{IN}$ = 1.5 V, R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	--	0.58	0.98	ms
V$_{OUT(SR)}$	V$_{OUT}$ Slew Rate	10% V$_{OUT}$ to 90% V$_{OUT}$ ↑; V$_{DD}$ = 2.7 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	0.20	0.38	0.55	V/ms
		10% V$_{OUT}$ to 90% V$_{OUT}$ ↑; V$_{DD}$ = 3.6 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	0.20	0.38	0.55	V/ms
T$_{OFF\_Delay}$	OFF Delay Time	50% ON to V$_{OUT}$ Fall Start ↓; V$_{DD}$ = 2.7 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; no C$_{LOAD}$	--	3	4.5	µs
		50% ON to V$_{OUT}$ Fall Start ↓; V$_{DD}$ = 3.6 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; no C$_{LOAD}$	--	6.5	9	µs
C$_{LOAD}$	Output Load Capacitance	C$_{LOAD}$ connected from VOUT to GND	--	10	--	µF
R$_{DISCHRG}$	Output Discharge Resistance	2.7 V ≤ V$_{DD}$ ≤ 3.6 V; V$_{OUT}$ < 0.4 V	--	160	210	Ω
ON_V$_{IH}$	ON Pin Input High Voltage		0.85	--	V$_{DD}$	V
ON_V$_{IL}$	ON Pin Input Low Voltage		-0.3	0	0.3	V

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current
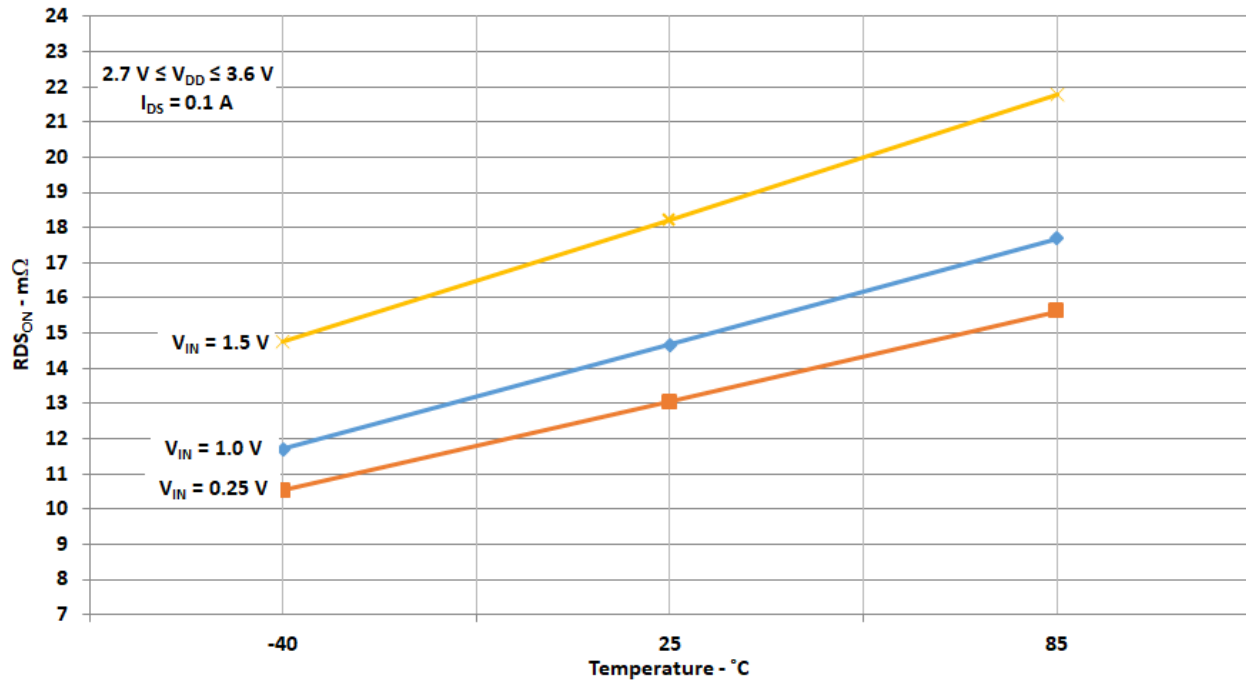
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement
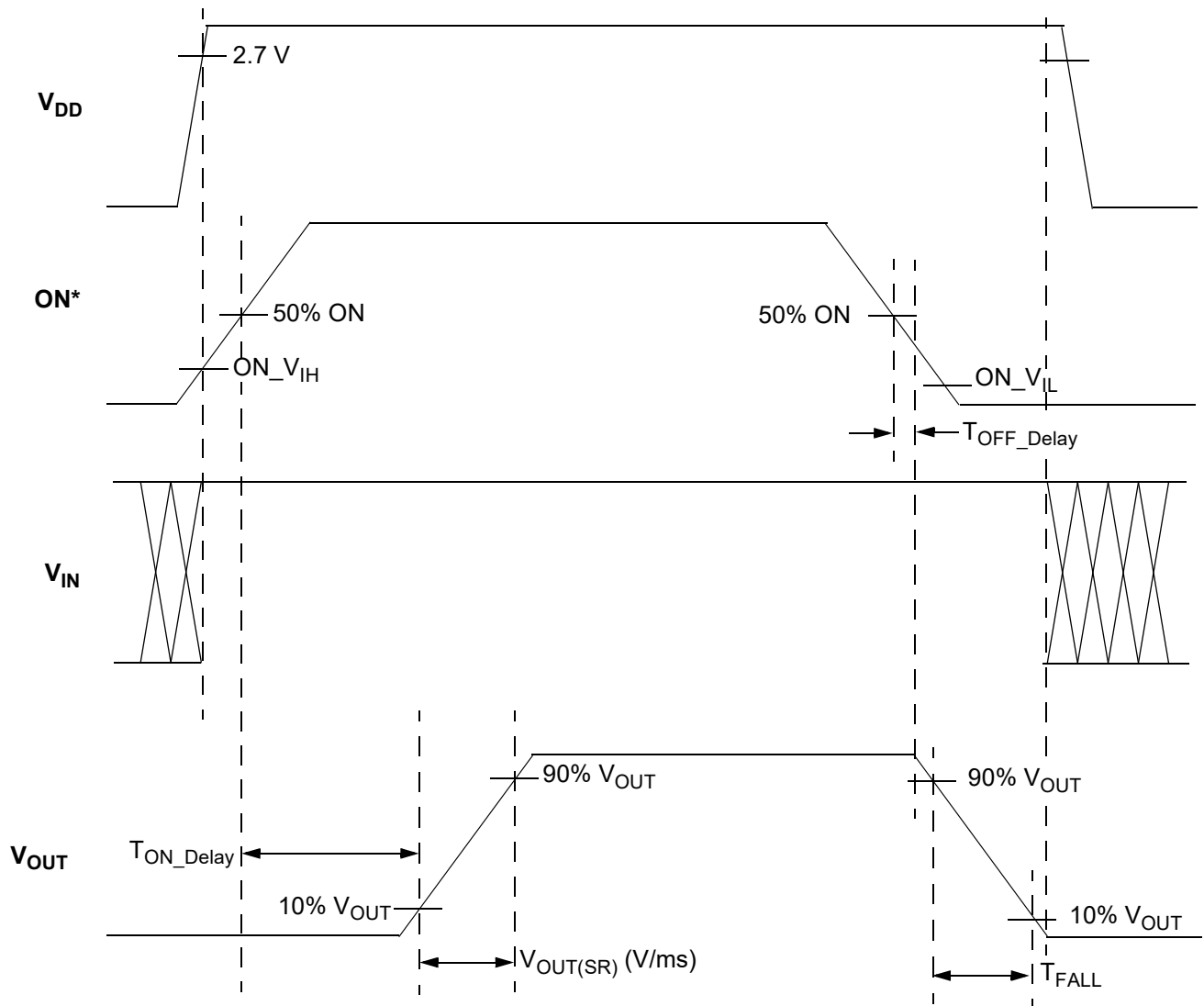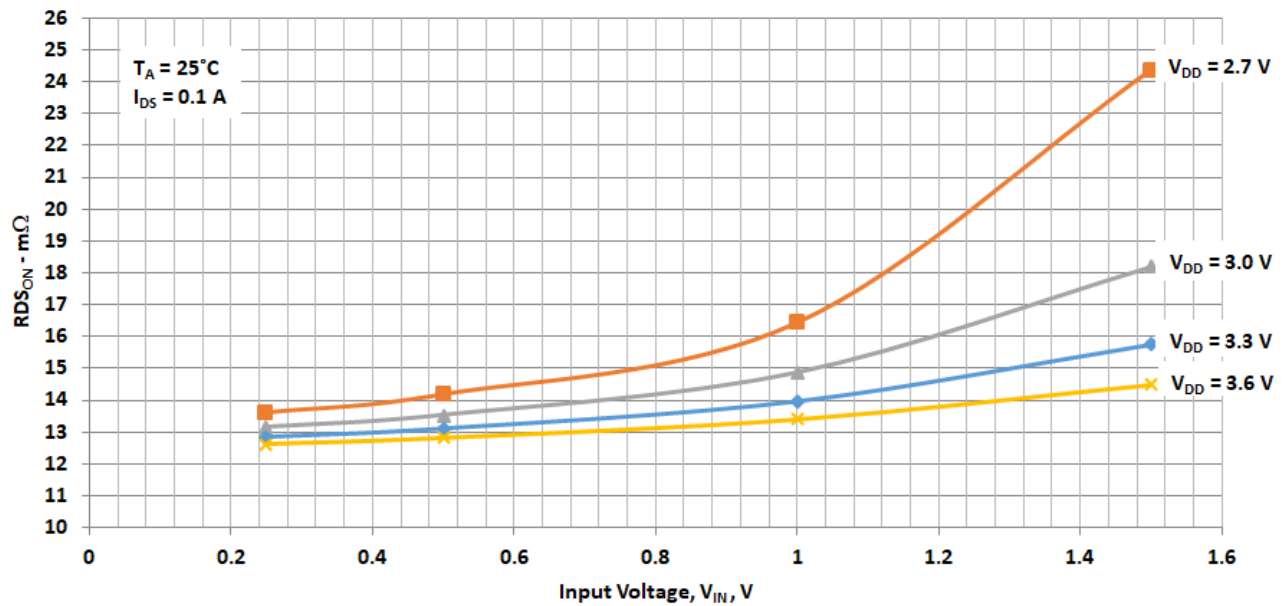

*Rise and Fall Times of the ON Signal are 100 ns

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Typical Performance Characteristics
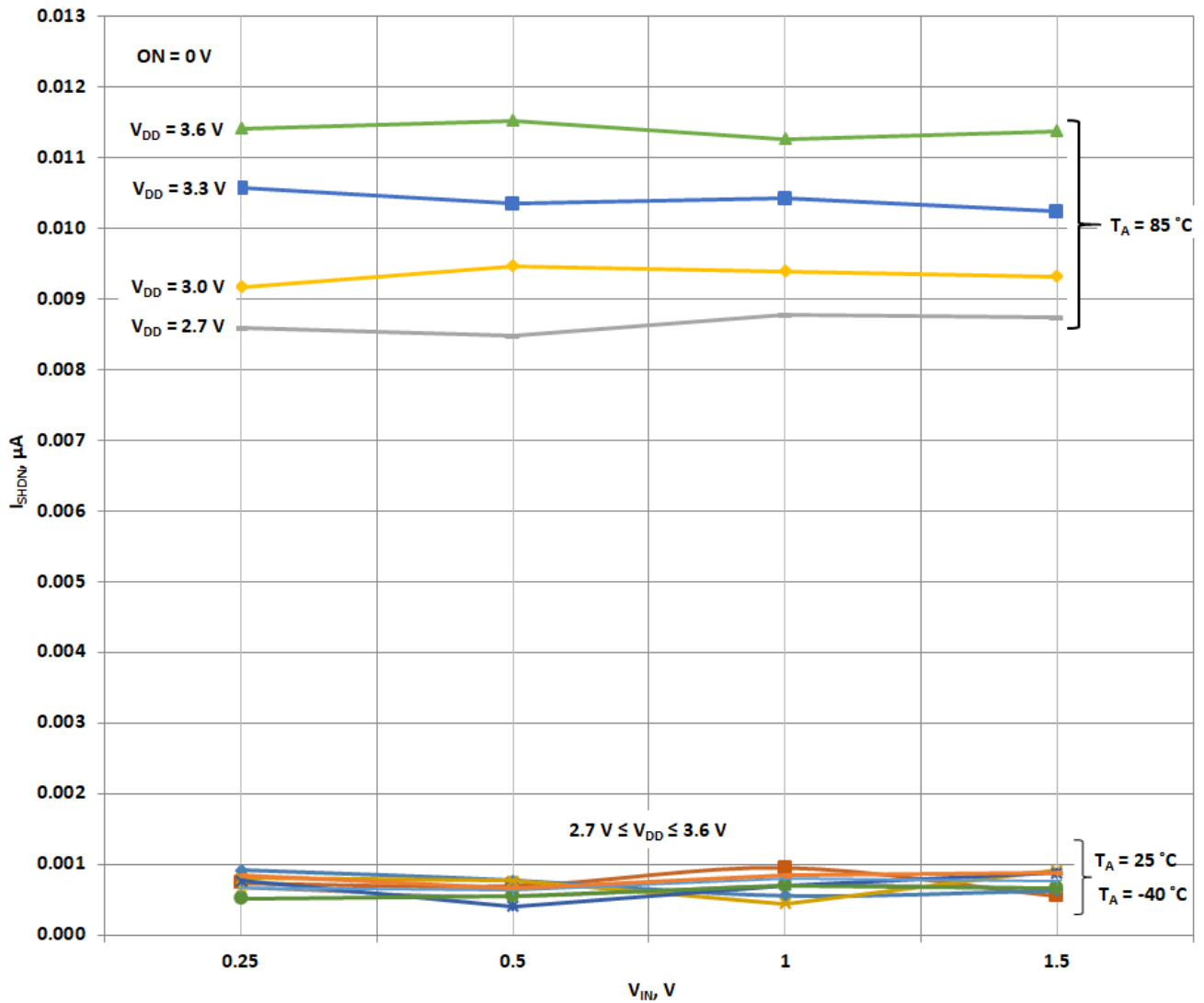
RDS$_{ON}$ vs. Temperature, V$_{IN}$, and V$_{DD}$

RDS$_{ON}$ vs. V$_{IN}$, and V$_{DD}$

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

I$_{SHDN}$ vs. V$_{IN}$, V$_{DD}$, and Temperature

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

I_{DD_Q2} when ON = 1.8 V vs. V_{IN}, V_{DD}, and Temperature
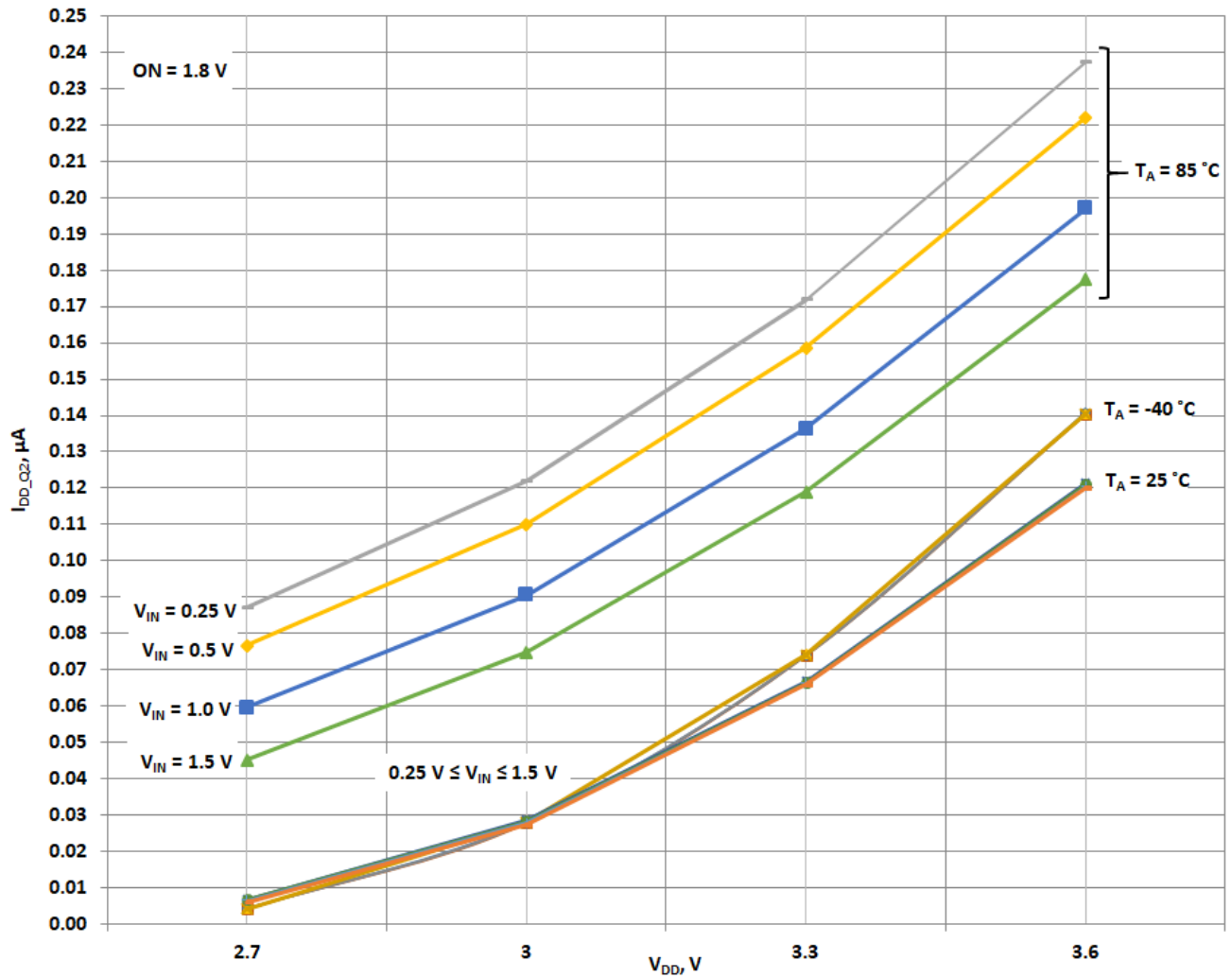
An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

I$_{DD\_Q2}$ when ON = V$_{DD}$ vs. V$_{IN}$, V$_{DD}$, and Temperature
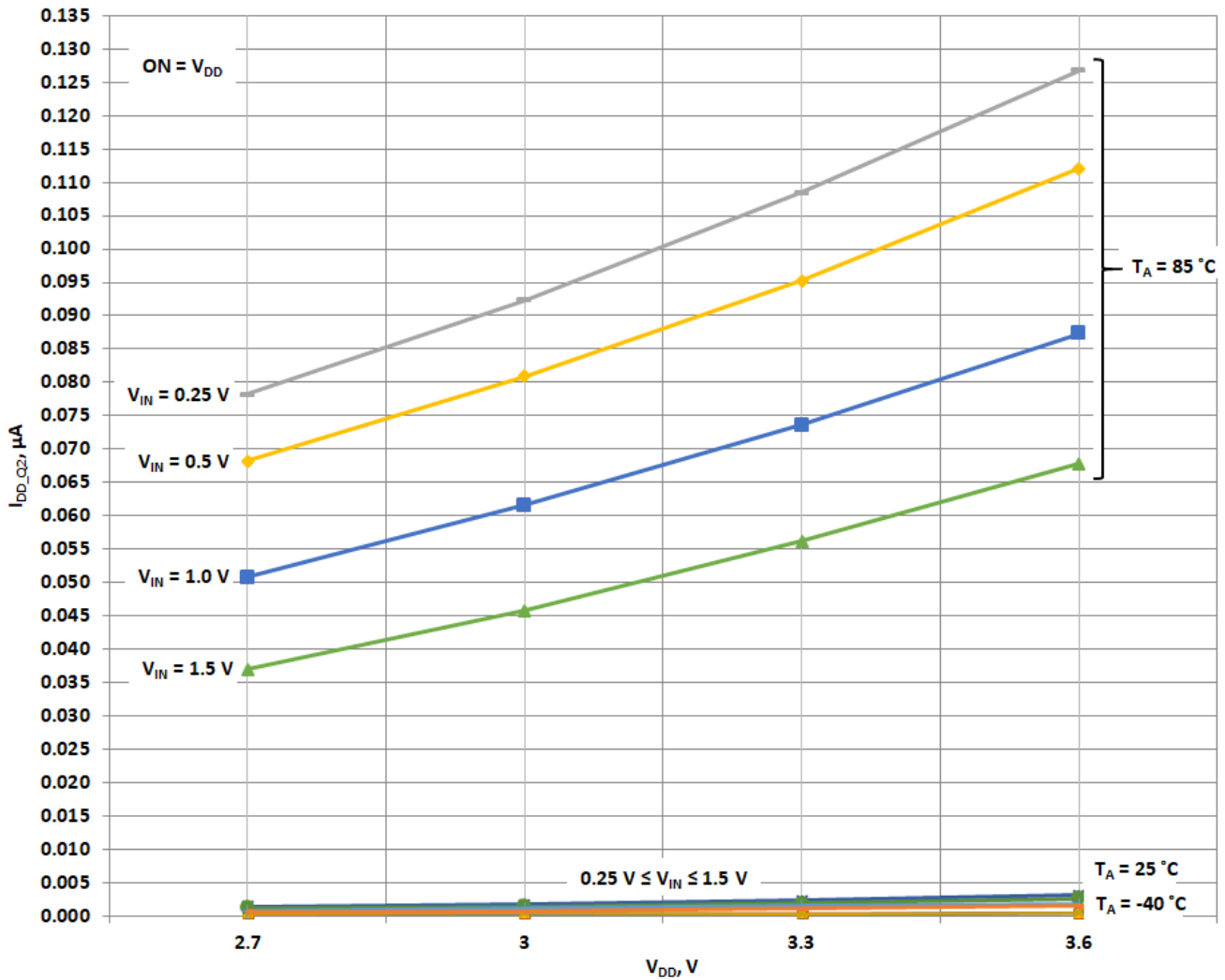
An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
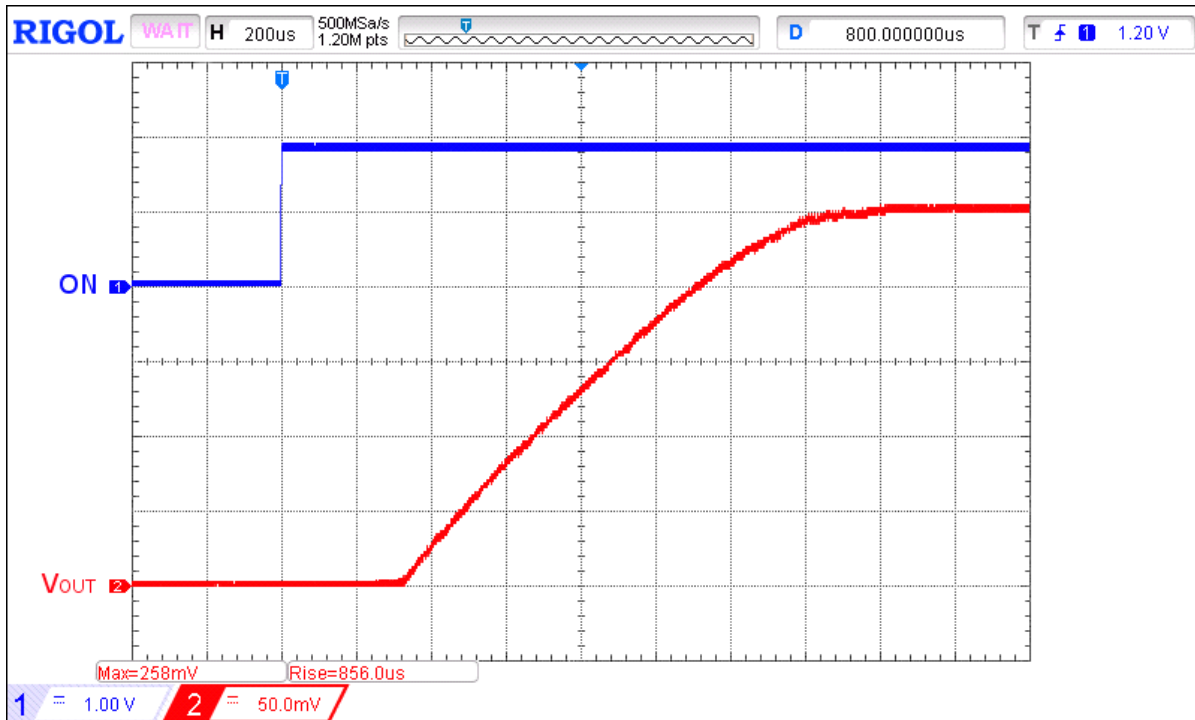Load Switch with Controlled Inrush Current

Typical Turn-on Waveforms
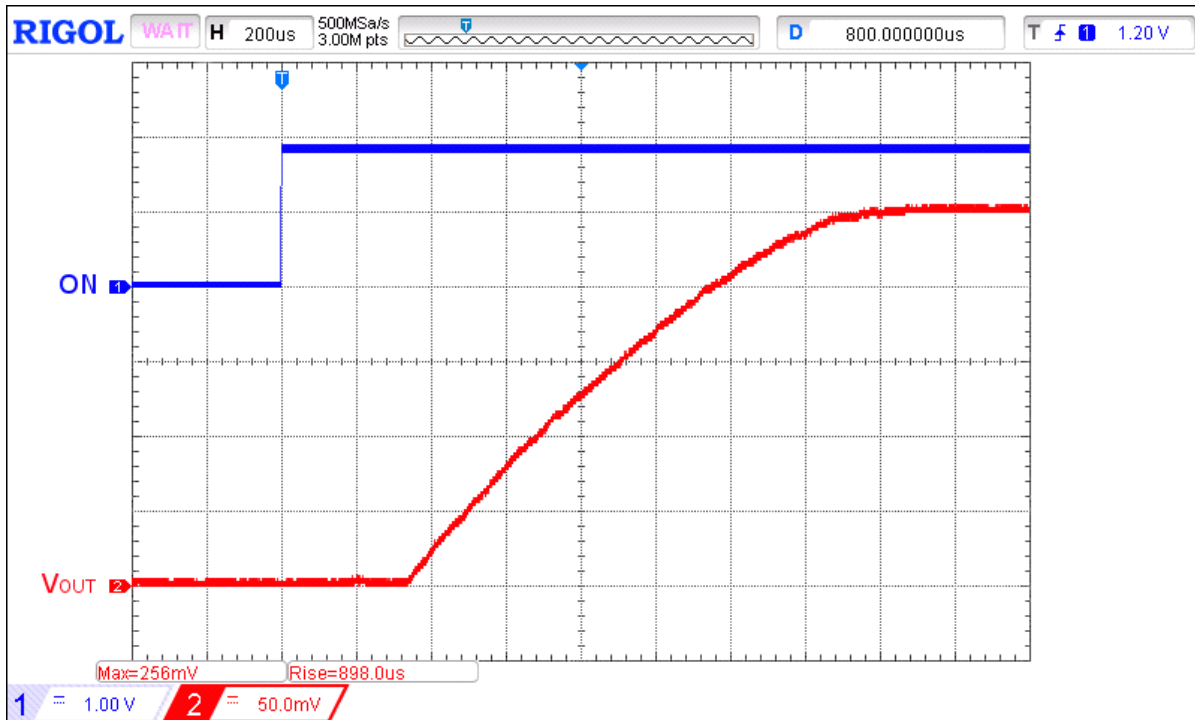
Figure 1. Typical Turn ON operation waveform for V_{DD} = 2.7 V, V_{IN} = 0.25 V, C_{LOAD} = 10 µF, R_{LOAD} = 1 kΩ
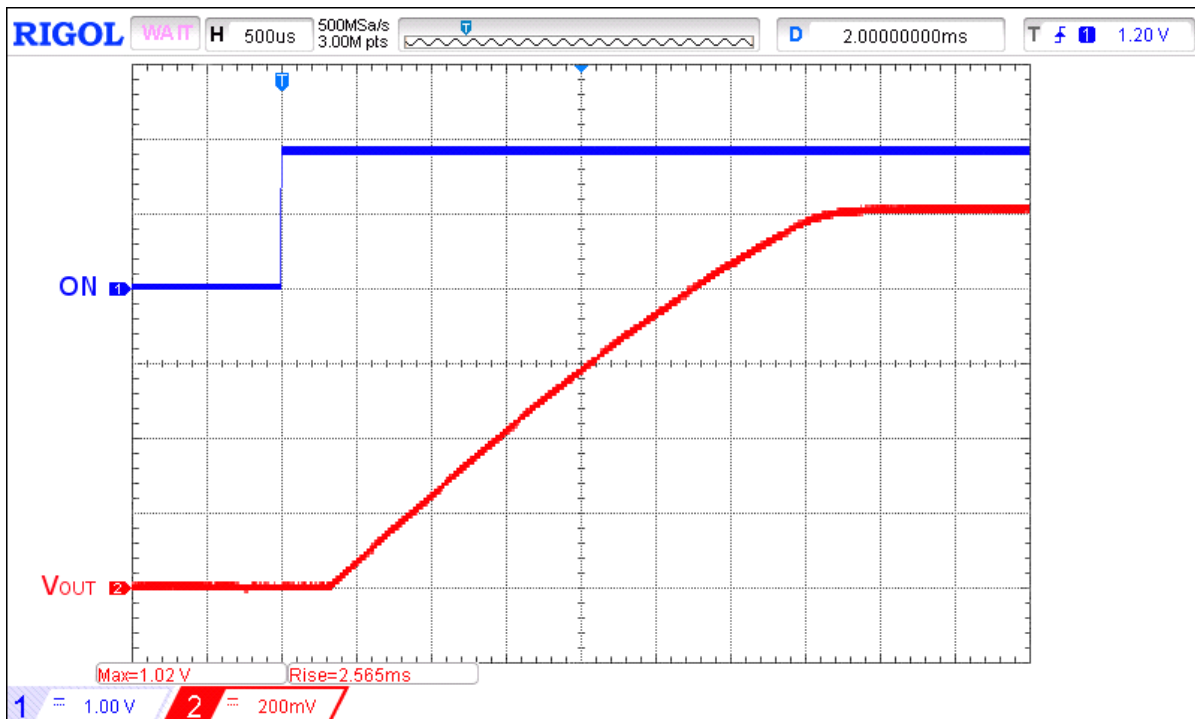
Figure 2. Typical Turn ON operation waveform for V_{DD} = 2.7 V, V_{IN} = 1 V, C_{LOAD} = 10 µF, R_{LOAD} = 1 kΩ

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current
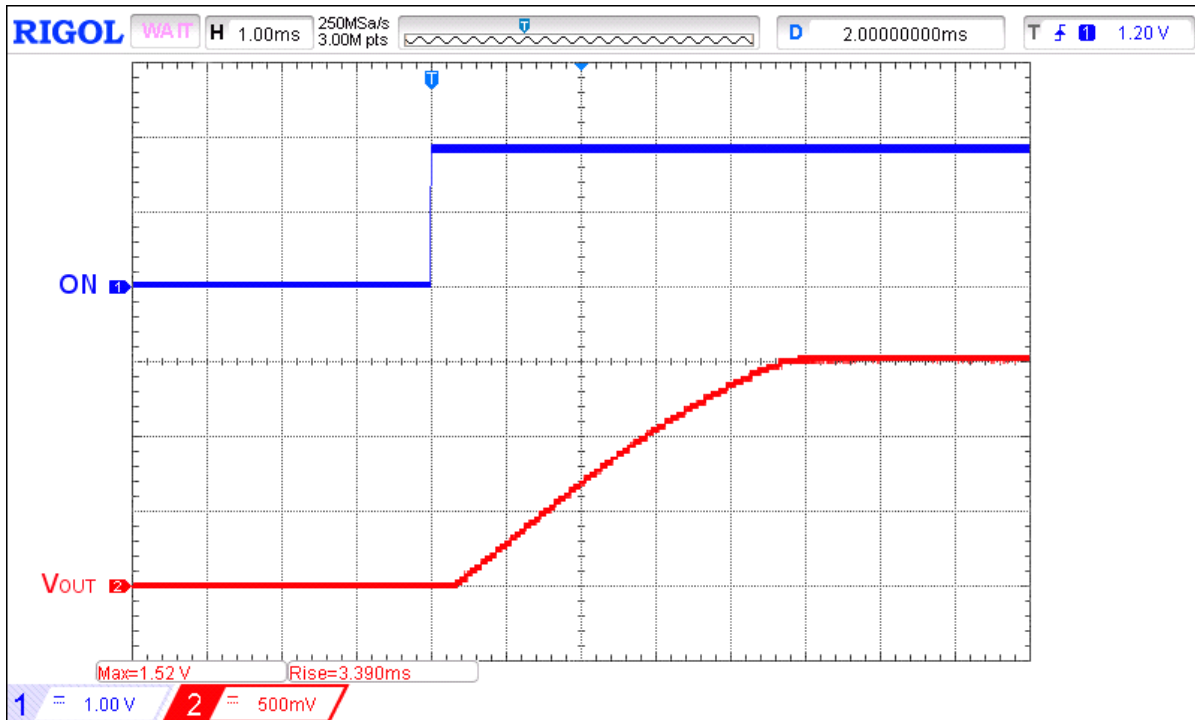
Figure 3. Typical Turn ON operation waveform for V_{DD} = 2.7 V, V_{IN} = 1.5 V, C_{LOAD} = 10 µF, R_{LOAD} = 1 kΩ
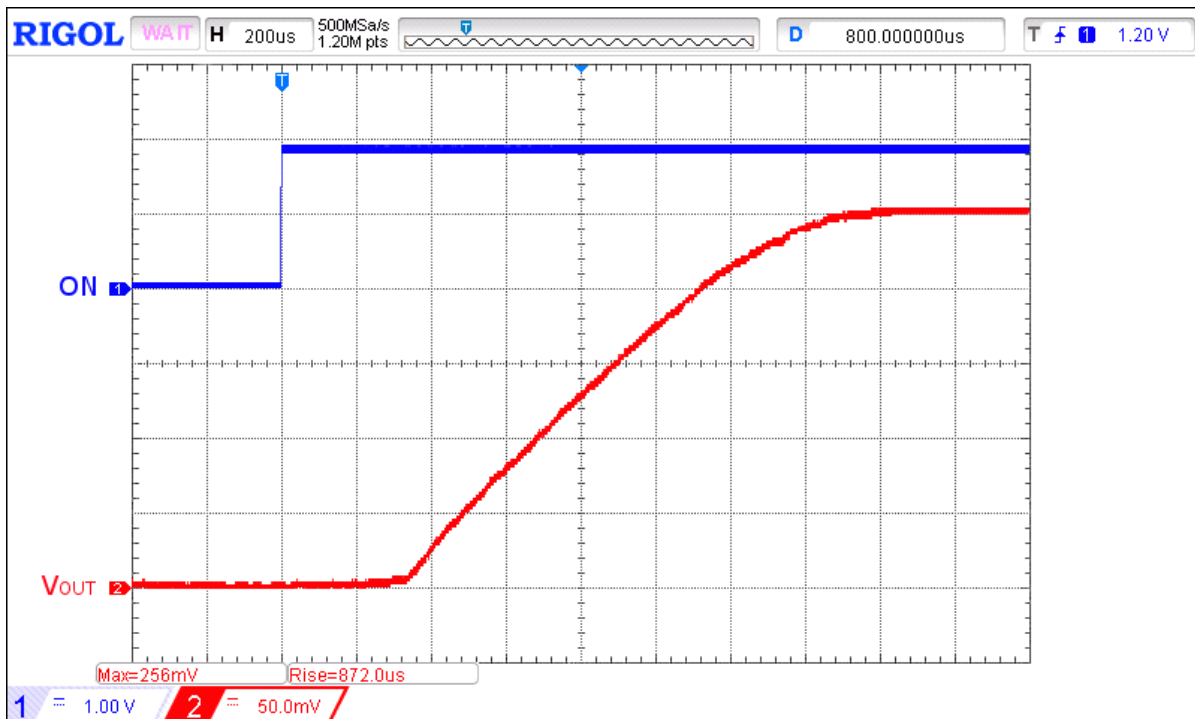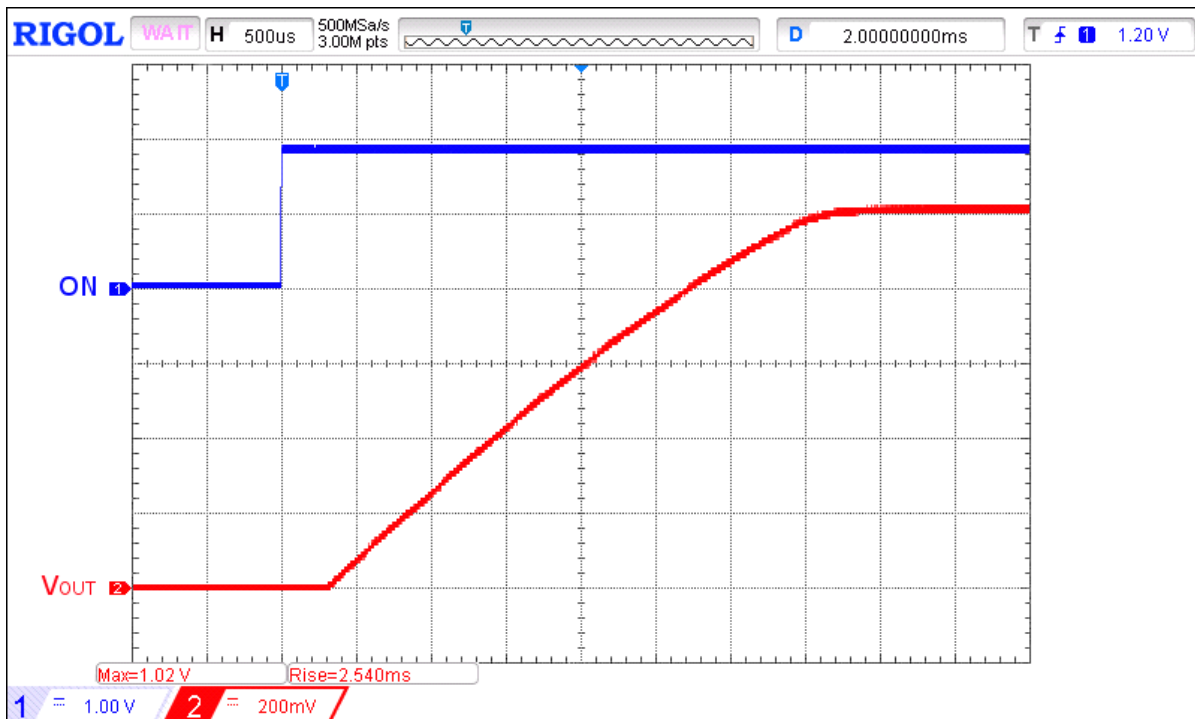

Figure 4. Typical Turn ON operation waveform for V_{DD} = 3 V, V_{IN} = 0.25 V, C_{LOAD} = 10 µF, R_{LOAD} = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
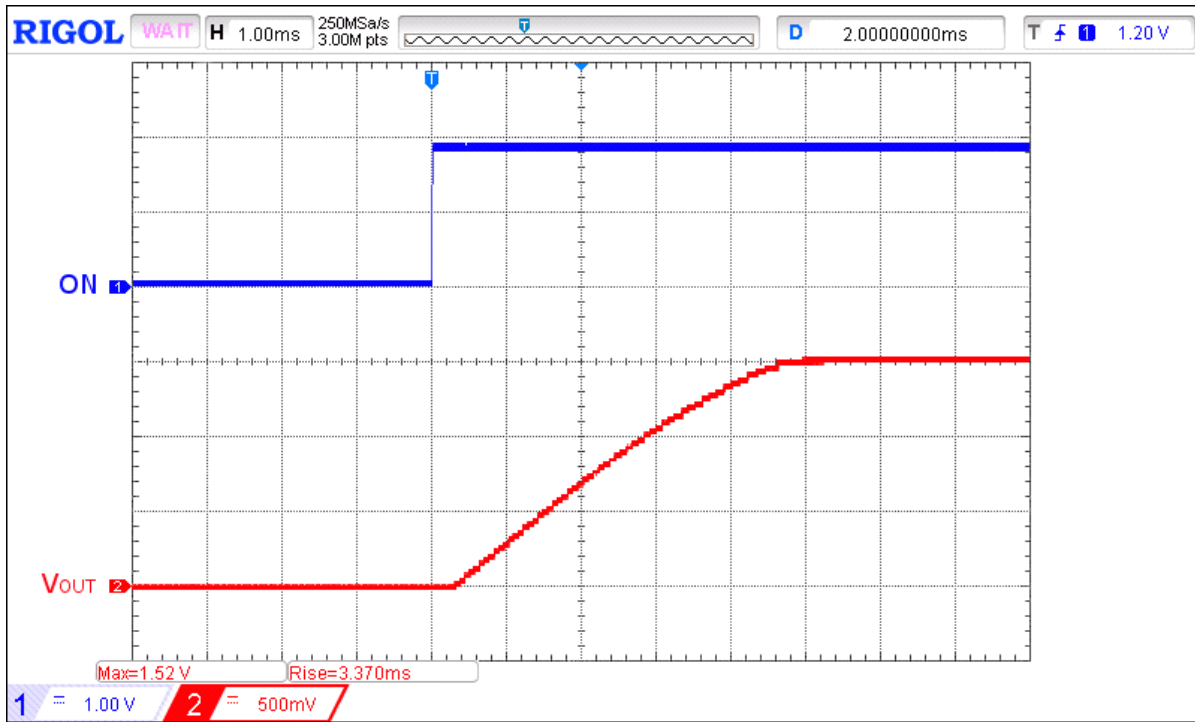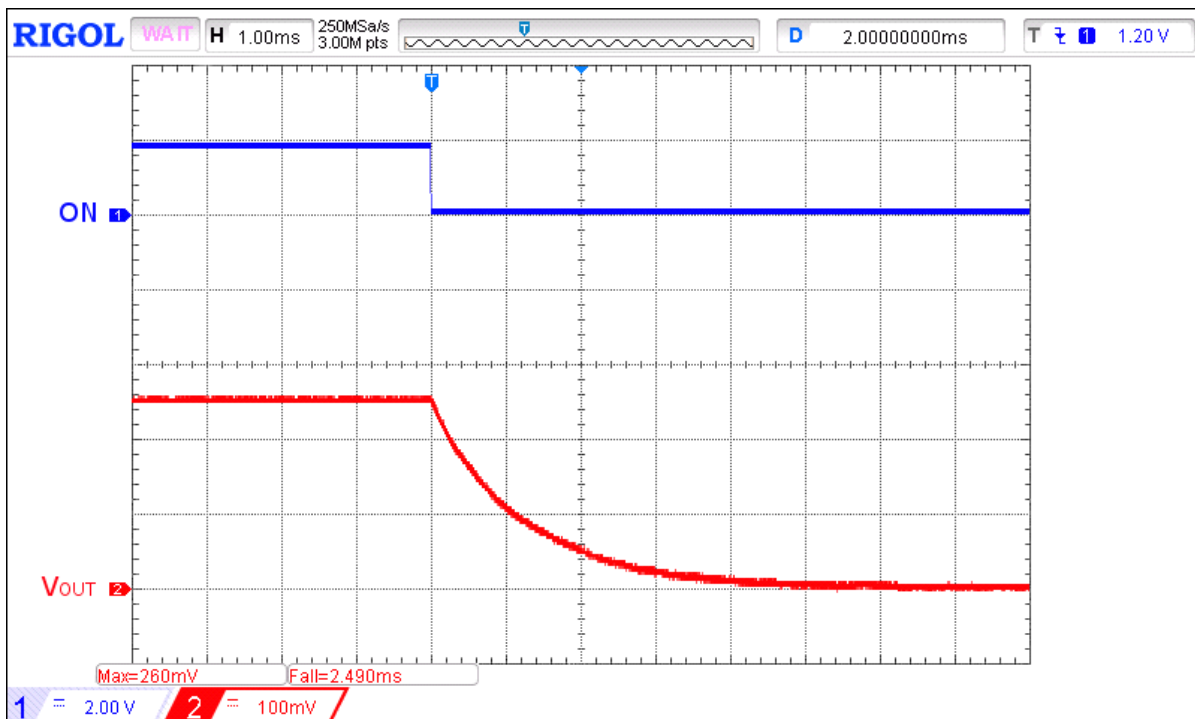Load Switch with Controlled Inrush Current
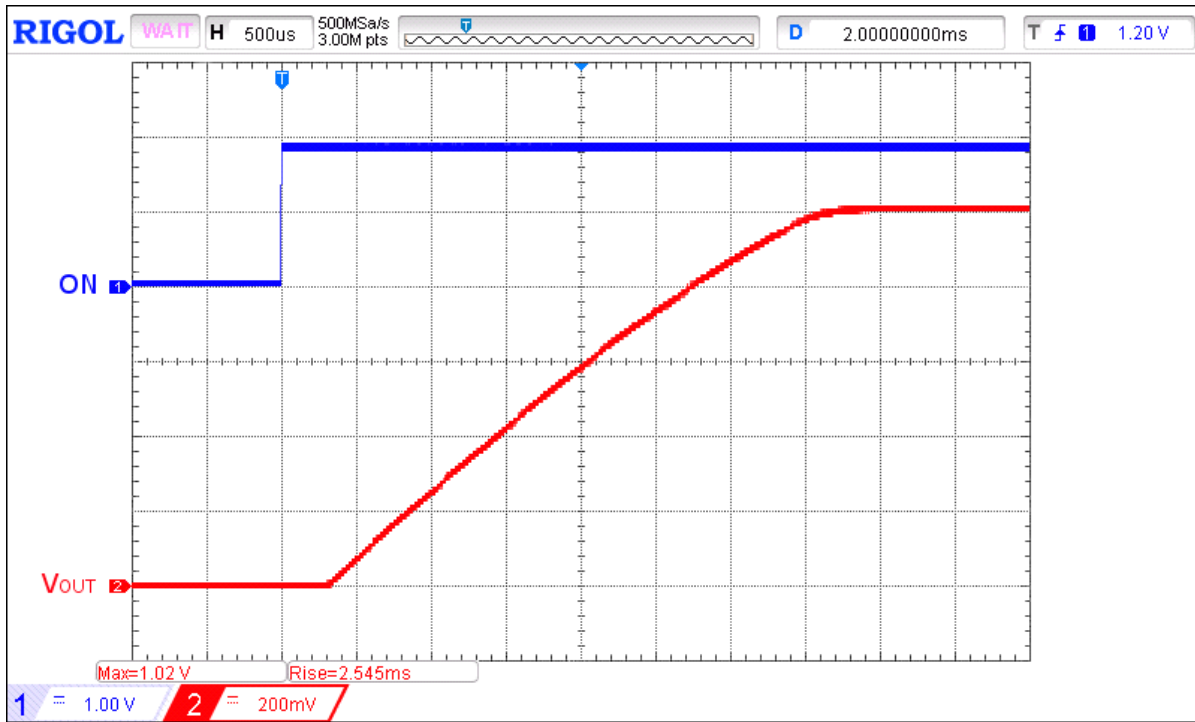
Figure 5. Typical Turn ON operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ
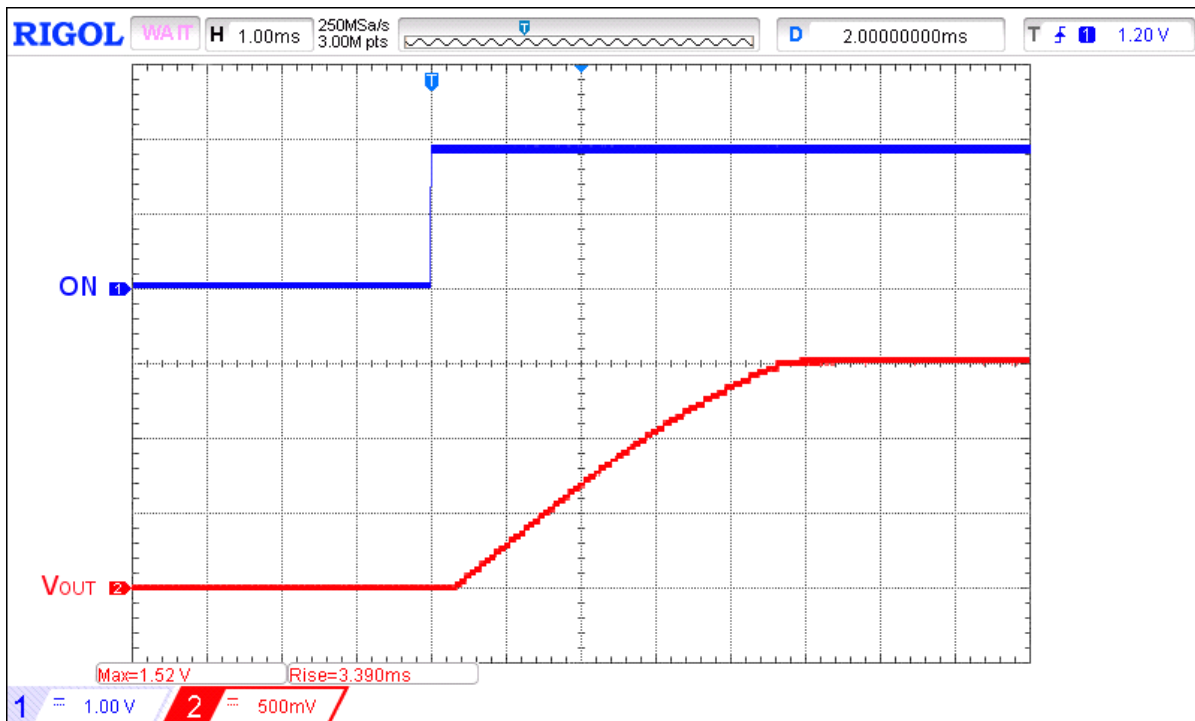
Figure 6. Typical Turn ON operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

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Figure 7. Typical Turn ON operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

Figure 8. Typical Turn ON operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

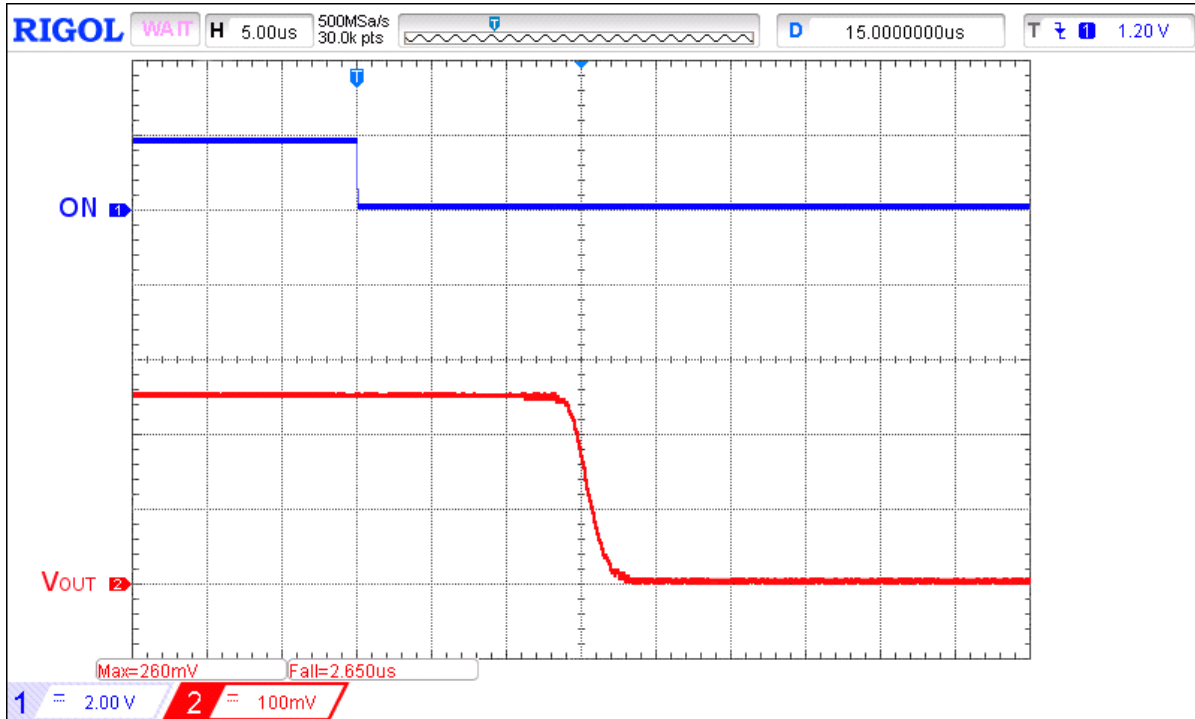**Figure 9. Typical Turn ON operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ**

Typical Turn-off Waveforms

Figure 10. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Figure 11. Typical Turn OFF operation waveform for V_{DD} = 2.7 V, V_{IN} = 0.25 V, no C_{LOAD}, R_{LOAD} = 1 kΩ
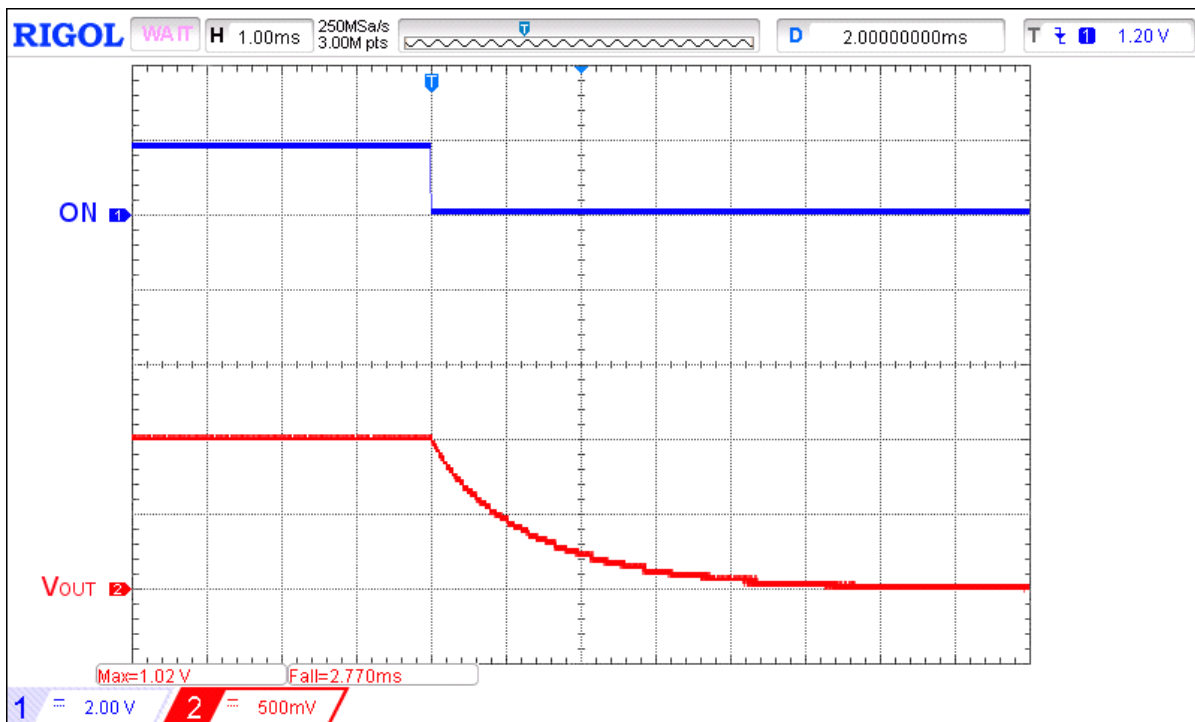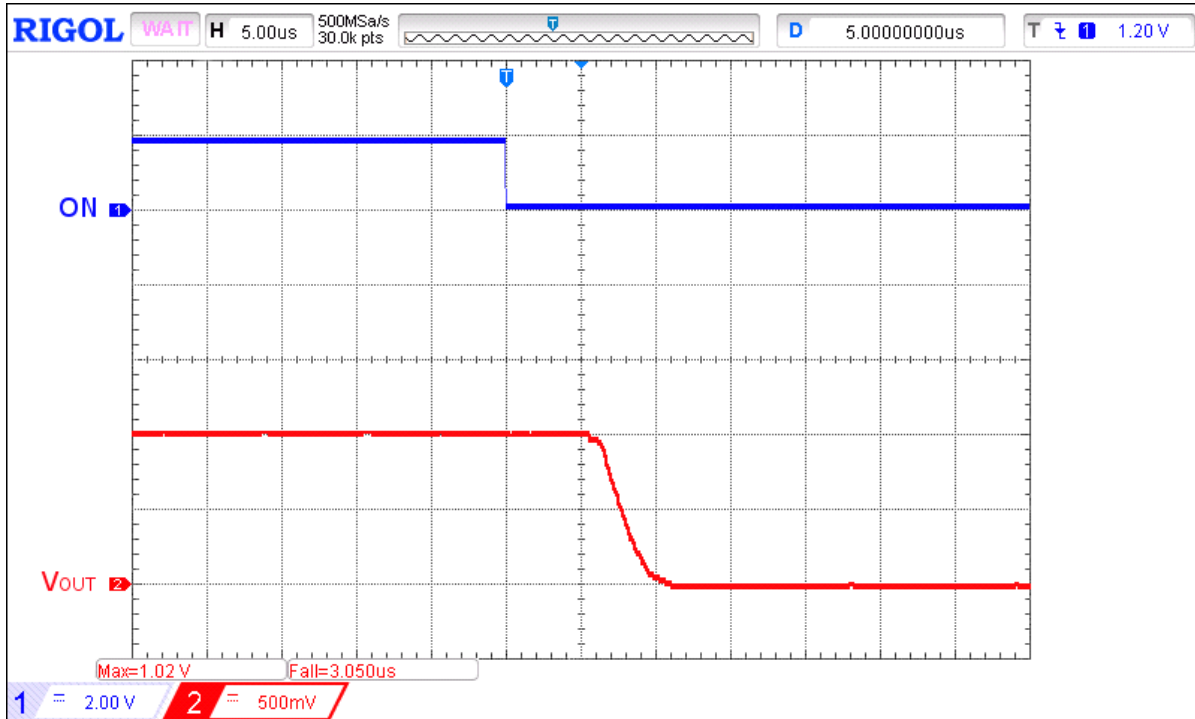

Figure 12. Typical Turn OFF operation waveform for V_{DD} = 2.7 V, V_{IN} = 1 V, C_{LOAD} = 10 µF, R_{LOAD} = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Figure 13. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
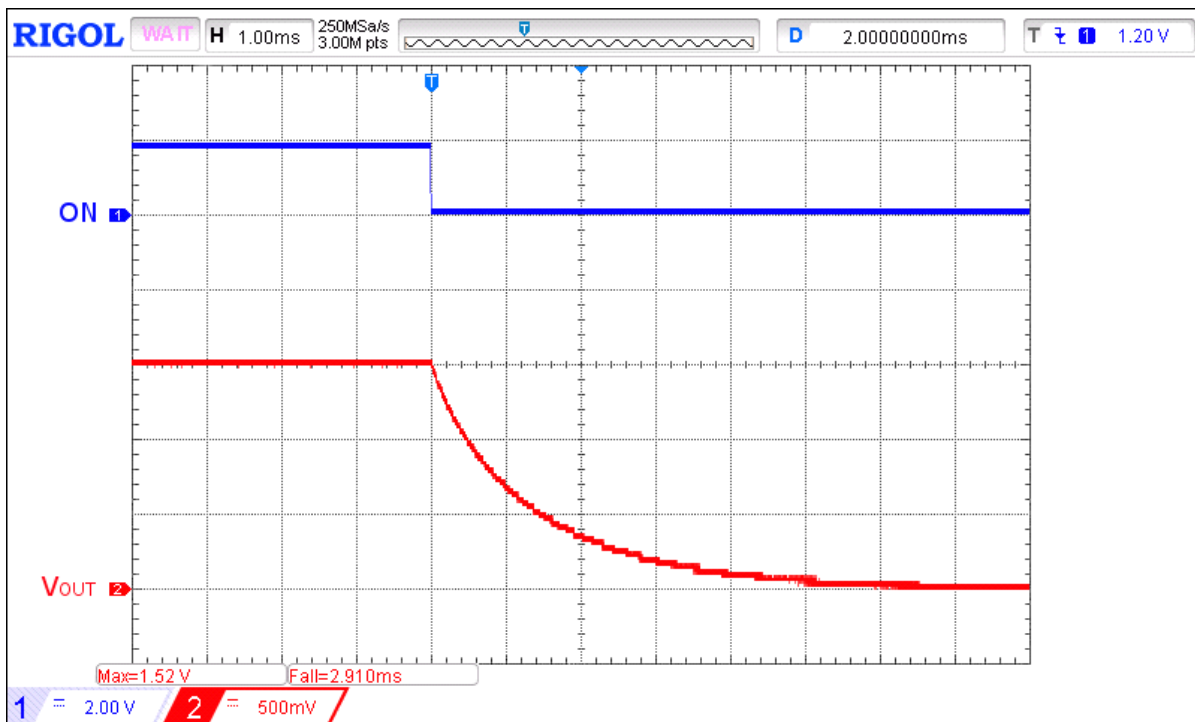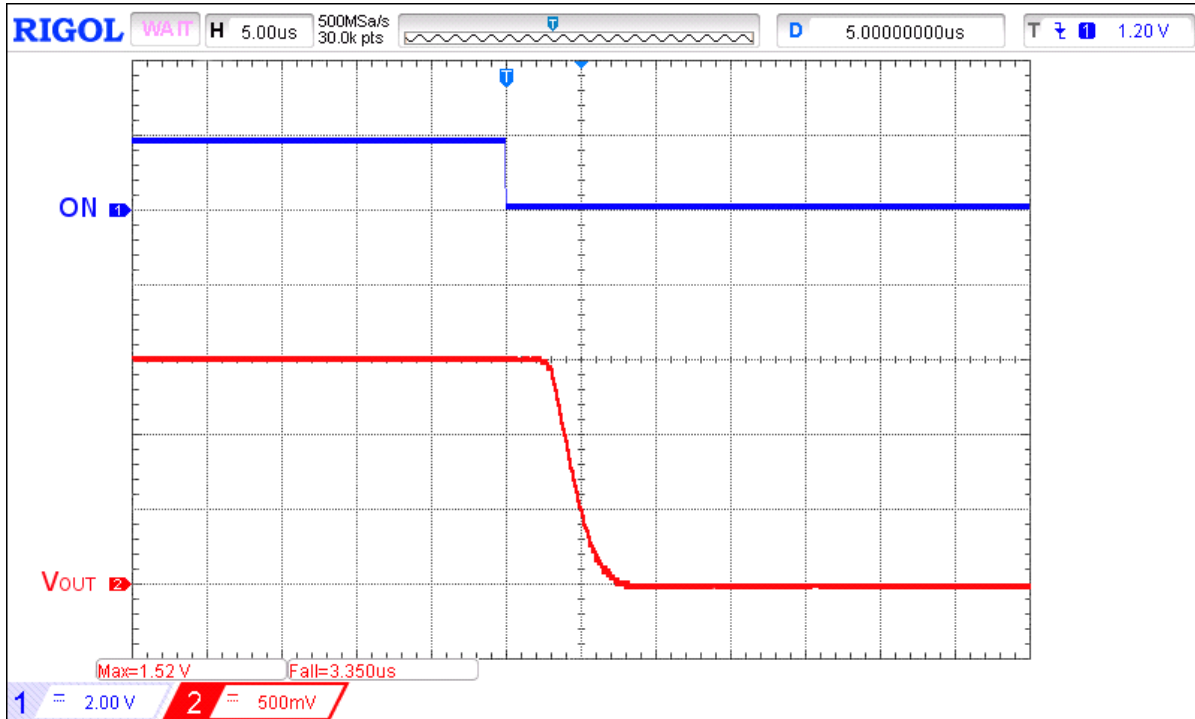

Figure 14. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Figure 15. Typical Turn OFF operation waveform for V_{DD} = 2.7 V, V_{IN} = 1.5 V, no C_{LOAD}, R_{LOAD} = 1 kΩ
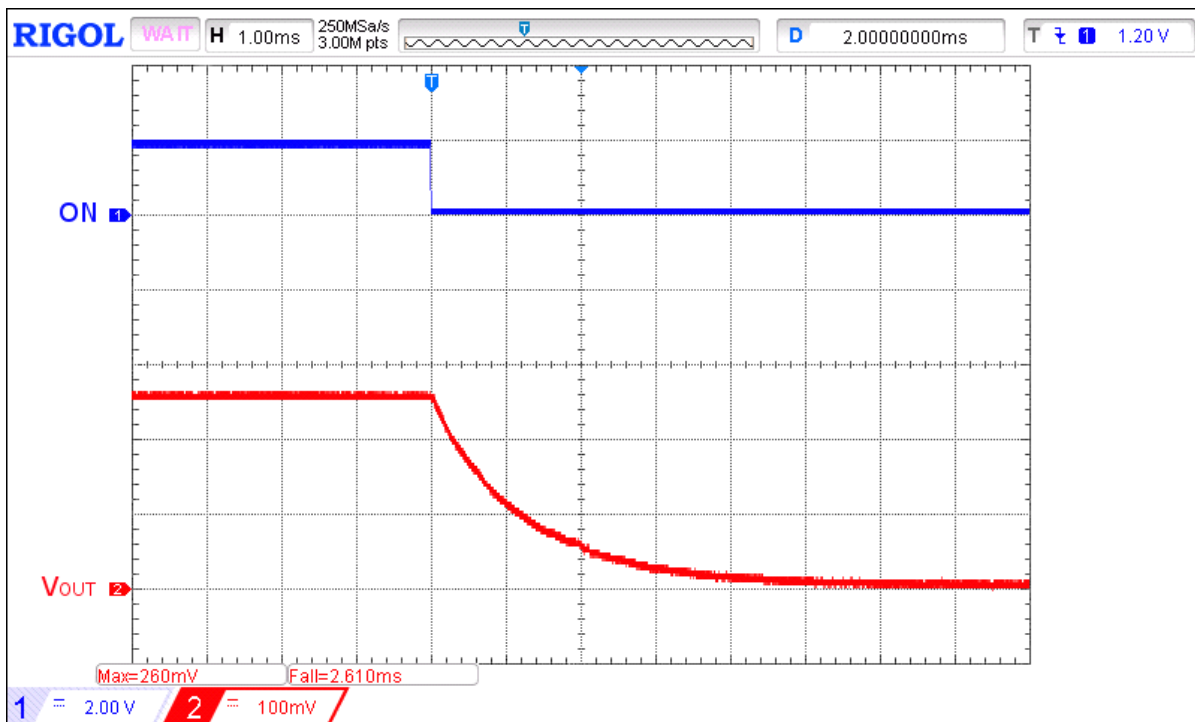

Figure 16. Typical Turn OFF operation waveform for V_{DD} = 3 V, V_{IN} = 0.25V, C_{LOAD} = 10 µF, R_{LOAD} = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
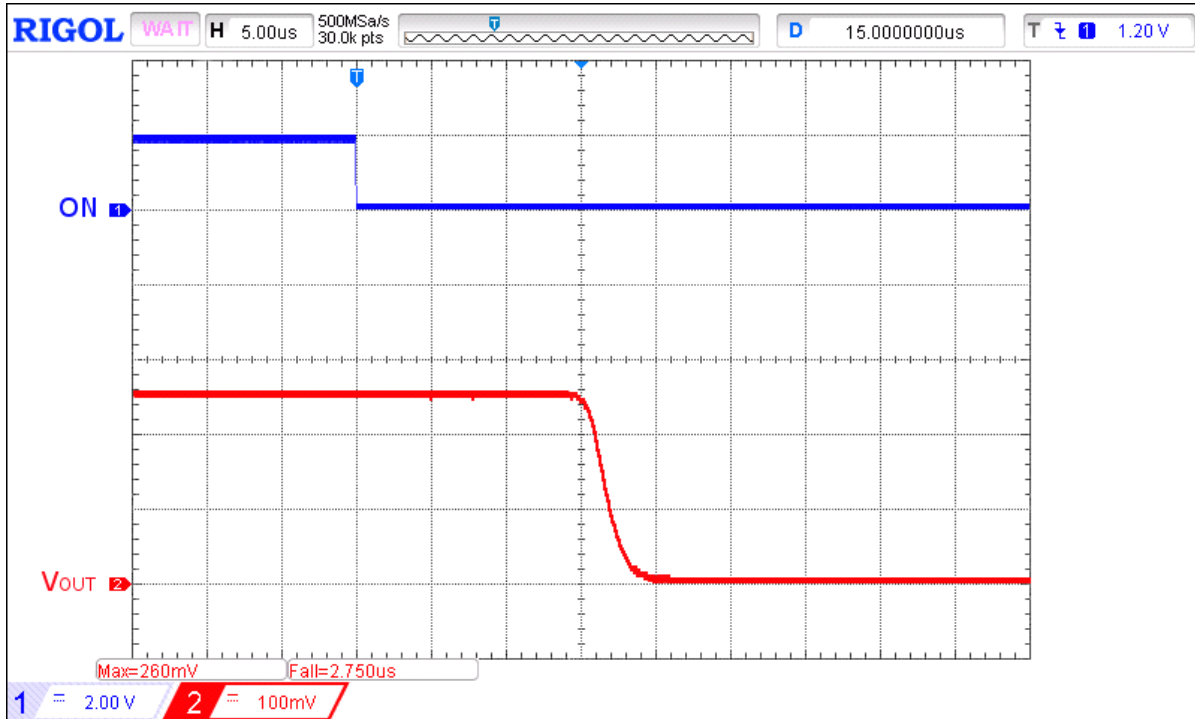Load Switch with Controlled Inrush Current

Figure 17. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 0.25 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
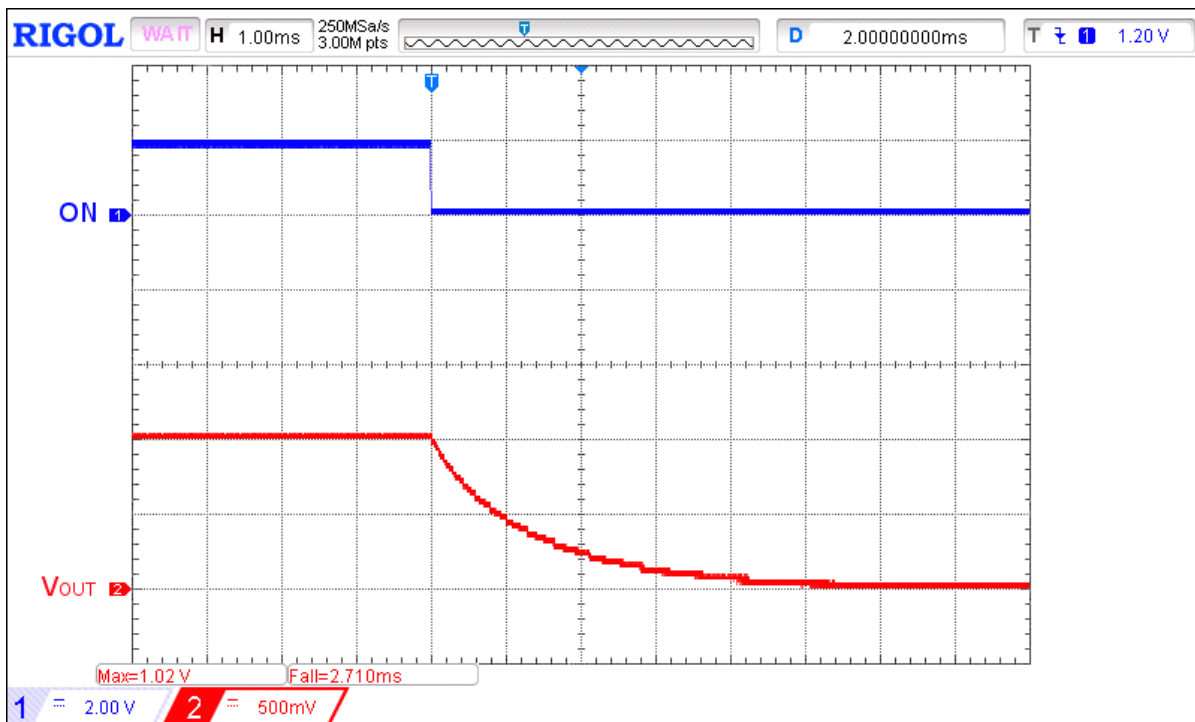
Figure 18. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current
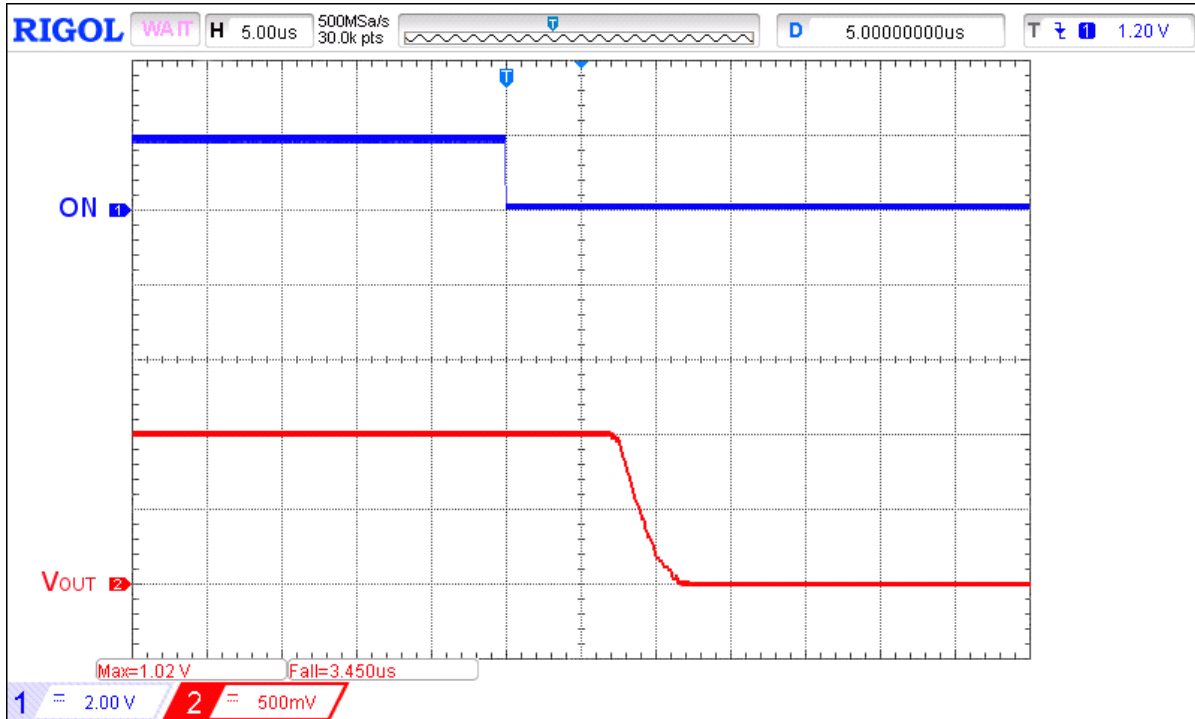
Figure 19. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
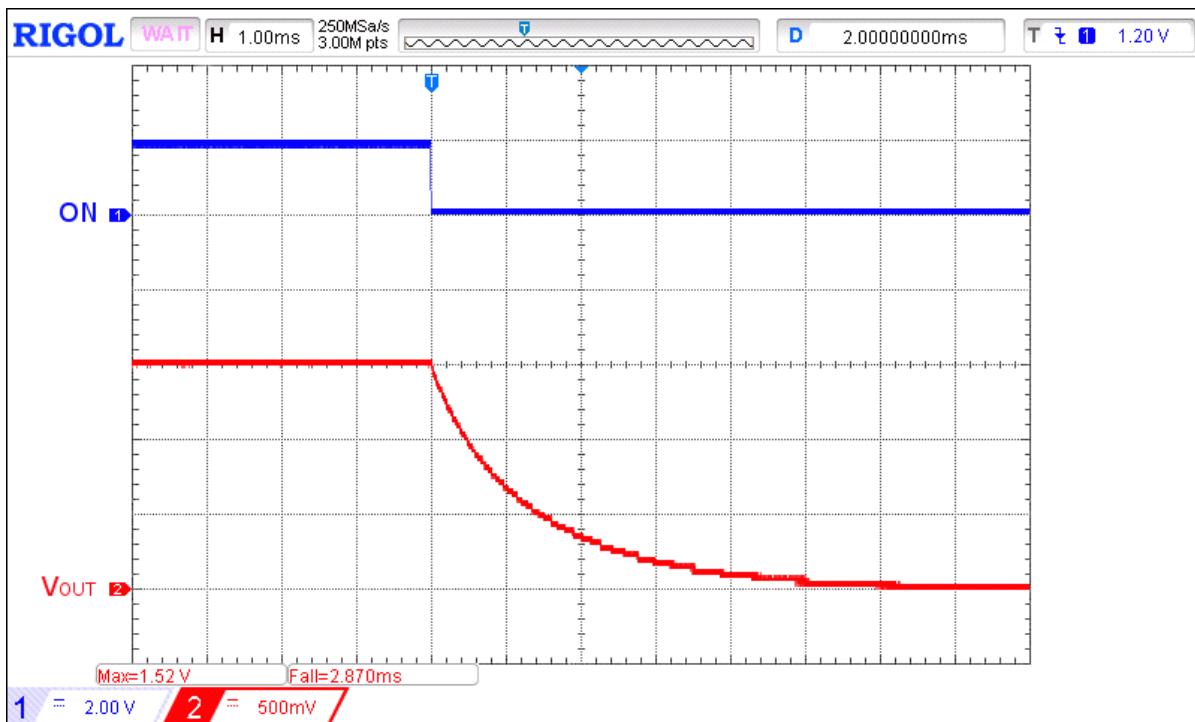
Figure 20. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

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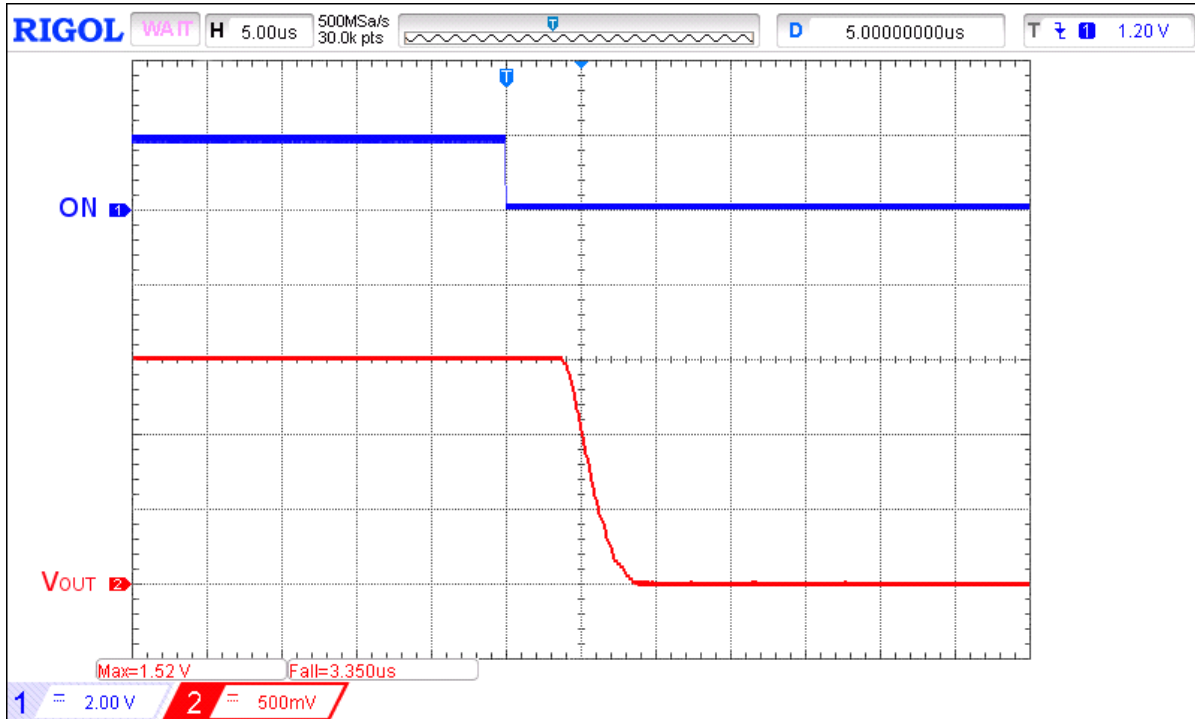
Figure 21. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1.5 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
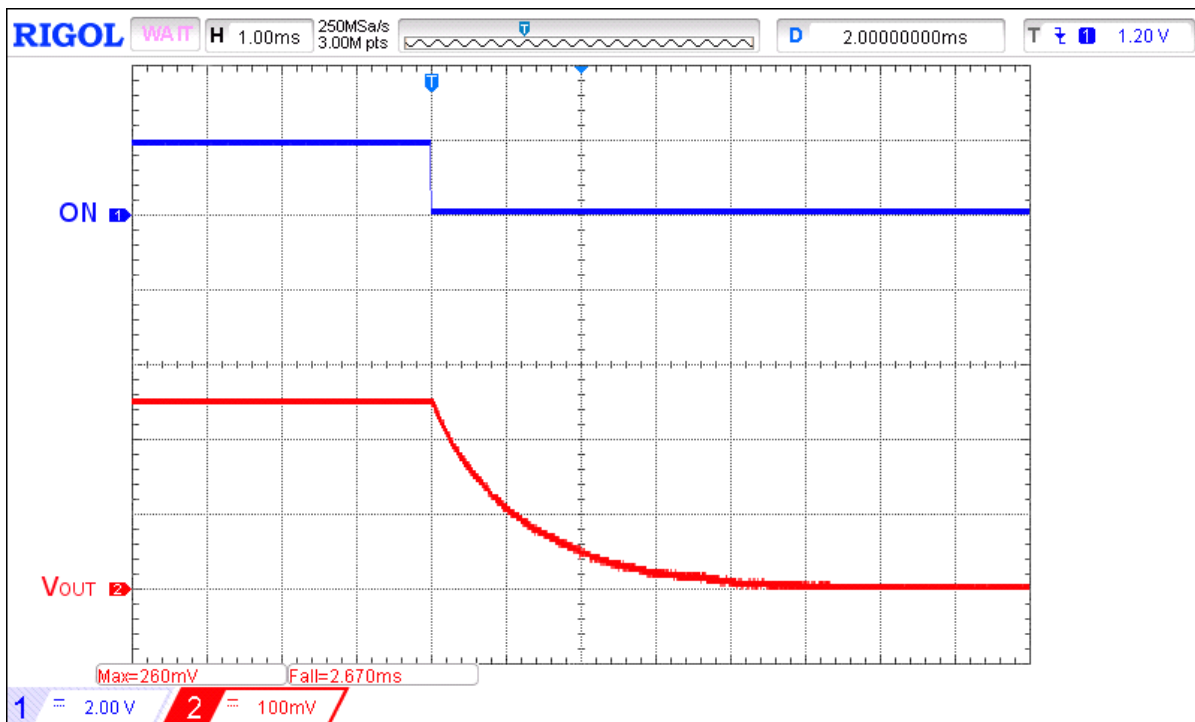
Figure 22. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Figure 23. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 0.25 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ

Figure 24. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current
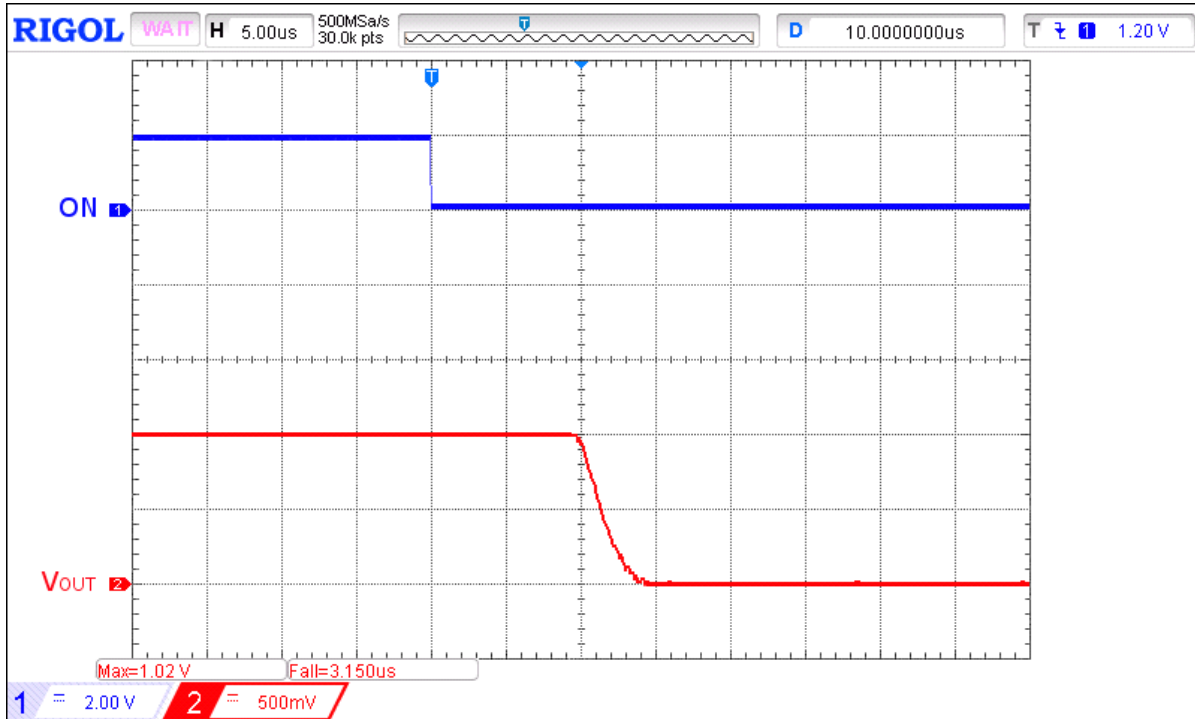
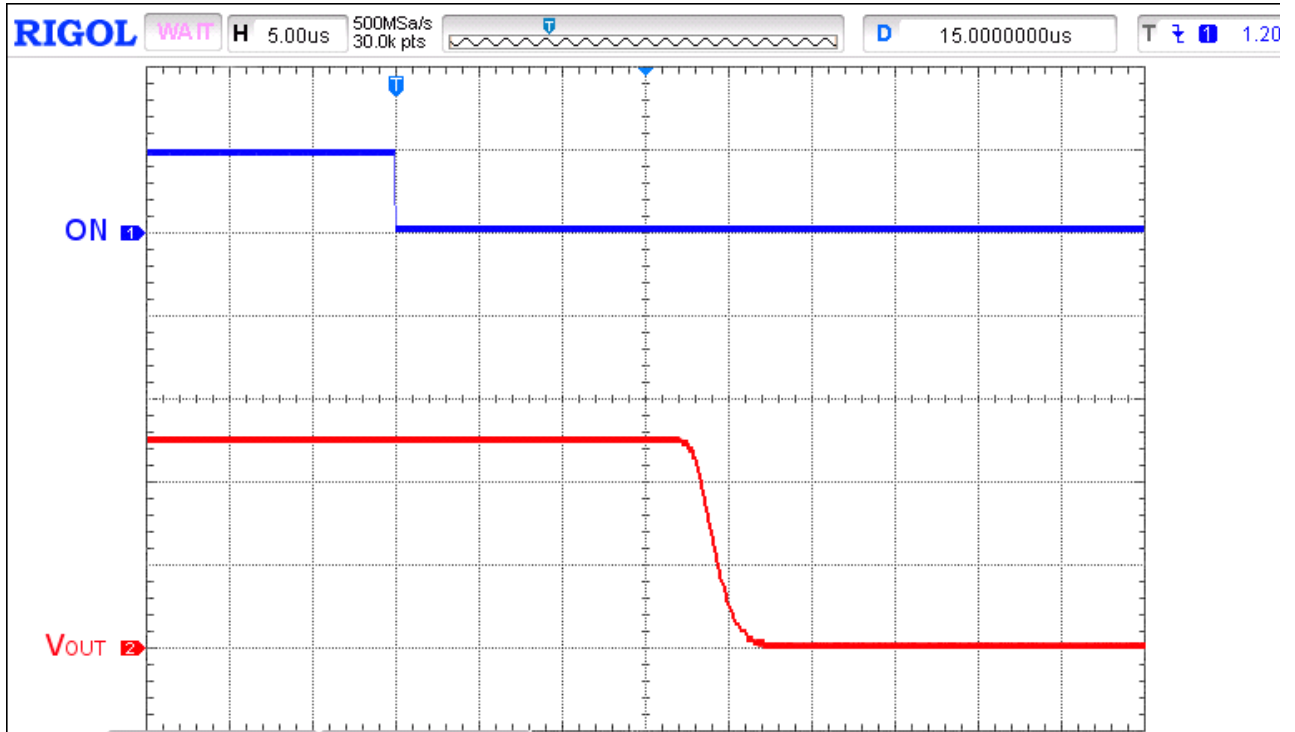Figure 25. Typical Turn OFF operation waveform for V_{DD} = 3.6 V, V_{IN} = 1 V, no C_{LOAD}, R_{LOAD} = 1 kΩ

Figure 26. Typical Turn OFF operation waveform for V_{DD} = 3.6 V, V_{IN} = 1.5 V, C_{LOAD} = 10 µF, R_{LOAD} = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Figure 27. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1.5 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
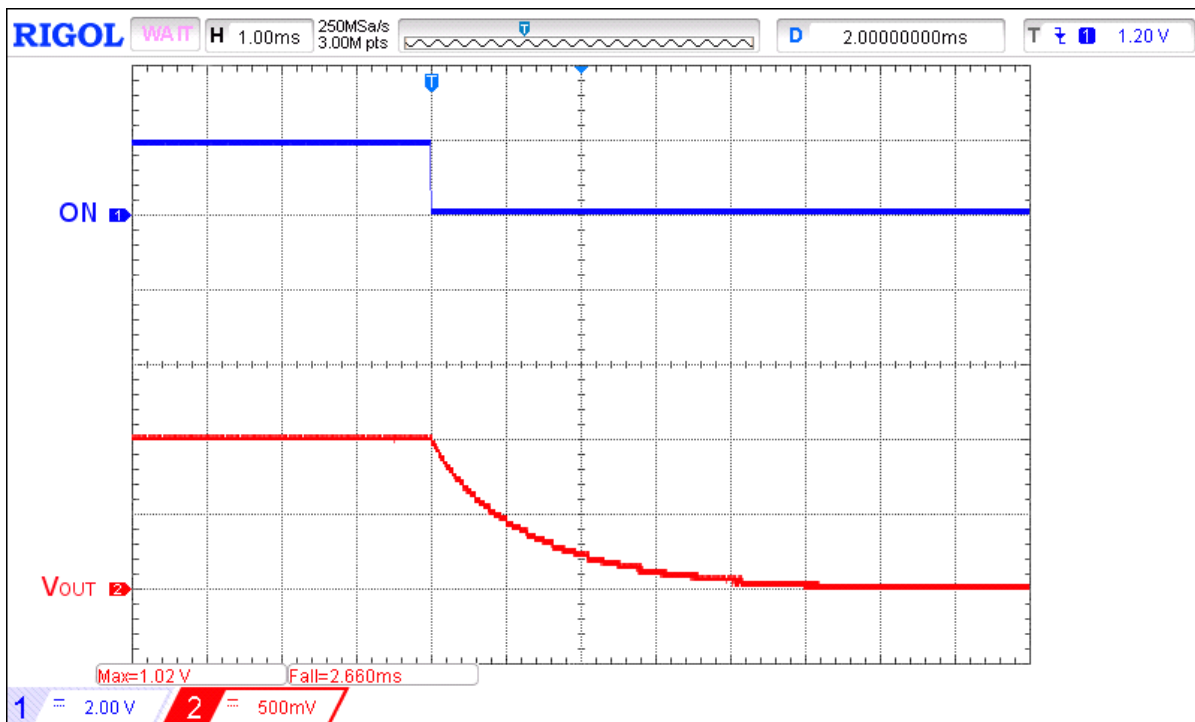
An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
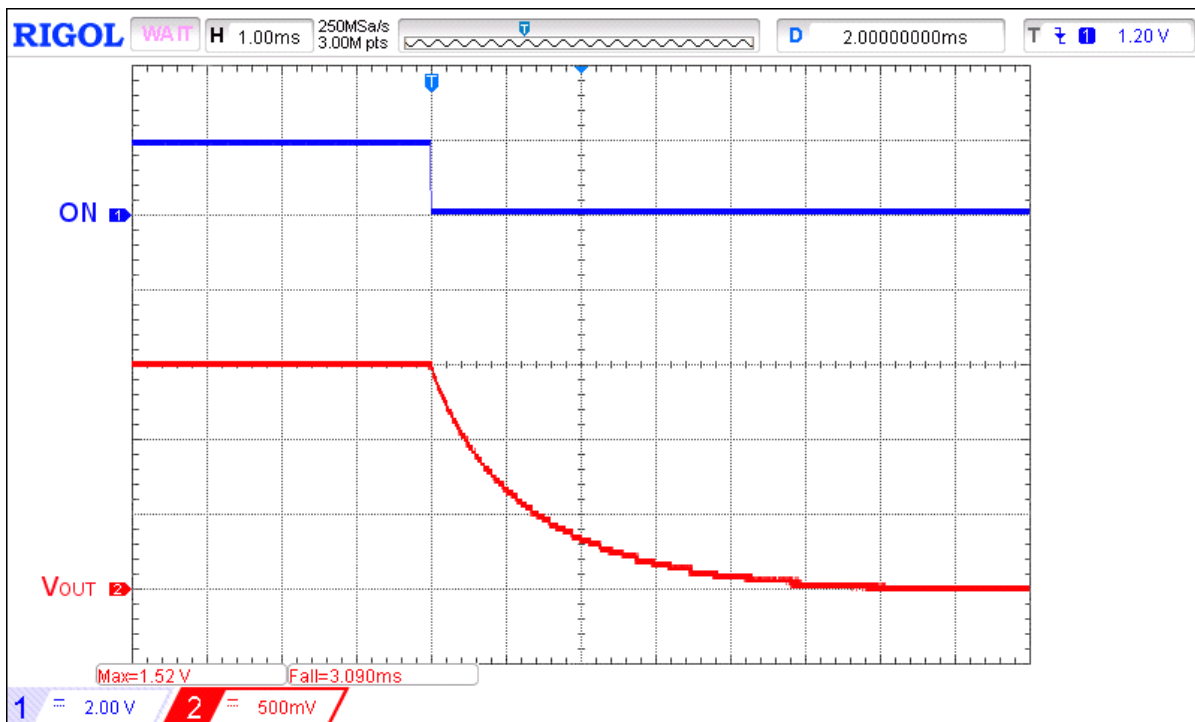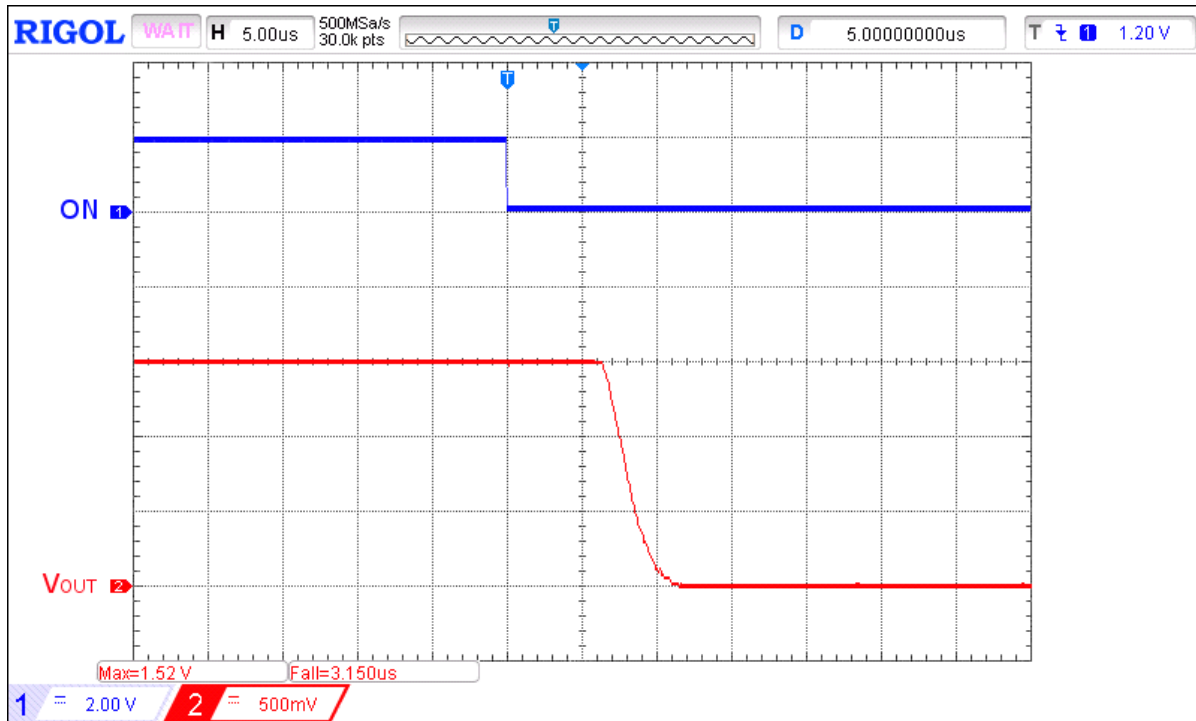Load Switch with Controlled Inrush Current

Applications Information

SLG59M1746C Power-Up/Power-Down Sequence Considerations

During V$_{DD}$ power-up operation, SLG59M1746C's internal circuitry is activated once V$_{DD}$ crosses 1 V, but the switch will not be turned on if ON = 0. Once V$_{DD}$ has reached 90% of its steady-state value (and within SLG59M1746C's nominal supply voltage range of 2.7 V to 3.6 V), the ON pin can then be toggled LOW-to-HIGH to close the switch.

A nominal power-up sequence is to apply V$_{DD}$ first, followed by V$_{IN}$ only after V$_{DD}$ is > 2.7 V, and finally toggling the ON pin LOW-to-HIGH after V$_{IN}$ is at least 90% of its final value.

If other power-up sequence is applied, the load switch can be turned on when ON is HIGH, but the behavior may differ from datasheet specifications.

A nominal power-down sequence is the power-up sequence in reverse order.

If V$_{DD}$ and V$_{IN}$ are applied at the same time, a voltage glitch may appear on the output pin at V$_{OUT}$. To prevent glitches at the output, it is recommended to connect at least 1 µF capacitor from the VOUT pin to GND and to keep the V$_{DD}$ & V$_{IN}$ ramp times higher than 2 ms.

As illustrated in the typical performance transient scope captures, the V$_{OUT}$ output follows a linear ramp when the load switch is turned on.

If ON and VDD are tied together and powered up, the load switch can be turned on, but the behavior may differ from datasheet specifications.

Power Dissipation

The junction temperature of the SLG59M1746C depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1746C is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2 + V_{DD} \times I_{DD\_Q2}$$

where:
PD = Power dissipation, in Watts (W)
RDS$_{ON}$ = Power MOSFET ON resistance, in Ohms (Ω)
I$_{DS}$ = Output current, in Amps (A)
V$_{DD}$ = Applied Supply Voltage, in Volts (V)
I$_{DD\_Q2}$ = IC's Supply Current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T$_J$ = Junction temperature, in Celsius degrees (°C)
θ$_{JA}$ = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T$_A$ = Ambient temperature, in Celsius degrees (°C)

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm² WLCSP
Load Switch with Controlled Inrush Current

Layout Guidelines:

1. The VDD pin (B2) needs a 0.1µF (or larger) external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG59M1746C's B2 pin.

2. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with <u>absolute minimum widths</u> of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 28, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1746C's VIN and VOUT pins;

4. The GND pin should be connected to system analog or power ground plane.

SLG59M1746C Evaluation Board:

A GreenFET Evaluation Board for SLG59M1746C is designed according to the statements above and is illustrated on Figure 28. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

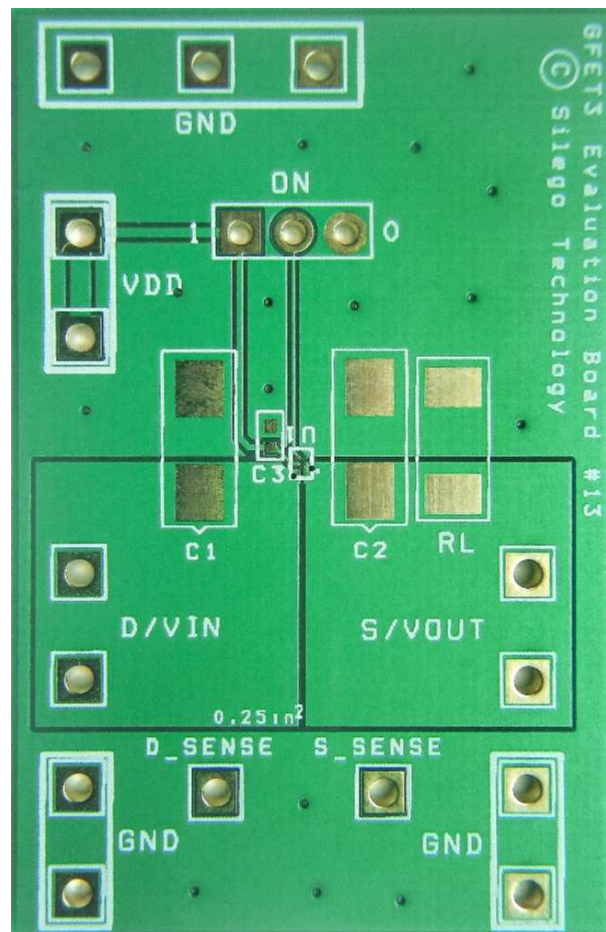**Figure 28. SLG59M1746C Evaluation Board**

An Ultra-low Power, RDS$_{ON}$ 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
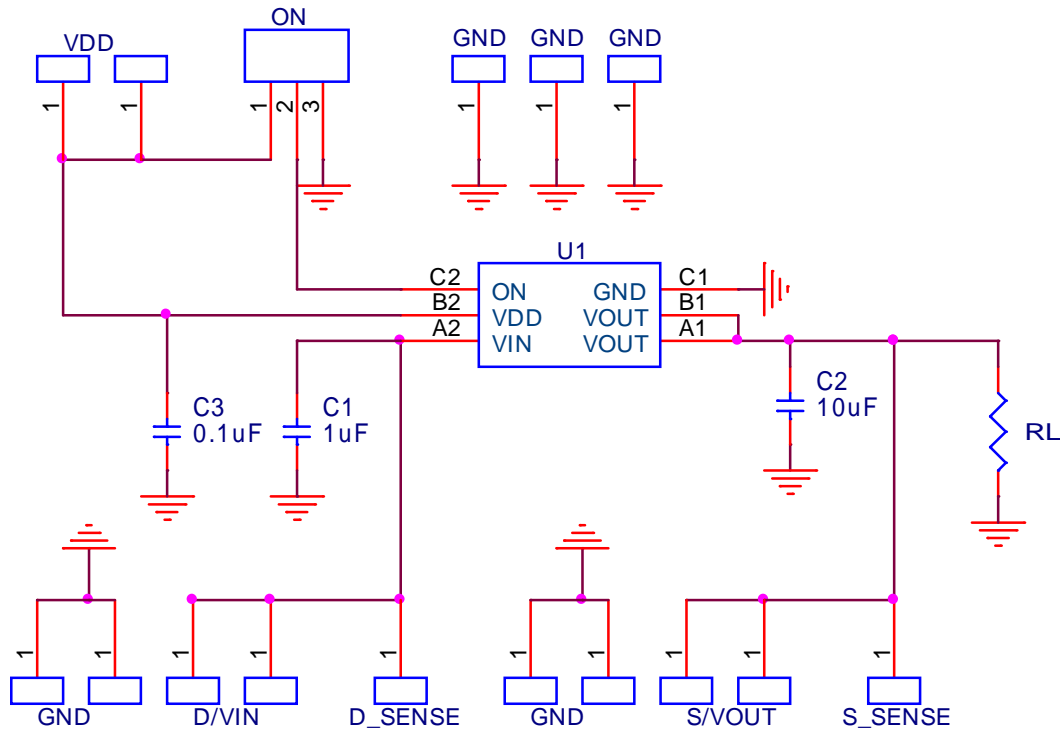Load Switch with Controlled Inrush Current

Figure 29. SLG59M1746C Evaluation Board Connection Circuit

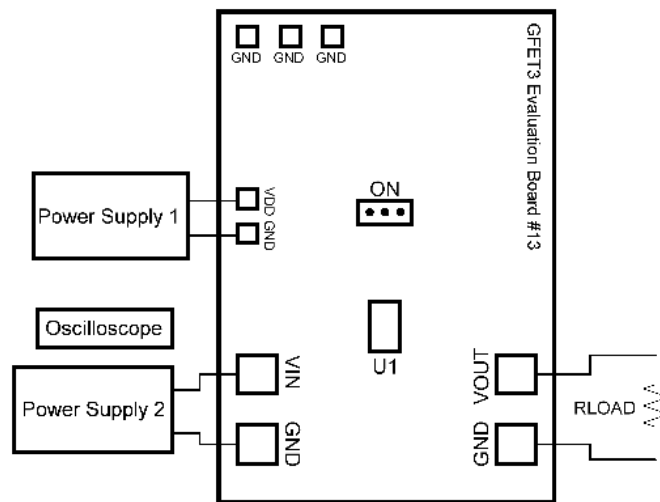## Basic Test Setup and Connections

Figure 30. SLG59M1746C Evaluation Board Connection Circuit

EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

2. Turn on Power Supply 1 and set desired V$_{DD}$ from 2.7 V…3.6 V range;

3. Turn on Power Supply 2 and set desired V$_{IN}$ from 0.25 V…1.5 V range;

4. Toggle the ON signal High or Low to observe SLG59M1746C operation.

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

Package Top Marking System Definition

```
┌─────────────────────┐
│                     │
│       ●NNN          │───── Serial Number Code
│                     │
Pin A1 Identifier      │
└─────────────────────┘
```

NNN - Serial Number Code Field[1]

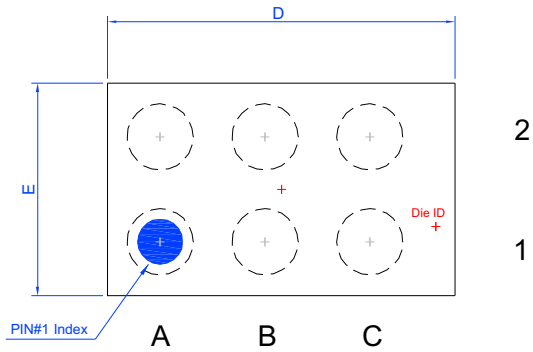Note 1: Each character in code field can be alphanumeric A-Z and 0-9

RENESAS

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
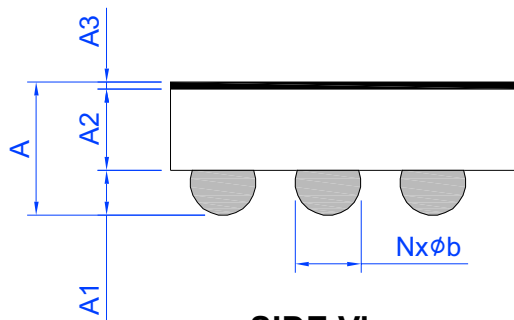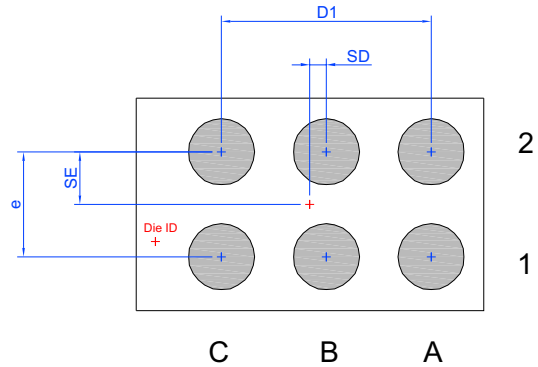Load Switch with Controlled Inrush Current

Package Drawing and Dimensions

6 Pin WLCSP Green Package 0.71 x 1.16 mm

Laser Marking View

Bump View

SIDE View

UNIT: mm							
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.390	0.445	0.500	D	1.130	1.160	1.190
A1	0.125	0.150	0.175	E	0.680	0.710	0.740
A2	0.245	0.270	0.295	e	0.35 BSC		
A3	0.020	0.025	0.030	D1	0.70 BSC		
b	0.195	0.220	0.245	SD	0.055 BSC		
N	6 (bump)			SE	0.175 BSC		

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP
Load Switch with Controlled Inrush Current

SLG59M1746C 6 Pin WLCSP PCB Landing Pattern

Exposed Bump
(Laser marking view)

Recommended
Land Pattern

1160

710

350

6X φ220

Die ID

700

55

350

175

6X φ185 ± 25

Ø185 Metal

50 max.

Solder mask
opening

Non-solder mask defined

50 min.

Metal under mask

Ø185
Solder mask opening

Solder mask defined
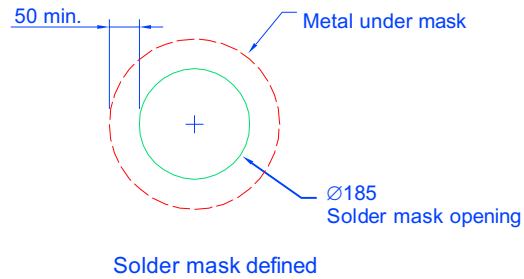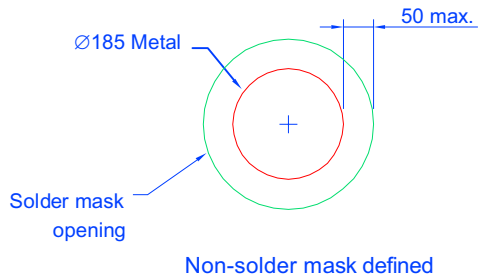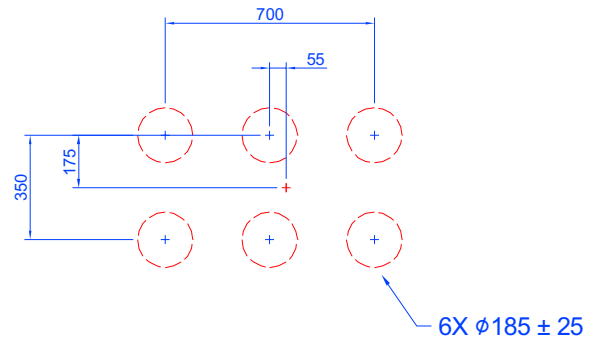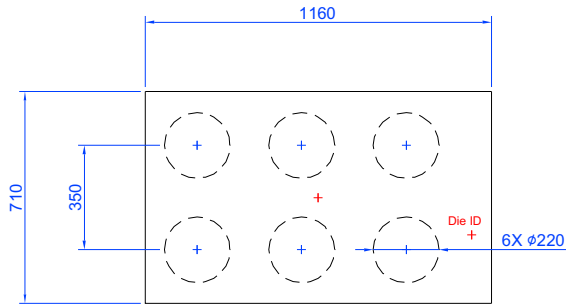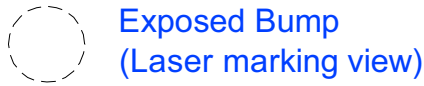
Solder mask detail (not to scale)

Unit: um

An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm² WLCSP
Load Switch with Controlled Inrush Current

Recommended Reflow Soldering Profile

For successful reflow of the SLG59M1746C a recommended thermal profile is illustrated below:
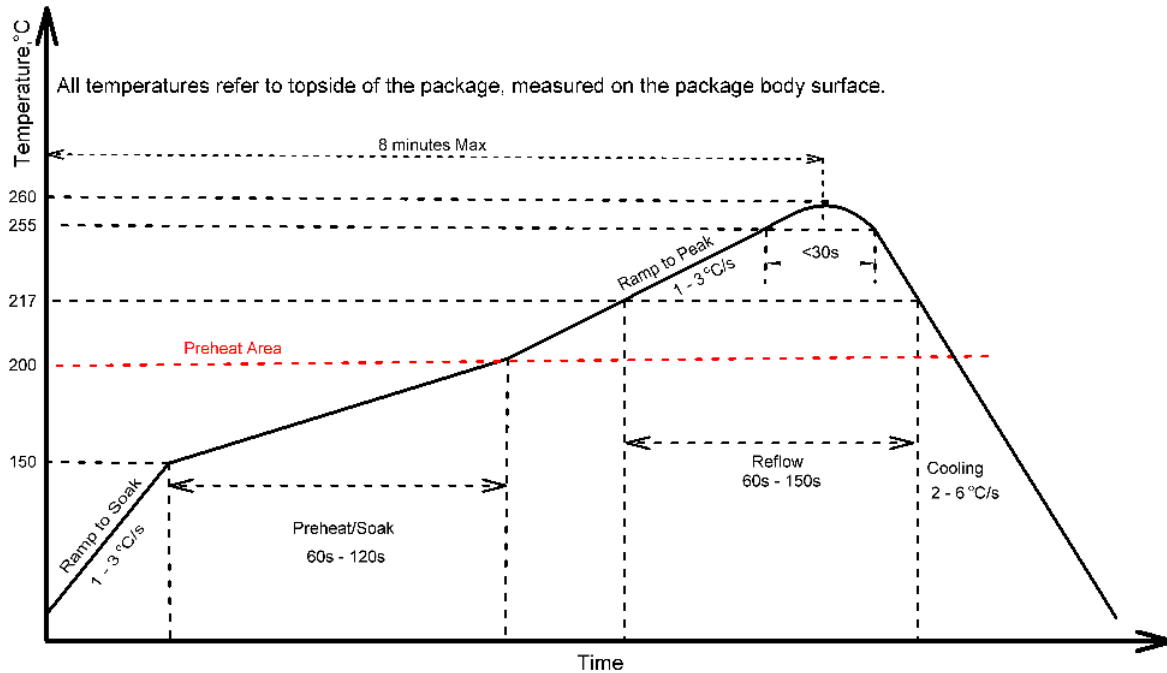
Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.242 mm³ (nominal).
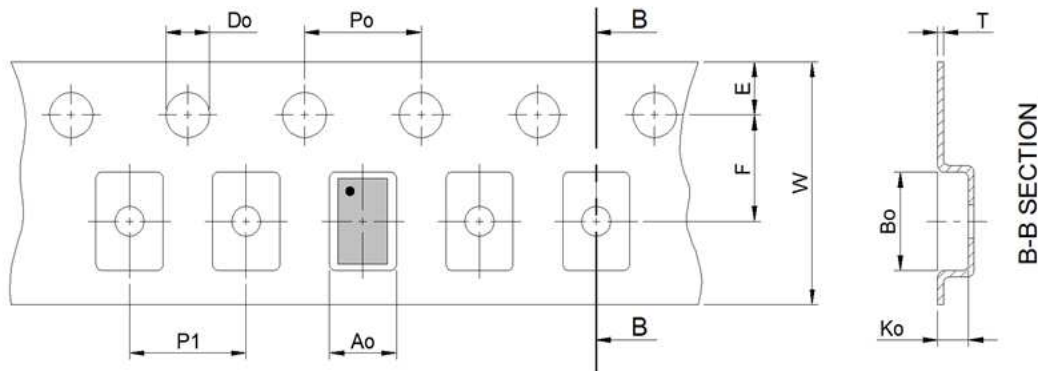
An Ultra-low Power, RDS_{ON} 17.6 mΩ, 1 A, 0.82 mm^2 WLCSP Load Switch with Controlled Inrush Current

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 6L 0.71 x 1.16 mm 0.35P Green	6	0.71 x 1.16	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
WLCSP 6L 0.71 x 1.16 mm 0.35P Green	0.77	1.22	0.53	4	4	1.5	1.75	3.5	0.2

Refer to EIA-481 specification

Revision History

Date	Version	Change
2/2/2022	1.02	Updated Company name and logo Fixed typos
3/25/2020	1.01	Fixed typos
3/20/2019	1.00	Production Release

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