EL9115

Triple Analog Video Delay Line

FN7441
Rev 7.00
January 12, 2012

The EL9115 is a triple analog delay line that allows skew compensation between any three signals. This part is perfect for compensating for the skew introduced by a typical CAT-5 cable with differing electrical lengths on each pair.

The EL9115 can be programmed in steps of 2ns up to 62ns total delay on each channel.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
EL9115ILZ	9115ILZ	20 Ld 5mmx5mm QFN	L20.5x5C

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to Tech Brief TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for EL9115. For more information on MSL, please see Tech Brief TB363.

Features

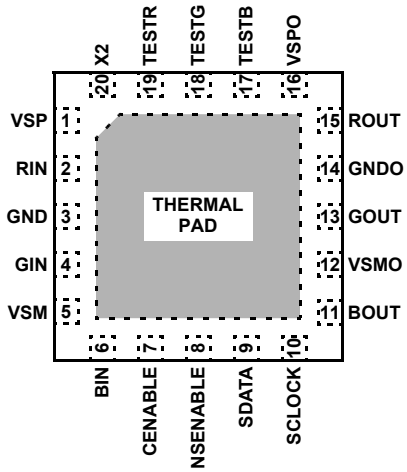
- 62ns total delay
- 2ns delay step increments
- Operates from ±5V supply
- Up to 122MHz bandwidth
- Low power consumption
- 20 Ld QFN (5mmx5mm) package
- Pb-free (RoHS compliant)

Applications

- Skew control for RGB
- Analog beamforming

Pinout

EL9115
(20 LD 5X5 QFN)
TOP VIEW



EXPOSED DIEPLATE SHOULD BE CONNECTED TO -5V

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_S+ to V_S-) 12V
Maximum Output Current. . . . . ±60mA
Storage Temperature Range . . . . . .-65°C to +150°C

Operating Conditions

Operating Junction Temperature . . . . . .+135°C
Ambient Operating Temperature . . . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
20 Ld QFN Package (Note 4). 32
Power Dissipation . . See "Typical Performance Curves" on page 4.
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

DC Electrical Specifications

V_{SA}+ = V_A+ = +5V, V_{SA}- = V_A- = -5V, T_A = +25°C, exposed die plate = -5V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
V+	Positive Supply Range		+4.5		+5.5	V
V-	Negative Supply Range		-4.5		-5.5	V
G_0	Gain Zero Delay	X2 = 5V, 150Ω load	1.81	1.9	2.04	
G_m	Gain Mid Delay		1.64	1.8	1.97	
G_f	Gain Full Delay		1.46	1.7	1.97	
DG_m0	Difference in Gain, 0 to Mid		-10	-4	2.3	%
DG_f0	Difference in Gain, 0 to Full		-17.5	-9	0.3	%
DG_fm	Difference in Gain, Mid to Full		-15	-5	4	%
V_{IN}	Input Voltage Range	Gain falls to 90% of nominal	-0.7		1.2	V
I_B	Input Bias Current			1	5	µA
R_{IN}	Input Resistance			10		MΩ
V_{OS_0}	Output Offset 0 Delay	X2 = +5V, 75 + 75Ω load	-90	0	90	mV
V_{OS_M}	Output Offset Mid Delay		-90	0	90	mV
V_{OS_F}	Output Offset Full Delay		-90	0	90	mV
Z_{OUT}	Output Impedance	Chip enable = +5V	4.5	5	6.3	Ω
		Chip enable = 0V		1		MΩ
+PSRR	Rejection of Positive Supply	X2 = +5V into 75 + 75Ω load		-38		dB
-PSRR	Rejection of Negative Supply	X2 = +5V into 75 + 75Ω load		-53		dB
I_{SP}	Supply Current (Note 5)	Chip enable = +5V current on V_{SP}	75	87	115	mA
I_{SM}	Supply Current (Note 5)	Chip enable = +5V current in V_{SM}	-15.25	-12.5	-9.75	mA
I_{SMO}	Supply Current (Note 5)	Chip enable = +5V current in V_{SMO}	-15.25	-13	-11	mA
I_{SPO}	Supply Current (Note 5)	Chip enable = +5V current in V_{SPO}	10	11.8	15.5	mA
ΔI_{SP}	Supply Current (Note 5)	Increase in I_{SP} per unit step in delay		0.9		mA
$I_{SP\ OFF}$	Supply Current (Note 5)	Chip enable = 0V current in V_{SP}		1.6		mA
I_{OUT}	Output Drive Current	10Ω load, 0.5V drive, X2 = 5V	40			mA
L_{HI}	Logic High	Switch high threshold		1.25	1.6	V
L_{LO}	Logic Low	Switch low threshold	0.8	1.15		V

AC Electrical Specifications $V_{SA}+ = V_A+ = +5V$, $V_{SA}- = V_A- = -5V$, $T_A = +25°C$, exposed die plate = -5V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 5)	TYP	MAX (Note 5)	UNIT
BW -3dB	3dB Bandwidth	0ns Delay Time		122		MHz
BW 0.1dB	0.1dB Bandwidth	0ns Delay Time		60		MHz
SR	Slew Rate	0ns Delay Time		400		V/µs
t_R - t_F	Transient Response Time	20% to 80%, for all delays, 1V step		2.5		ns
V_{OVER}	Voltage Overshoot	For any delay, response to 1V step input		5		%
Glitch	Switching Glitch	Time for o/p to settle after last s_clock edge		100		ns
THD	Total Harmonic Distortion	$1V_{P-P}$ 10MHz sinewave, offset by +0.2V at mid delay setting		-50	-40	dB
X_t	Hostile Crosstalk	Stimulate G, measure R/B at 1MHz		-80		dB
V_N	Output Noise	Gain X2, measured at 75Ω load		2.5		mV_{RMS}
d_t	Nominal Delay Increment	Note 7	1.75	2	2.25	ns
t_{MAX}	Maximum Delay		55	62	70	ns
D_{ELDT}	Delay Diff Between Channels			1.6		%
t_{PD}	Propagation Delay	Measured input to output		9.8		ns
t_{MAX}	Max s_clock Frequency	Maximum programming clock speed			10	MHz
t_en_ck	Minimum Separation Between Serial Enable and Clock	Check enable low edge can occur after t_en_ck of previous (ignored) clock and up to before t_en_ck of next (wanted) clock. Clock edges occurring within t_en_ck of the enable edge will have uncertain effect.		10		ns

NOTES:

5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. All supply currents measured with Delay R = 0ns, G = mid delay, B = full delay.
7. Delay increment limits are derived by taking Maximum Delay limits and dividing by the number of steps for the device (e.g., the number of steps for the EL9115 is 31).

Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VSP	+5V for delay circuitry and input amp
2	RIN	Red channel input, ref GND
3	GND	0V for delay circuitry supply
4	GIN	Green channel input, ref GND
5	VSM	-5V for input amp
6	BIN	Blue channel input, ref GND
7	CENABLE	Chip enable logical +5V enables chip
8	NSENABLE	$\overline{\text{ENABLE}}$ for serial input; enable on low
9	SDATA	Data into registers; logic threshold 1.2V
10	SCLOCK	Clock to enter data; logical; data written on negative edge
11	BOUT	Blue channel output, ref GND_O
12	VSMO	-5V for output buffers
13	GOUT	Green channel output, ref GND_O
14	GNDO	0V reference for input and output buffers
15	ROUT	Red channel output, ref GND_O
16	VSPO	+5V for output buffers

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	PIN DESCRIPTION
17	TESTB	Blue channel phase detector output
18	TESTG	Green channel phase detector output
19	TESTR	Red channel phase detector output
20	X2	Sets gain to 2X if input high; X1 otherwise
Thermal Pad		Must be connected to -5V

Typical Performance Curves

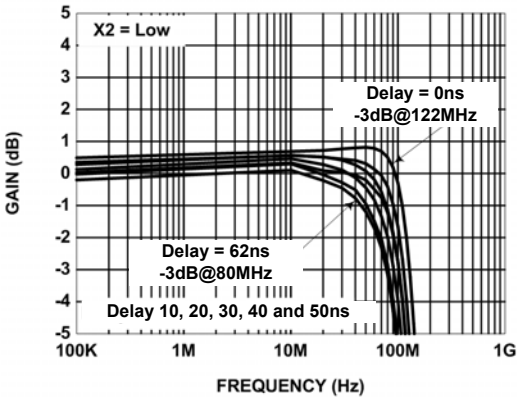


FIGURE 1. GAIN vs FREQUENCY

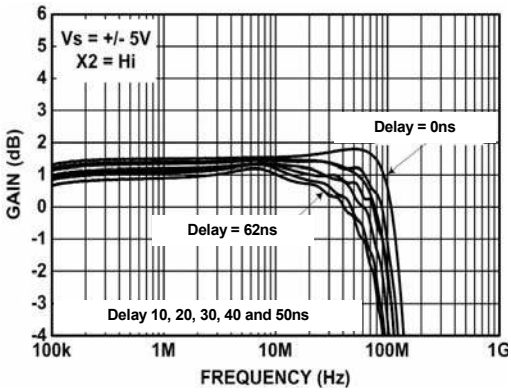


FIGURE 2. GAIN vs FREQUENCY

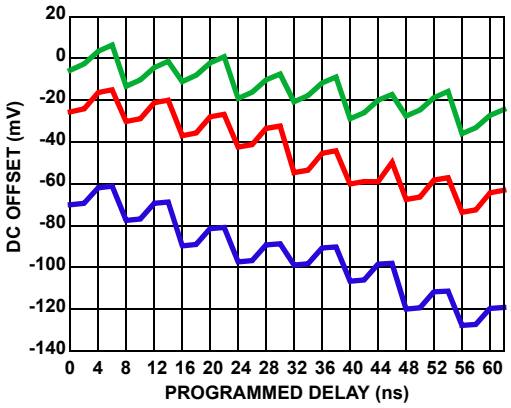


FIGURE 3. DC OFFSET vs DELAY TIME (GAIN = 2X)

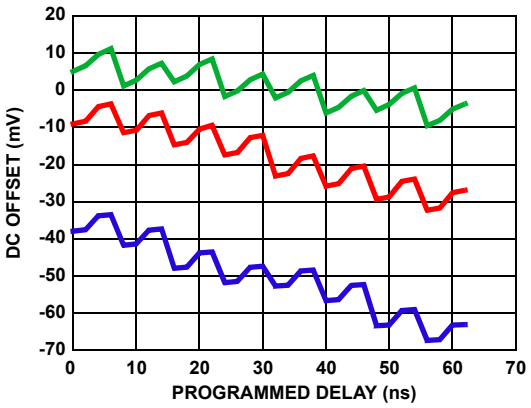


FIGURE 4. DC OFFSET vs DELAY TIME (GAIN = 1X)

Typical Performance Curves (Continued)

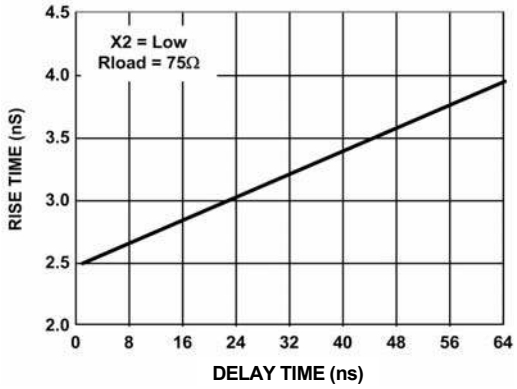


FIGURE 5. RISE TIME vs DELAY TIME

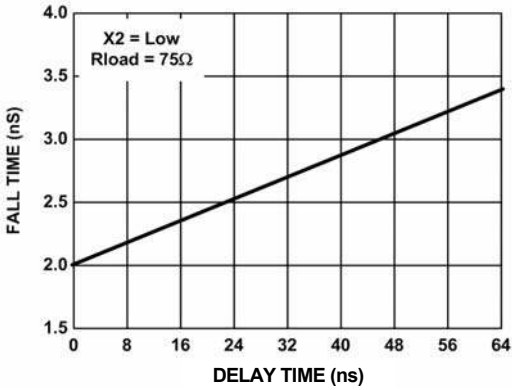


FIGURE 6. FALL TIME vs DELAY TIME

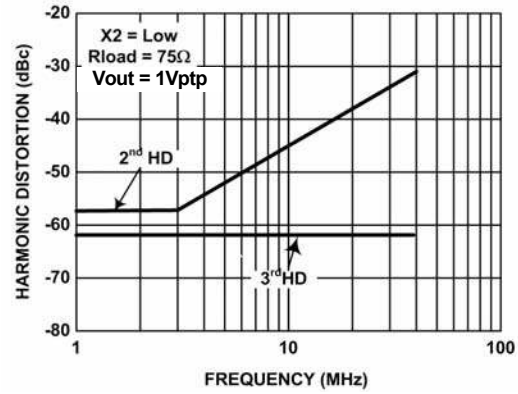


FIGURE 7. DISTORTION vs FREQUENCY

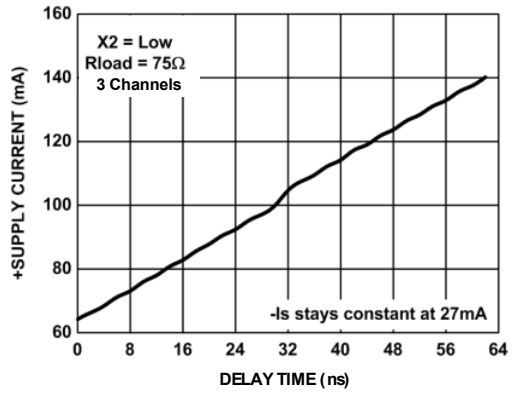


FIGURE 8. POSITIVE SUPPLY CURRENT vs DELAY TIME

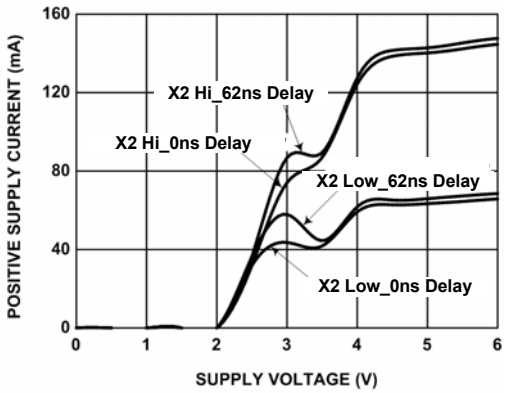


FIGURE 9. $I_{SUPPLY}+$ vs $V_{SUPPLY}+$

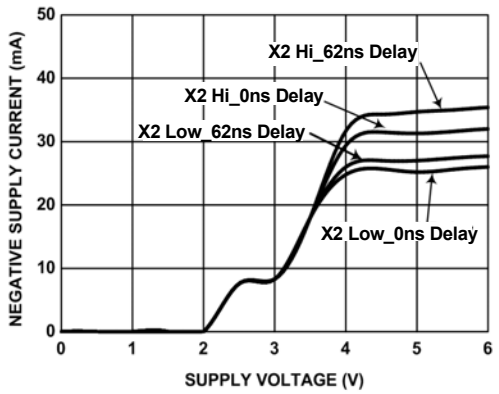


FIGURE 10. $I_{SUPPLY}-$ vs $V_{SUPPLY}-$

Typical Performance Curves (Continued)

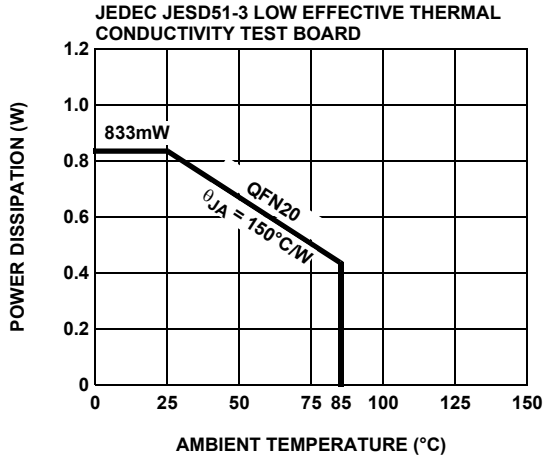


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

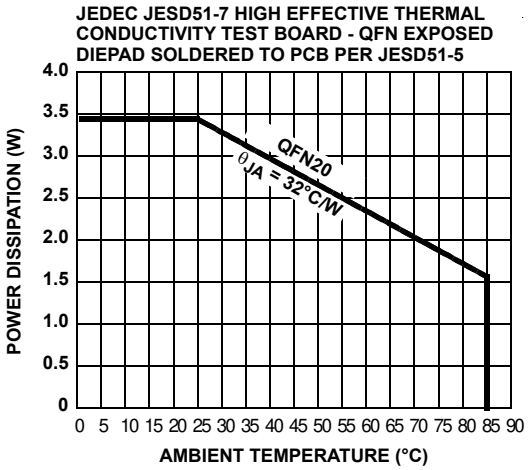


FIGURE 12. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

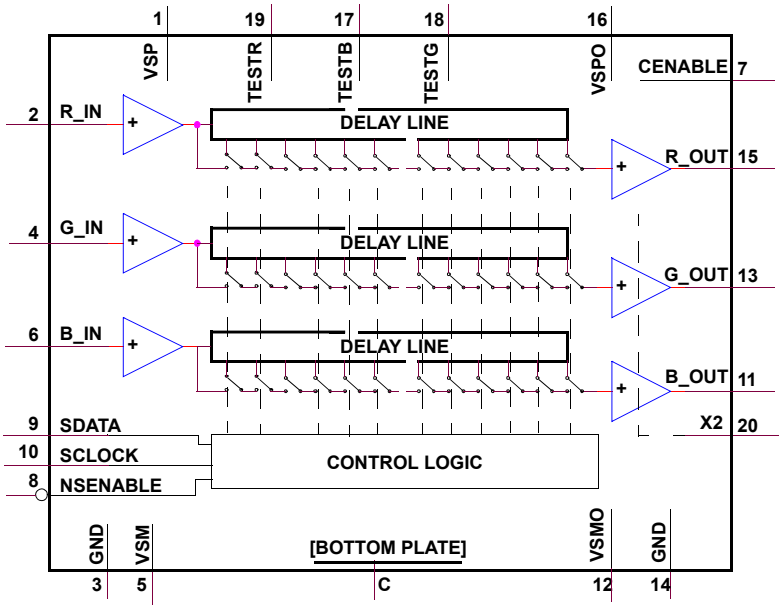


FIGURE 13. EL9115 BLOCK DIAGRAM

Applications Information

EL9115 is a triple analog delay line receiver that allows skew compensation between any three high frequency signals. This part compensates for time skew introduced by a typical CAT-5 cable with differing electrical lengths on each pair. The EL9115 can be independently programmed via SPI interface in steps of 2ns up to 62ns total delay on each channel while achieving over 80MHz bandwidth.

Figure 13 shows the EL9115 block diagram. The three analog inputs are ground reference single-ended signals. After the signal is received, the delay is introduced by switching filter blocks into the signal path. Each filter block is an all-pass filter introducing 2ns delay. In addition to time delay, each filter block also introduces some low pass filtering. As a result, the bandwidth of the signal path decreases from 120MHz at 0ns delay setting to 80MHz at the maximum delay setting, as shown in Figure 1 of the “Typical Performance Curves” on page 4.

In addition to delay, the extra amplifiers in the signal path also introduce offset voltage. The output offset voltage can shift by 100mV for X2 high setting and 50mV for X2 low.

In operation, it is best to allocate the most delayed signal 0ns delay and then increase the delay on the other channels to bring them into line. This will result in the lowest power and distortion solution to balancing delays.

Power Dissipation

As the delay setting increases, additional filter blocks turn on and insert into the signal path. For each 2ns of delay per channel, V_{SP} current increases by 0.9mA while V_{SM} does not change significantly. Under the extreme settings, the positive supply current reaches 140mA and the negative supply current can be 35mA. Operating at ±5V power supply, the total power dissipation is as shown in Equation 1:

$$PD = 5 \bullet 140mA + 5 \bullet 35mA = 875mW \quad \text{(EQ. 1)}$$

θ_{JA} required for long term reliable operation can be calculated. This is done using Equation 2:

$$\theta_{JA} = (T_J - T_A)/PD = 57°C/W \quad \text{(EQ. 2)}$$

where:

T_J is the maximum junction temperature (+135°C)

T_A is the maximum ambient temperature (+85°C)

For a 20 Ld package in a proper layout PCB heat-sinking copper area, 40°C/W θ_{JA} thermal resistance can be achieved. To disperse the heat, the bottom heat-spreader must be soldered to the PCB. Heat flows through the heat-spreader to the circuit board copper then spreads and convects to air. Thus, the PCB copper plane becomes the heatsink (see TB389). This has proven to be a very effective technique. A separate application note, which details the 20 Ld QFN PCB design considerations, is available.

TABLE 1. SERIAL BUS DATA

vwxyz	DELAY
00000	0
00001	2
00010	4
00011	6
00100	8
00101	10
00110	12
00111	14
01000	16
01001	18
01010	20
01011	22
01100	24
01101	26
01110	28
01111	30
10000	32
10001	34
10010	36
10011	38
10100	40
10101	42
10110	44
10111	46
11000	48
11001	50
11010	52
11011	54
11100	56
11101	58
11110	60
11111	62

NOTE: Delay register word = 0abvwxyz; Red register - ab = 01; Green register - ab = 10; Blue register - ab = 11; vwxyz selects delay.

Serial Bus Operation

On the first negative clock edge after NSEnable goes low, read the input from DATA (Figure 14). This DATA level should be 0 (write into registers); READ is not supported. Read the next two data bits on subsequent negative edges and interpret them as the register to be filled. Reg 01 = R, 02 = G, 03 = B, 00 test use. Read the next five bits of data and send them to register. At the end of each block of 8 bits, any further data is treated as being a new word. Data entered is shifted directly to the final

registers as it is clocked in. Initial value of all registers on power-up is 0. It is the user's responsibility to send complete patterns of 8 clock cycles, even if the first bit is set to 1. If less than 8 bits are sent, data will only be partially shifted through the registers. The pattern of 8 starts with NSEnable going low, so it is good practice to frame each word within an NS enable burst.

Test Pins

Three test pins are provided (Test R, Test G, Test B). During normal operation, the test pins output pulses of current for a duration of the overlap between the inputs, as shown in Figure 15:

Test_R pulse = Red out (A) wrt Green out (B)

Test_G pulse = Green out wrt Blue out

Test_B pulse = Blue out wrt Red out

Averaging the current gives a direct measure of the delay between the two edges. When A precedes B the current pulse is +50µA, and the output voltage goes up. When B precedes A, the pulse is -50µA.

For the logic to work correctly, A and B must have a period of overlap while they are high (a delay longer than the pulse width cannot be measured).

Signals A and B are derived from the video input by comparing the video signal with a slicing level, which is set by an internal DAC. This enables the delay to be measured either from the rising edges of sync-like signals encoded on top of the video or from a dedicated set-up signal. The outputs can be used to set the correct delays for the signals received.

The DAC level is set through the serial input by bits 1 through 4 directed to the test register (00). Table 2 shows the settings for the DAC slice level bits.

Test Mode

Bit zero of the test register is set to 0 for normal operation. If it is set to 1 then the device is in Test Mode. In Test Mode, the DAC voltage is directed to the Green channel output, while for the Red and Blue channels, the test outputs are now pulses of current which are generated by looking at the delay between the input and output of the channel. They thus enable the delay to be measured.

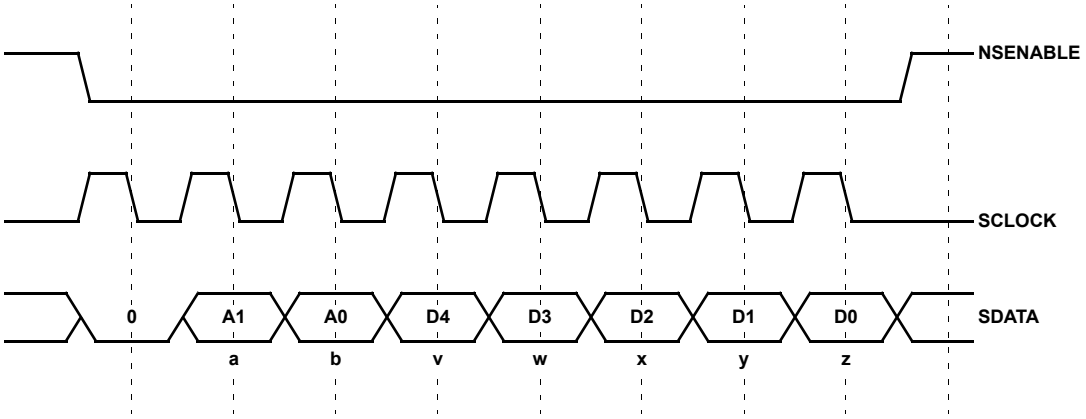


FIGURE 14. SERIAL DATA TIMING

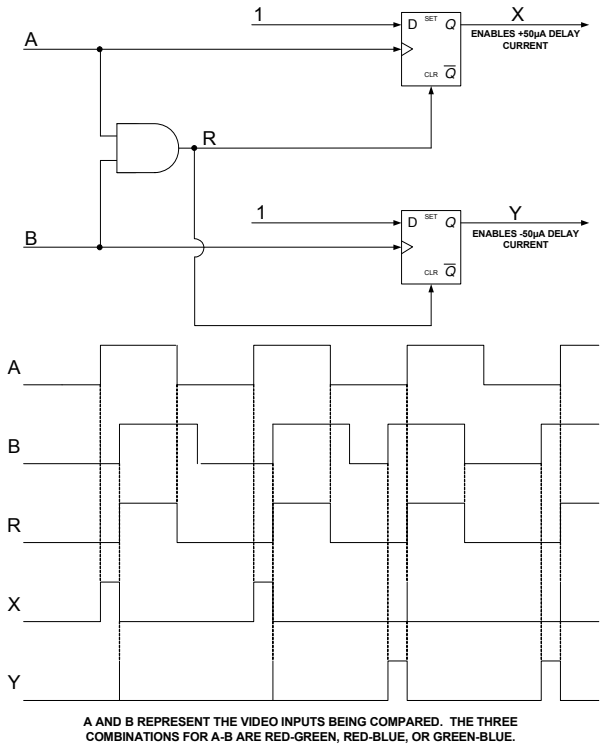


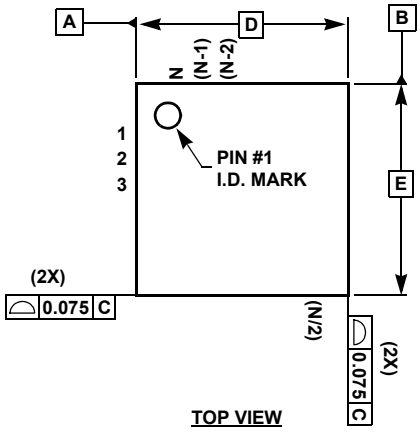
FIGURE 15. DELAY DETECTOR

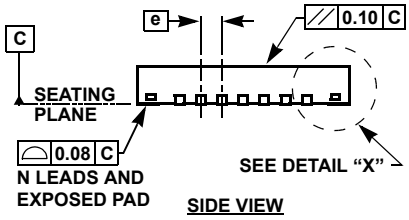
TABLE 2. DAC SLICE LEVEL SETTINGS

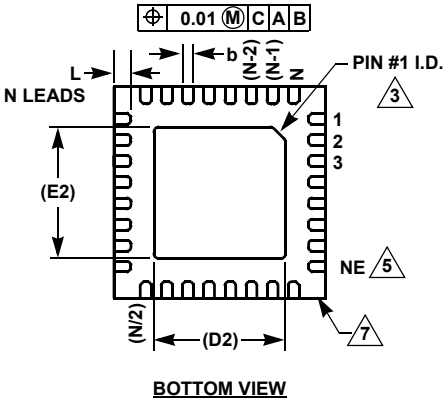
wxyz	DAC/mV
1000	-400
1001	-350
1010	-300
1011	-250
1100	-200
1101	-150
1110	-100
1111	-50
0000	0
0001	50
0010	100
0011	150
0100	200
0101	250
0110	300
0111	350

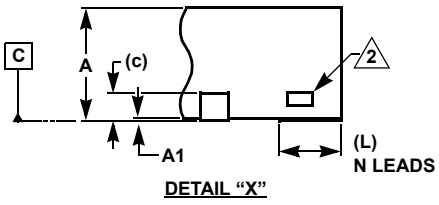
NOTE: Test Register word = 000wxyzt. If t = 1 test mode else normal. wxyz fed to DAC. z is LSB

Quad Flat No-Lead Plastic Package (QFN)









L20.5x5C

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.05	-
b	0.28	0.30	0.32	-
c		0.20 REF		-
D		5.00 BASIC		-
D2		3.70 REF		8
E		5.00 BASIC		-
E2		3.70 REF		8
e		0.65 BASIC		-
L	0.35	0.40	0.45	-
N		20		4
ND		5 REF		6
NE		5 REF		5

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NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.
9. One of 10 packages in MDP0046