TOSHIBA Field-Effect Transistor Silicon N / P Channel MOS Type

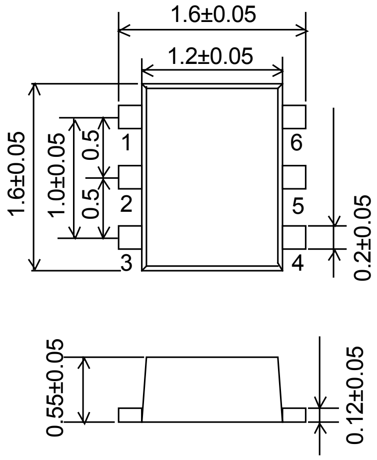
SSM6L35FE

○ High-Speed Switching Applications

○ Analog Switch Applications

- N-ch: 1.2-V drive
  P-ch: 1.2-V drive
- N-ch, P-ch, 2-in-1
- Low ON-resistance Q1 N-ch: R_{on} = 20 Ω (max) (@V_{GS} = 1.2 V)
  : R_{on} = 8 Ω (max) (@V_{GS} = 1.5 V)
  : R_{on} = 4 Ω (max) (@V_{GS} = 2.5 V)
  : R_{on} = 3 Ω (max) (@V_{GS} = 4.0 V)
  Q2 P-ch: R_{on} = 44 Ω (max) (@V_{GS} = -1.2 V)
  : R_{on} = 22 Ω (max) (@V_{GS} = -1.5 V)
  : R_{on} = 11 Ω (max) (@V_{GS} = -2.5 V)
  : R_{on} = 8 Ω (max) (@V_{GS} = -4.0 V)

Unit: mm



ES6

1.Source1 4.Source2
2.Gate1 5.Gate2
3.Drain2 6.Drain1

JEDEC	-
JEITA	-
TOSHIBA	2-2N1D

Weight: 3.0 mg (typ.)

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain–source voltage		V_{DSS}	20	V
Gate–source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	180	mA
	Pulse	I_{DP}	360	

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain–source voltage		V_{DSS}	-20	V
Gate–source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	-100	mA
	Pulse	I_{DP}	-200	

Absolute Maximum Ratings (Ta = 25 °C) (Common to the Q1, Q2)

Characteristic	Symbol	Rating	Unit
Drain power dissipation	P_D(Note 1)	150	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating
Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.135 mm^2 × 6)

Start of commercial production
2008-03

Q1 Electrical Characteristics (Ta = 25°C)

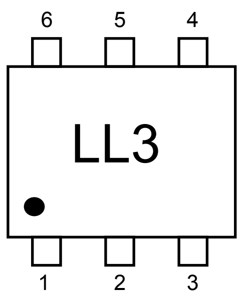
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0V	—	—	±10	μA
Drain–source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0V	20	—	—	V
Drain cutoff current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0V	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.4	—	1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 50 mA (Note 2)	115	—	—	mS
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = 50 mA, V_{GS} = 4 V (Note 2)	—	1.5	3	Ω
			I_D = 50 mA, V_{GS} = 2.5 V (Note 2)	—	2	4	
			I_D = 5 mA, V_{GS} = 1.5 V (Note 2)	—	3	8	
			I_D = 5 mA, V_{GS} = 1.2 V (Note 2)	—	5	20	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0V, f = 1 MHz	—	9.5	—	pF
Reverse transfer capacitance		C_{rss}		—	4.1	—	
Output capacitance		C_{oss}		—	9.5	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 3 V, I_D = 50 mA, V_{GS} = 0 to 2.5 V	—	115	—	ns
	Turn-off time	t_{off}		—	300	—	
Drain–source forward voltage		V_{DSF}	I_D = - 180 mA, V_{GS} = 0V (Note 2)	—	-0.9	-1.2	V

Q2 Electrical Characteristics (Ta = 25°C)

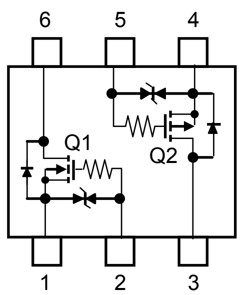
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±10	μA
Drain–source breakdown voltage		$V_{(BR)\ DSS}$	I_D = -0.1 mA, V_{GS} = 0 V	-20	—	—	V
Drain cutoff current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.4	—	-1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -50 mA (Note 2)	77	—	—	mS
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = -50 mA, V_{GS} = -4 V (Note 2)	—	4.3	8	Ω
			I_D = -50 mA, V_{GS} = -2.5 V (Note 2)	—	5.6	11	
			I_D = -5 mA, V_{GS} = -1.5 V (Note 2)	—	8.2	22	
			I_D = -2 mA, V_{GS} = -1.2 V (Note 2)	—	11	44	
Input capacitance		C_{iss}	V_{DS} = -3 V, V_{GS} = 0 V, f = 1 MHz	—	12.2	—	pF
Reverse transfer capacitance		C_{rss}		—	6.5	—	
Output capacitance		C_{oss}		—	10.4	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -3 V, I_D = -50 mA, V_{GS} = 0 to -2.5 V	—	175	—	ns
	Turn-off time	t_{off}		—	251	—	
Drain–source forward voltage		V_{DSF}	I_D = 100 mA, V_{GS} = 0 V (Note 2)	—	0.83	1.2	V

Note 2: Pulse test

Marking

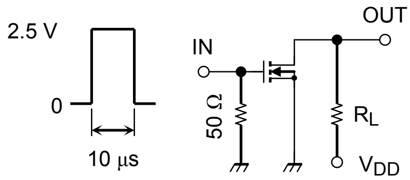


Equivalent Circuit (top view)



Q1 Switching Time Test Circuit

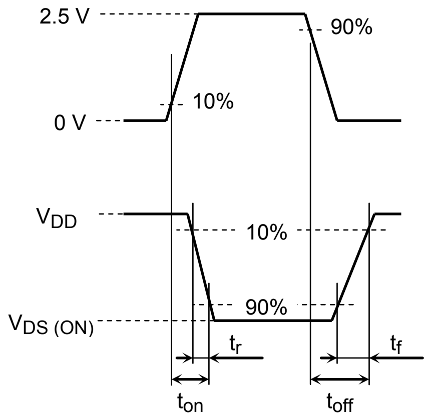
(a) Test Circuit



V_{DD} = 3 V
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

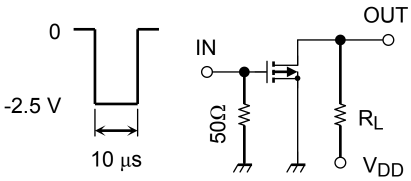
(b) V_{IN}

(c) V_{OUT}



Q2 Switching Time Test Circuit

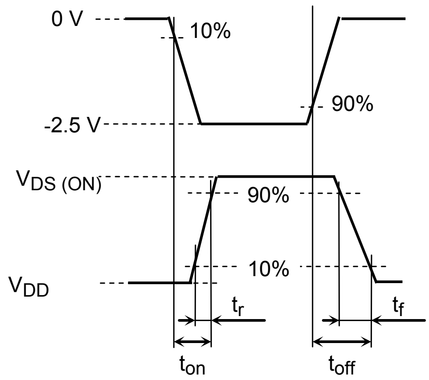
(a) Test Circuit



V_{DD} = -3 V
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Q1 Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the Q1 of the SSM6L35FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

Q2 Usage Considerations

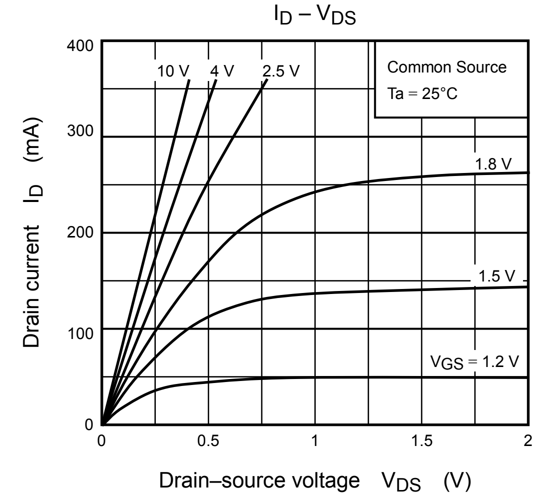
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-1 mA for the Q2 of the SSM6L35FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

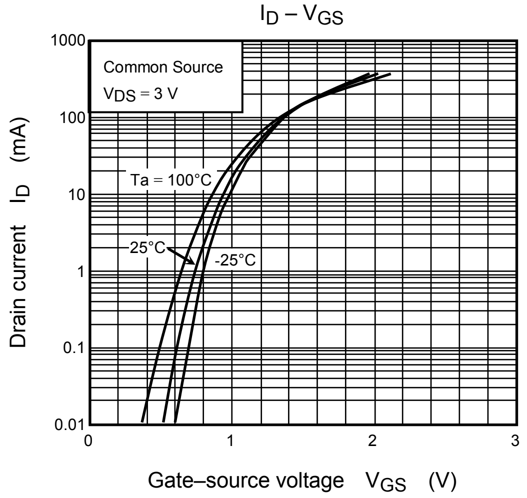
Take this into consideration when using the device.

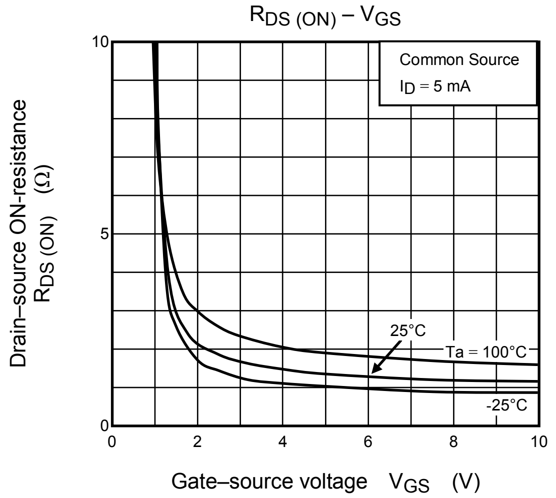
Handling Precaution

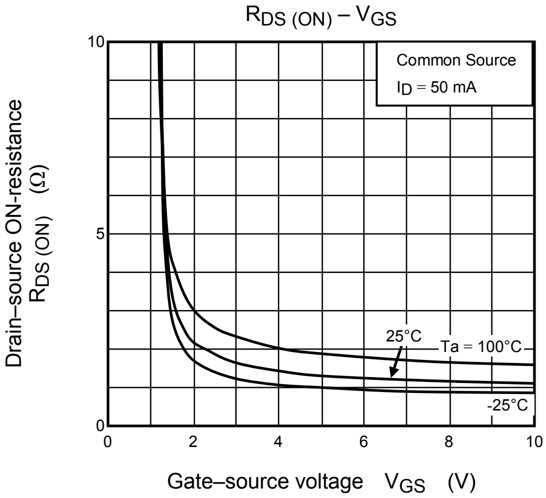
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

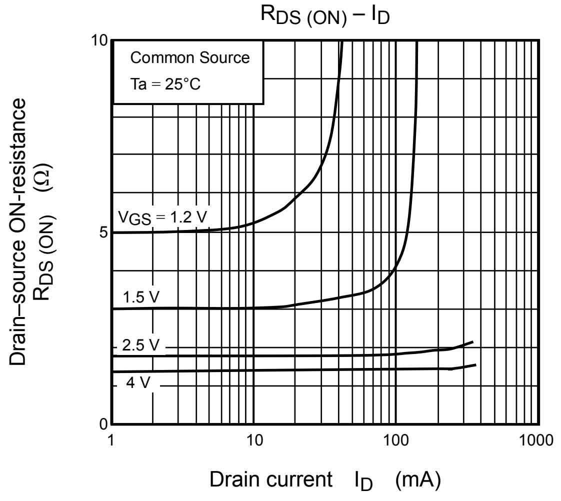
Q1 (N-ch MOSFET)

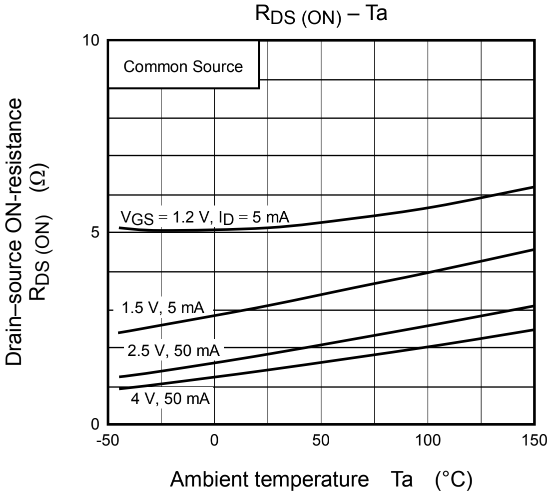




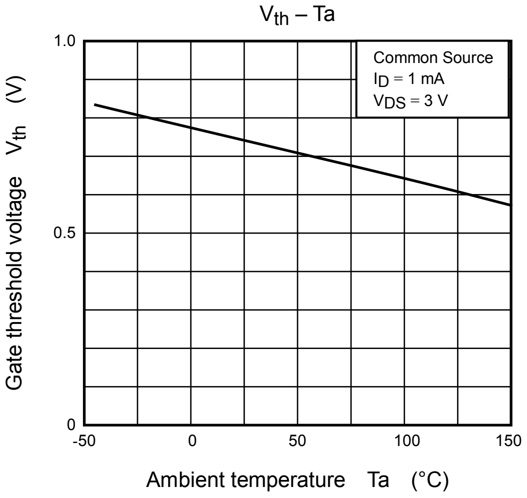


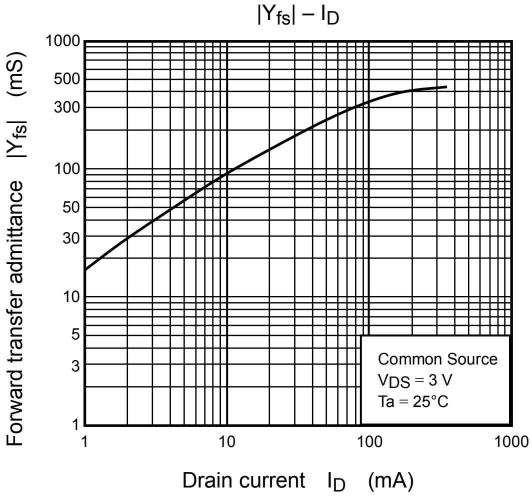


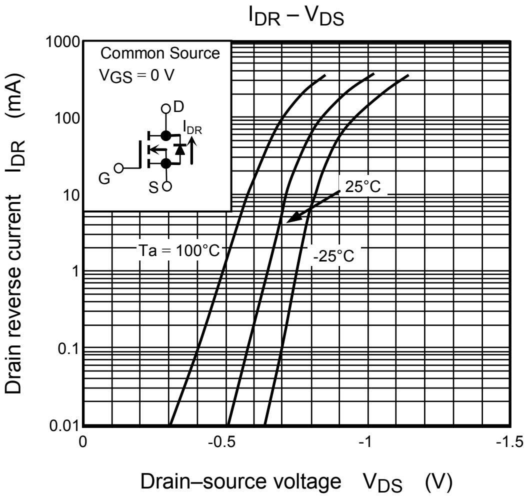


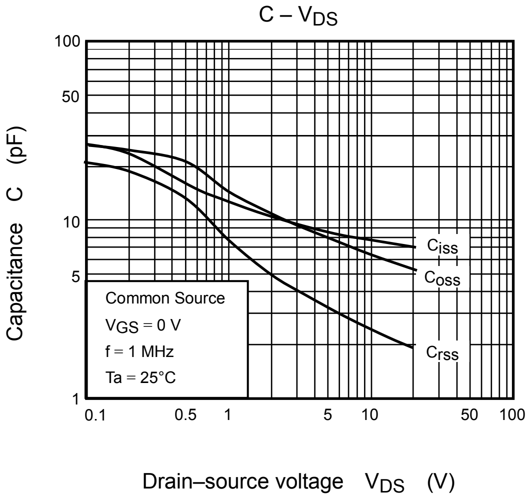


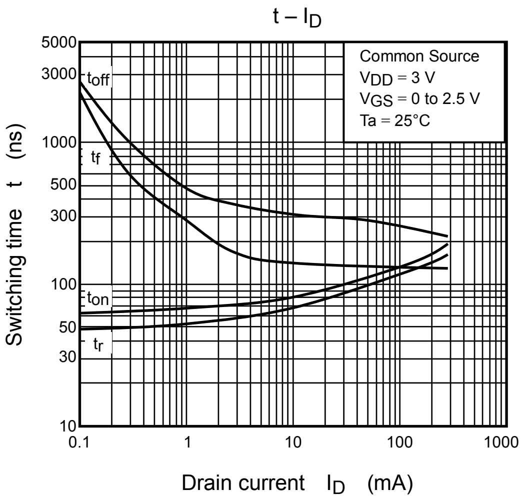
Q1 (N-ch MOSFET)



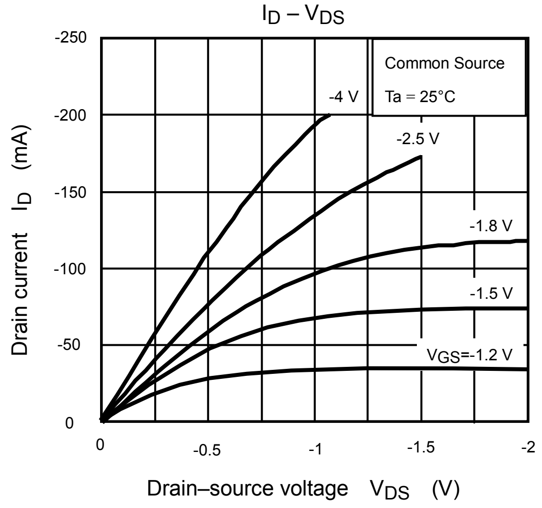


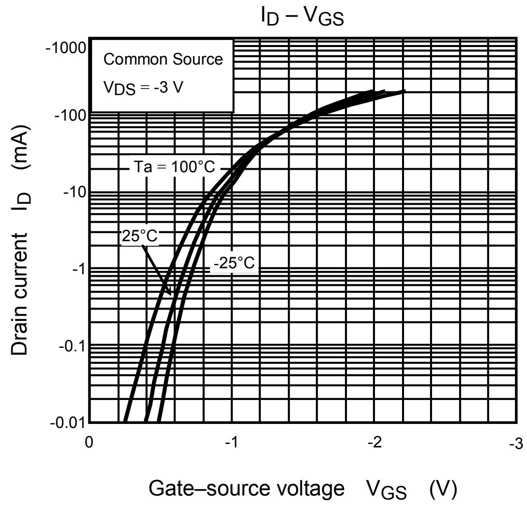


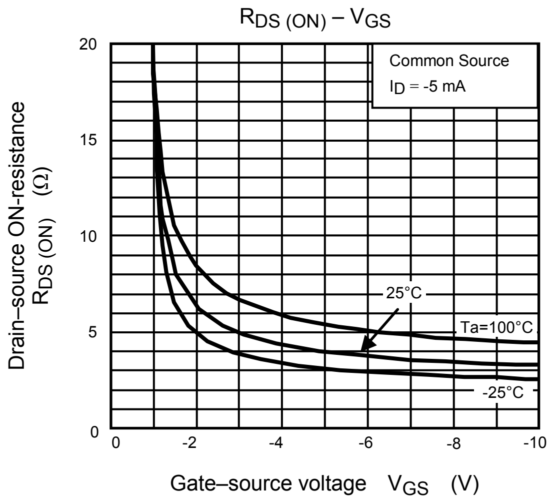


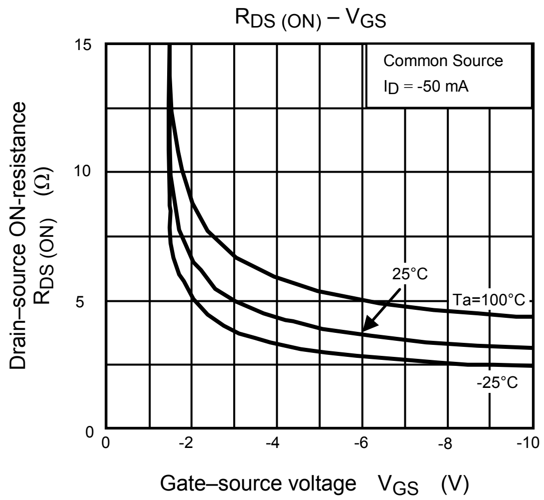


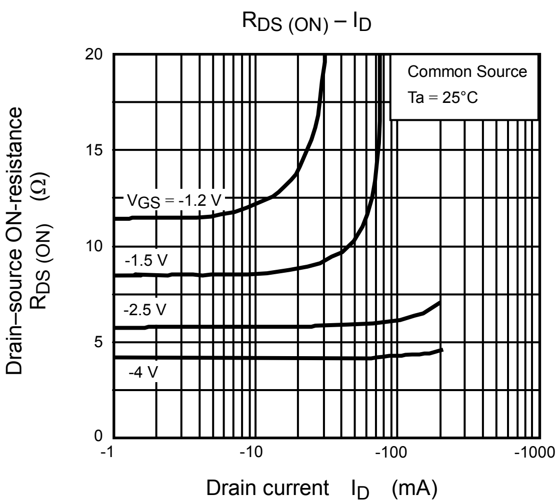
Q2 (P-ch MOSFET)

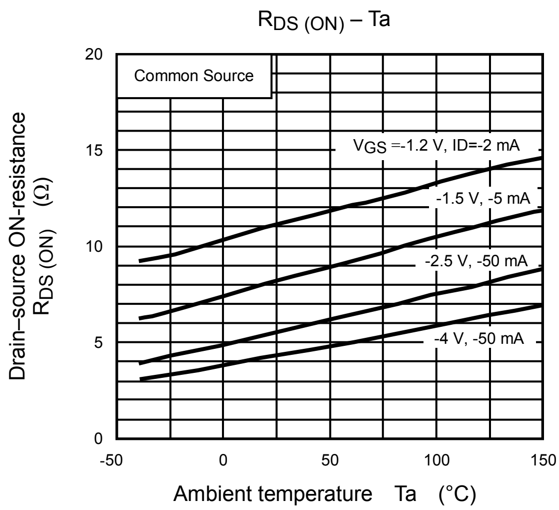




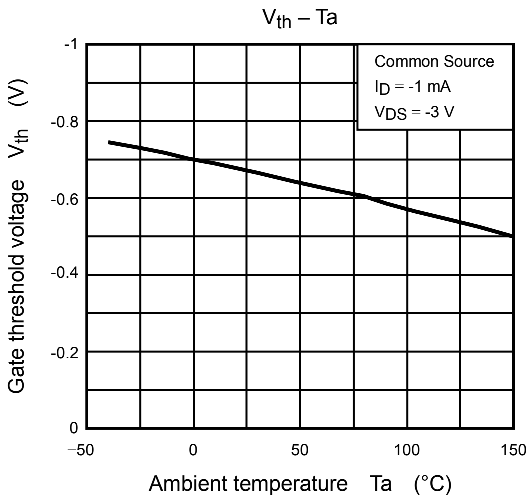


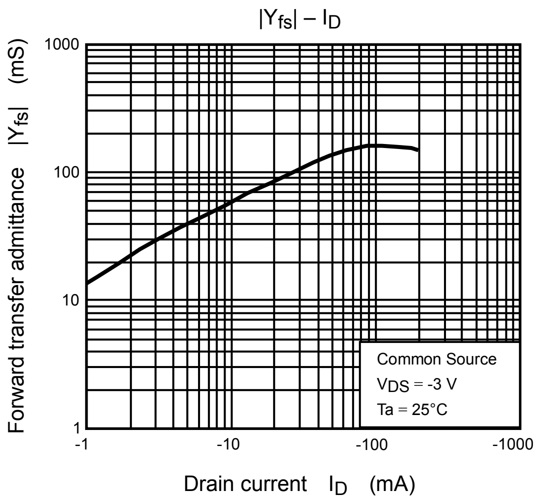


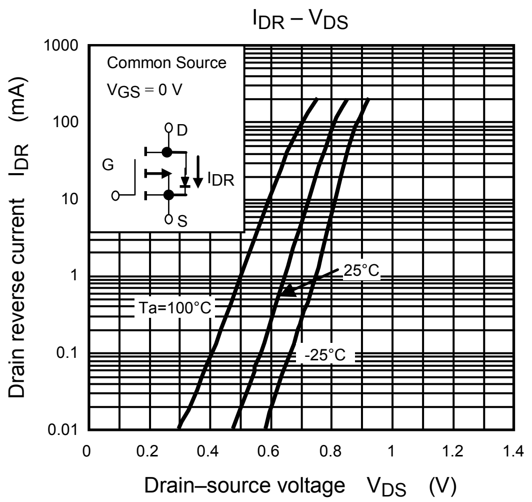


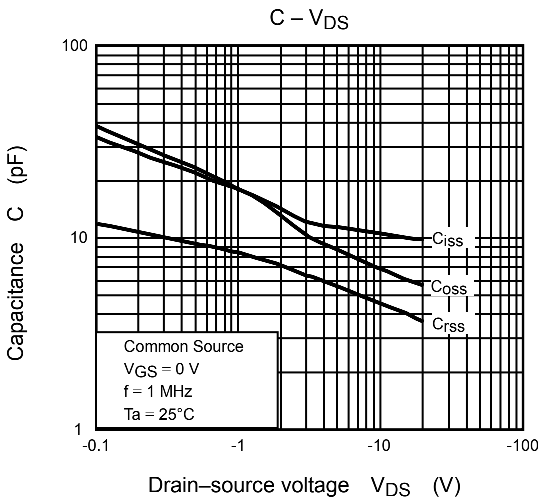


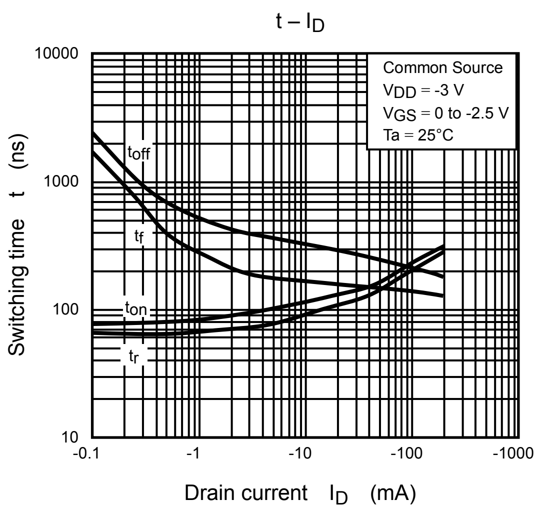
Q2 (P-ch MOSFET)

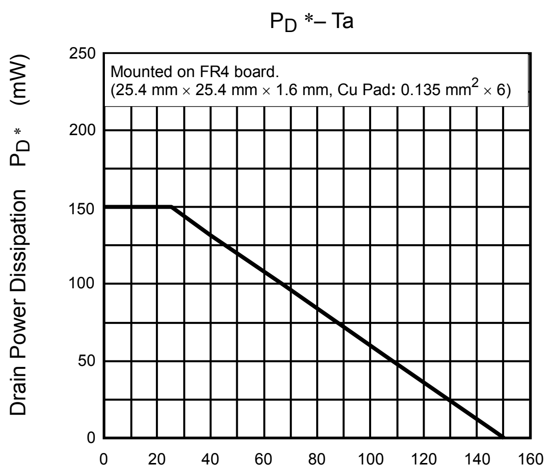












*:Total Rating

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