

# **DELKIN DEVICES®**

## **E300 Series**

### **Industrial eUSB Module**

#### **Engineering Specification**

**Document Number: 401-0451-00**

**Revision: C**

## Product Overview

- **Capacity**
  - 1GB – 32GB
- **USB Interface**
  - USB 3.1 Compliant
- **Flash Interface**
  - Flash type: SLC
- **Performance**
  - Read: up to 75 MB/s
  - Write: up to 29 MB/s
- **Power Consumption<sup>Note1</sup>**
  - Active mode: < 125mA
  - Idle mode: < 45mA
- **MTBF**
  - More than 2,000,000 hours at 0°C
- **Features**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - SMART
  - Firmware Update Capability
- **Temperature Range**
  - Operation: -40°C ~ 85°C
  - Storage: -50°C ~ +100°C
- **RoHS compliant**

### Notes:

1. Please see “5.2 Power Consumption” for details.

# TABLE OF CONTENTS

|           |  |           |
|-----------|--|-----------|
| <b>1.</b> | <b>INTRODUCTION.....</b>                   | <b>6</b>  |
| 1.1.      | General Description.....                   | 6         |
| 1.2.      | Flash Management.....                      | 6         |
| 1.2.1.    | <i>Error Correction Code (ECC)</i> .....   | 6         |
| 1.2.2.    | <i>Wear Leveling</i> .....                 | 6         |
| 1.2.3.    | <i>Bad Block Management</i> .....          | 7         |
| 1.2.4.    | <i>SMART</i> .....                         | 7         |
| 1.2.5.    | <i>Read Disturb Management</i> .....       | 7         |
| 1.2.6.    | <i>Firmware Redundancy</i> .....           | 7         |
| 1.2.7.    | <i>Dynamic Data Refresh</i> .....          | 8         |
| 1.2.8.    | <i>Power Fail Robustness</i> .....         | 8         |
| 1.2.9.    | <i>Page-based Mapping</i> .....            | 8         |
| <b>2.</b> | <b>PRODUCT SPECIFICATIONS .....</b>        | <b>9</b>  |
| 2.1.      | Overview .....                             | 9         |
| 2.2.      | Sequential and Random Performance.....     | 10        |
| 2.3.      | Part Numbers .....                         | 10        |
| 2.4.      | Connector & Configuration Options.....     | 11        |
| <b>3.</b> | <b>ENVIRONMENTAL SPECIFICATIONS.....</b>   | <b>12</b> |
| 3.1.      | Environmental Conditions.....              | 12        |
| 3.1.1.    | <i>Temperature and Humidity</i> .....      | 12        |
| 3.1.2.    | <i>Shock &amp; Vibration</i> .....         | 12        |
| 3.2.      | MTBF.....                                  | 12        |
| 3.3.      | Certification & Compliance .....           | 12        |
| <b>4.</b> | <b>ENDURANCE &amp; DATA RETENTION.....</b> | <b>13</b> |
| <b>5.</b> | <b>ELECTRICAL SPECIFICATIONS .....</b>     | <b>13</b> |
| 5.1.      | Supply Voltage .....                       | 13        |
| 5.2.      | Power Consumption .....                    | 13        |
| <b>6.</b> | <b>INTERFACE.....</b>                      | <b>14</b> |
| 6.1.      | Pin Assignment and Descriptions .....      | 14        |
| <b>7.</b> | <b>PHYSICAL ATTRIBUTES .....</b>           | <b>15</b> |

|           |   |           |
|-----------|---|-----------|
| 7.1.      | Mechanical Form Factor .....                                    | 15        |
| 7.2.      | Mechanical Dimensions.....                                      | 15        |
| <b>8.</b> | <b>ATA PASS THROUGH, IDENTIFY DEVICE &amp; SMART .....</b>      | <b>16</b> |
| 8.1.      | Supported Commands in ATA Pass Through.....                     | 16        |
| 8.2.      | ATA Identify Device Information.....                            | 16        |
| 8.3.      | ATA SMART Functionality.....                                    | 18        |
| 8.3.1.    | <i>SMART Enable Operations .....</i>                            | <i>18</i> |
| 8.3.2.    | <i>SMART Disable Operations.....</i>                            | <i>19</i> |
| 8.3.3.    | <i>SMART Read Data .....</i>                                    | <i>19</i> |
| 8.3.4.    | <i>SMART Data Structure .....</i>                               | <i>20</i> |
| 8.3.5.    | <i>Spare Block Count Attribute.....</i>                         | <i>21</i> |
| 8.3.6.    | <i>Spare Block Count Worst Chip Attribute Threshold .....</i>   | <i>21</i> |
| 8.3.7.    | <i>Erase Count Attribute .....</i>                              | <i>21</i> |
| 8.3.8.    | <i>Total ECC Errors Attribute .....</i>                         | <i>22</i> |
| 8.3.9.    | <i>Correctable ECC Errors Attribute.....</i>                    | <i>22</i> |
| 8.3.10.   | <i>Total Number of Reads Attribute.....</i>                     | <i>22</i> |
| 8.3.11.   | <i>Power On Count Attribute.....</i>                            | <i>23</i> |
| 8.3.12.   | <i>Total LBAs Written Attribute.....</i>                        | <i>23</i> |
| 8.3.13.   | <i>Total LBAs Read Attribute.....</i>                           | <i>23</i> |
| 8.3.14.   | <i>Anchor Block Status Attribute .....</i>                      | <i>23</i> |
| 8.3.15.   | <i>Trim Status Attribute .....</i>                              | <i>24</i> |
| 8.3.16.   | <i>SMART Read Attribute Threshold.....</i>                      | <i>24</i> |
| 8.3.17.   | <i>Spare Block Count Attribute Threshold.....</i>               | <i>24</i> |
| 8.3.18.   | <i>Spare Block Count Worst Channel Attribute Threshold.....</i> | <i>25</i> |
| 8.3.19.   | <i>Erase Count Attribute Threshold .....</i>                    | <i>25</i> |
| 8.3.20.   | <i>Total ECC Errors Attribute Threshold.....</i>                | <i>25</i> |
| 8.3.21.   | <i>Correctable ECC Errors Attribute Threshold.....</i>          | <i>25</i> |
| 8.3.22.   | <i>UDMA CRC Errors Attribute Threshold.....</i>                 | <i>25</i> |
| 8.3.23.   | <i>Total Number of Reads Attribute Threshold.....</i>           | <i>25</i> |
| 8.3.24.   | <i>Power On Count Attribute Threshold.....</i>                  | <i>25</i> |
| 8.3.25.   | <i>Total LBAs Written Attribute Threshold .....</i>             | <i>26</i> |
| 8.3.26.   | <i>Total LBAs Read Attribute Threshold.....</i>                 | <i>26</i> |
| 8.3.27.   | <i>Anchor Block Status Attribute Threshold .....</i>            | <i>26</i> |
| 8.3.28.   | <i>Trim Status Attribute Threshold .....</i>                    | <i>26</i> |
| 8.3.29.   | <i>SMART Return Status .....</i>                                | <i>26</i> |

## LIST OF TABLES

|  |    |
|--|----|
| Table 2-1 Performance by Capacity & Firmware Type .....  | 10 |
| Table 2-2 Part Numbers by Capacity & Firmware Type ..... | 10 |
| Table 2-3 Connector & Fixed/Removable Options .....      | 11 |
| Table 5-1 Supply Voltage .....                           | 13 |
| Table 5-2 Power Consumption .....                        | 13 |
| Table 6-1 Pin Assignment and Description for eUSB .....  | 14 |
| Table 7-1 eUSB Mechanical Form Factor Attributes .....   | 15 |

# 1.Introduction

## 1.1. General Description

Delkin's E300 Series Embedded USB (eUSB) is designed as a compact, non-removable storage module to be used as a boot device or for storage of critical data. The industrial-grade eUSB is fully compliant with USB 3.1 specifications, and is built with industrial temp SLC NAND flash.

## 1.2. Flash Management

### 1.2.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the controller in Delkin's Industrial eUSB drive applies an advanced BCH ECC algorithm, which can detect and correct errors occur during read processes, ensuring data been read correctly, as well as protecting data from corruption. The Delkin Industrial eUSB also employs "near-miss" ECC, such that all blocks which reach a certain error threshold are automatically refreshed immediately upon detection. The threshold is determined by the specific flash and ECC configuration in the card.

### 1.2.2. Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some blocks are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling techniques are applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

The controller in Delkin's newest Industrial eUSB drive utilizes an advanced Wear Leveling algorithm, which optimizes life and performance, through a combination of static and global wear leveling. Static wear leveling is utilized until one flash reaches 90% of the rated P/E cycles, which is more efficient from a performance standpoint. Once a flash reaches 90%, wear leveling switches to a global scheme, and all flash blocks participate in wear leveling as one large pool, which enables the card to maximize lifetime.

### **1.2.3. Bad Block Management**

Bad blocks are blocks that include one or more invalid bits and therefore, their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Blocks that develop invalid bits during the lifespan of the flash are named “Later Bad Blocks”. The controller in Delkin’s Industrial eUSB drive implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manage any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves data reliability.

### **1.2.4. SMART**

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. While there is not an industry standard for USB drive SMART functionality, as there is for SATA & PATA devices, the Delkin eUSB supports ATA pass through commands to collect data from the card. Refer to Section 7 for the command details and the information that can be extracted from the card.

### **1.2.5. Read Disturb Management**

Delkin’s Industrial eUSB drives have advanced Read Disturb Management to prevent uncorrectable errors in heavy read applications. As flash geometries shrink, the likelihood of disturbances when adjacent pages are frequently read is increased, and typically wear leveling is triggered by writing and erasing. However, the advanced read disturb management system actually counts all reads on a block level, and compares them to a configurable threshold. Once the threshold has been reached, a read wear level is triggered and the block is refreshed, sending it to the back of the line. This ensures that errors will not accumulate to the point that they will be uncorrectable.

### **1.2.6. Firmware Redundancy**

Since flash storage is often used in applications with unstable sources of power, protecting the firmware is critical. Delkin’s Industrial eUSB drives maintain two copies of firmware within the flash, so that if the primary copy of the firmware is damaged, the back-up copy can be used, the back-up copy is used, and then the original copy is repaired.

### **1.2.7. Dynamic Data Refresh**

Typically, when a drive is new and less than 10% of the program/erase cycles have been consumed, the data retention time of the flash is 5 or 10 years, depending on the type of flash. At end of life, however, when 100% of the program/erase cycles have been consumed, typically, the retention time is 1 year. To extend long term data retention over the life of a card, Delkin's Industrial eUSB will automatically refresh data that is not accessed for a long time, which can be triggered based on a configurable power-on count threshold and operate in the background.

### **1.2.8. Power Fail Robustness**

With the goal of preventing data corruption and card failure, Delkin's Industrial eUSB drives have been developed to survive unscheduled power interruptions with minimal effect. In the event of a power loss, the controller will reset and flash is immediately write-protected. A log is kept of recent flash transactions, and if the last data in the log is corrupt, then the controller will recover the latest valid entry. If a write operation was in process at the time of the power loss, but not committed to flash, or the tables had not yet been updated, then this data might be lost. Since the original data is always kept in a "twin" of the active block, we can always revert back to the last known valid state of the card.

### **1.2.9. Page-based Mapping**

The E300 eUSB utilizes page-based mapping, which has the advantages of improved random performance, and reduced write amplification, which improves device overall life.



## 2. Product Specifications

### 2.1. Overview

- **Capacity / Flash Type**
  - 1GB to 32GB Industrial Temperature SLC
  
- **Electrical/Physical Interface**
  - Compliant with USB 3.1 Gen 1 Specification, which includes backward compatibility to USB 2.0 and 1.1
  
- **ECC Scheme**
  - Capable of correcting up to 96 bits per 1K Byte – BCH engine
  
- **Supports SMART commands**
  
- **Supports Secure Erase and Sanitize via ATA pass through commands**
  
- **AES encryption engine 128 and 256-bit**
  
- **OS Compatibility**
  - All USB 2.0 Compatible Operating Systems supported, including:
    - Windows 7 (32 & 64bit), Windows 8, Windows 10, Windows XP
    - Linux Kernel 4.2.0-27 (Ubuntu 15.10)
    - Mac OS X 10.8.4, 10.11.2

## 2.2. Sequential and Random Performance

**Table 2-1 Performance by Capacity & Firmware Type**

| Capacity | Sequential  |              | Random      |              |
|----------|-------------|--------------|-------------|--------------|
|          | Read (MB/s) | Write (MB/s) | Read (MB/s) | Write (MB/s) |
| 1GB SLC  | TBD         | TBD          | 5.0         | 3.5          |
| 2GB SLC  | TBD         | TBD          | 5.0         | 3.5          |
| 4GB SLC  | 35          | 21           | 5.0         | 3.8          |
| 8GB SLC  | 75          | 35           | 7.0         | 3.5          |
| 16GB SLC | 75          | 35           | 5.6         | 3.8          |
| 32GB SLC | TBD         | TBD          | 5.6         | 3.8          |

Measured with CrystalDiskMark 3.0.3 64 bit in USB 3.0 mode, Random performance for 4K blocks.

## 2.3. Part Numbers

### Industrial SLC eUSB (-40 to 85°C Operating Temperature)

**Table 2-2 Part Numbers by Capacity**

| Capacity | Part Number       |
|----------|-------------------|
| 1GB      | M40GTQHFL-xx000-D |
| 2GB      | M402TQHFL-xx000-D |
| 4GB      | M404TQJGR-xx000-D |
| 8GB      | M408TQJGR-xx000-D |
| 16GB     | M416TNKGR-xx000-D |
| 32GB     | M432TNJGR-xx000-D |

#### NOTES:

1. "xx" in part number is determined by connector selection and fixed vs. removable configuration. See Section 2.4 for available options.
2. For optional Acrylic conformal coating (contact Delkin for additional cost and MOQ) to protect the devices from moisture and contaminants, replace the 000 in the part number with 050.
3. Customized parts will have a special code in place of the 000 to indicate the customer-specific features or attributes of the part.
4. Contact Delkin for information on a Security version of this product, with zone locking & encryption capabilities via an API or direct commands. NDA required.

## 2.4. Connector & Configuration Options

**Table 2-3 Connector & Fixed/Removable Options**

| Code | Pitch  | Total Height* | Orientation | Fixed / Removable                          | Connector Mfr / Part # |
|------|--------|---------------|-------------|--|------------------------|
| RA   | 0.100" | 9.77mm        | Right Angle | Removable                                  | Sullins NPPC052KFMS-RC |
| R1   | 0.100" | 5.93mm        | Right Angle | Removable                                  | Samtec HLE-105-02-G-DV |
| R2   | 2mm    | 6.97mm        | Right Angle | Removable                                  | Samtec MMS-105-02-L-DV |
| R3   | 2mm    | 4.53mm        | Right Angle | Removable                                  | Samtec CLT-105-02-G-D  |
| R4   | 0.100" | 5.93mm        | Right Angle | Fixed Disk                                 | Samtec HLE-105-02-G-DV |
| R5   | 2mm    | 6.97mm        | Right Angle | Fixed Disk                                 | Samtec MMS-105-02-L-DV |
| R6   | 2mm    | 4.53mm        | Right Angle | Fixed Disk                                 | Samtec CLT-105-02-G-D  |
| R7   | 0.100" | 9.77mm        | Right Angle | Fixed Disk                                 | Sullins NPPC052KFMS-RC |
| R8   | 0.100" | 9.77mm        | Right Angle | Removable<br>No keying plug at Pin 9       | Sullins NPPC052KFMS-RC |
| RL   | 0.100" | 5.93mm        | Right Angle | Removable<br>External LED<br>configuration | Samtec HLE-105-02-G-DV |
| ST   | 2mm    | 6.46mm        | Straight    | Removable                                  | Samtec MMS-105-02-L-DH |
| SF   | 2mm    | 6.46mm        | Straight    | Fixed Disk                                 | Samtec MMS-105-02-L-DH |

\*Total Height is referenced as Dimension X on the mechanical drawing in Section 7.2

Note: All connectors have keying plug at Pin 9, except R8 as noted.

## 3. Environmental Specifications

### 3.1. Environmental Conditions

#### 3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -50°C to +100°C
  - Operational: -40°C to +85°C
  
- Humidity:
  - RH 10 - 95% under 55°C

#### 3.1.2. Shock & Vibration

- Shock Specification
  - 12G Sawtooth pulse, 11 ms duration, 3 axes
  
- Vibration Specification
  - Sine Vibration: 10Hz ~2000Hz, 16.3 G peak to peak, 3 axes
  - Random Vibration: 10Hz ~2000Hz, 1.49 GRMS, 3 axes

### 3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Delkin's eUSB SSD is more than 2,000,000 hours for 0°C to 25°C operation.

### 3.3. Certification & Compliance

- RoHS
- USB 3.1

## 4. Endurance & Data Retention

| Attribute                      | Value  |
|--------------------------------|--|
| Raw Flash Program/Erase Rating | 60,000 cycles  |
| TBW                            | Contact Delkin for TBW and life estimate based on your specific application / workload             |
| Data Retention                 | 10 years when P/E cycles < 10% of rated cycling<br>1 year when P/E cycles at 100% of rated cycling |

## 5. Electrical Specifications

### 5.1. Supply Voltage

Table 5-1 Supply Voltage

| Parameter         | Rating   |
|-------------------|----------|
| Operating Voltage | 5V ± 10% |

### 5.2. Power Consumption

Table 5-2 Power Consumption

| Capacity | Read (max) | Write (max) | Idle (max) |
|----------|------------|-------------|------------|
| 1GB      | TBD        | TBD         | TBD        |
| 2GB      | TBD        | TBD         | TBD        |
| 4GB      | 95         | 90          | 40         |
| 8GB      | 125        | 120         | 45         |
| 16GB     | TBD        | TBD         | TBD        |
| 32GB     | TBD        | TBD         | TBD        |

Unit: mA

**NOTES:**

1. The measured input power voltage is 5V.
2. Power Consumption may vary according to flash configuration, host platform and other factors.

## 6.Interface

### 6.1. Pin Assignment and Descriptions

**Table 6-1 Pin Assignment and Description for eUSB**

| Pin Number | eUSB Pin | Description  |
|------------|----------|--|
| 1          | VCC      | 5.0V USB Bus Power Input                                 |
| 2          | SSRX+    | Superspeed Receiver                                      |
| 3          | DM       | USB 2.0 data in negative pin terminal                    |
| 4          | SSRX-    | Superspeed Receiver                                      |
| 5          | DP       | USB 2.0 data in positive pin terminal                    |
| 6          | SSTX+    | Superspeed Transmitter                                   |
| 7          | GND      | 0V regulator ground reference input                      |
| 8          | SSTX-    | Superspeed Transmitter                                   |
| 9          | NC       | Not Connected – Keying Plug (except R8 connector option) |
| 10         | Option   | Optional External LED Connection (contact Delkin)        |

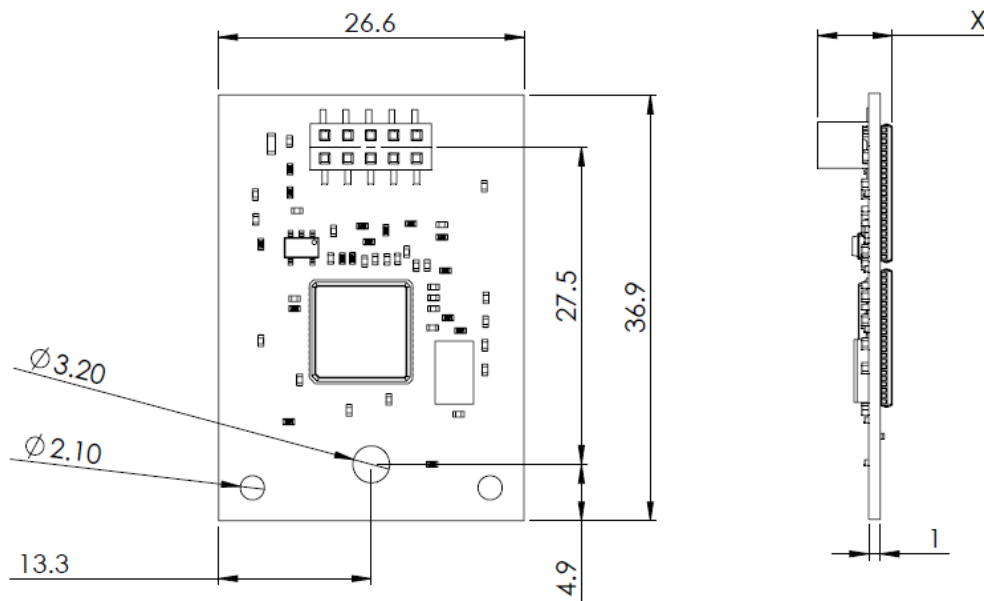
## 7. Physical Attributes

### 7.1. Mechanical Form Factor

Table 7-1 eUSB Mechanical Form Factor Attributes

| Dimension  | Value                  |
|--|------------------------|
| Length   | 36.9mm $\pm$ 0.5mm     |
| Width  | 26.6mm $\pm$ 0.5mm     |
| Thickness  | Varies with Connector  |
| Center of Mounting Hole to Centerline of Connector | 27.5mm $\pm$ 0.5mm     |
| Mass   | 10 g (0.35 oz) maximum |

### 7.2. Mechanical Dimensions



All dimensions in mm. Tolerance on all dimensions  $\pm$  0.5mm.

| Connector Code | Total Height (Dimension X) |
|----------------|----------------------------|
| RA, R7, R8     | 9.77mm                     |
| R1, R4, RL     | 5.93mm                     |
| R2, R5         | 6.97mm                     |
| R3, R6         | 4.53mm                     |
| ST, SF         | 6.46mm                     |

## 8. ATA Pass Through, IDENTIFY DEVICE & SMART

### 8.1. Supported Commands in ATA Pass Through

The following table lists the ATA commands that are supported by the eUSB firmware in the ATA Pass-Through(12) and ATA Pass-Through(16) commands.

| No. | Comand Name     | Code | FR | SC | SN | CY | DR | HD | LBA |
|-----|-----------------|------|----|----|----|----|----|----|-----|
| 1   | Identify Device | ECh  | -- | -- | -- | -- | Y  | -- | --  |
| 2   | SMART           | B0h  | Y  | -- | -- | Y  | Y  | -- | --  |

Notes: FR: Feature Register  
 SC: Sector Count register  
 SN: Sector Number register  
 CY: Cylinder Low/High register  
 DR: Drive bit of Drive/Head Register  
 HD: Head No. (0 to 15) of Drive/Head Register  
 Y: Used for the command  
 -- : Not used for the command

### 8.2. ATA Identify Device Information

The following table lists the information returned by the Identify Device ATA Passthrough command.

| Word Address | Default Value | Total Bytes | Data Field Type Information                            |
|--------------|---------------|-------------|--|
| 0            | 0040h         | 2           | General configuration bit significant information      |
| 1 - 4        | 0000h         | 8           | Reserved   |
| 5            | 0200h         | 2           | Number of unformatted bytes per sector                 |
| 6 - 9        | 0000h         | 8           | Reserved   |
| 10-19        | XXXXh         | 20          | Serial number (20 ASCII characters)                    |
| 20           | 0002h         | 2           | Buffer type (dual-ported multi-sector)                 |
| 21           | 0001h         | 2           | Buffer size in 512 byte increments                     |
| 22           | 0004h         | 2           | Number of ECC bytes passed on Read/Write Long Commands |
| 23-26        | XXXXh         | 8           | Firmware revision (8 ASCII characters)                 |
| 27-46        | XXXXh         | 40          | Model number (40 ASCII characters)                     |
| 47           | 8001h         | 2           | Maximum 1 sector on Read/Write Multiple command        |
| 48           | 0000h         | 2           | Double Word not Supported                              |
| 49           | 0F00h         | 2           | Capabilities: DMA, LBA, IORDY supported                |
| 50           | 4001h         | 2           | Capabilities: device specific standby timer minimum    |
| 51           | 0200h         | 2           | PIO data transfer cycle timing mode 2                  |
| 52           | 0000h         | 2           | DMA data transfer cycle timing mode not supported      |
| 53           | 0007h         | 2           | Data Fields 64 to 70 and 88 are valid                  |
| 54 - 58      | 0000h         | 10          | Reserved   |
| 59           | 0101h         | 2           | Multiple sector setting is valid                       |
| 60-61        | XXXXh         | 4           | Total number of sectors addressable in LBA Mode        |
| 62           | 0000h         | 2           | Single Word DMA transfer not implemented               |



| Word Address | Default Value | Total Bytes | Data Field Type Information  |
|--------------|---------------|-------------|--|
| 63           | 0007h         | 2           | Multiword DMA transfer mode, modes 0 to 2 supported  |
| 64           | 0003h         | 2           | Advanced PIO modes: modes 3 and 4 supported  |
| 65           | 0078h         | 2           | Minimum Multiword DMA cycle time.  |
| 66           | 0078h         | 2           | Recommended Multiword DMA cycle time.  |
| 67           | 0078h         | 2           | Minimum PIO transfer cycle time without flow control   |
| 68           | 0078h         | 2           | Minimum PIO transfer cycle time with flow control  |
| 69-79        | 0000h         | 22          | Reserved   |
| 80           | 01E0h         | 2           | Major version number, ATA-5 to ATA-8 support   |
| 81           | FFFFh         | 2           | Minor version number, not reported   |
| 82           | 0001h         | 2           | Command set: SMART features set  |
| 83           | 4000h         | 2           | Command set: none  |
| 84           | 4000h         | 2           | Command set/feature supported extension: none  |
| 85           | 00Xh          | 2           | Command set enabled: SMART feature set enabled/disabled  |
| 86           | 0000h         | 2           | Command set enabled: none  |
| 87           | 4000h         | 2           | Command set/feature default  |
| 88           | 043Fh         | 2           | UDMA modes 0 to 6 supported<br>Selected UDMA speed depends on USB speed:<br>SuperSpeed = UDMA6<br>HighSpeed = UDMA4<br>FullSpeed = UDMA1 |
| 89 – 118     | 0000h         | 60          | Reserved   |
| 119          | 4000h         | 2           | Command set/feature set supported extension: none  |
| 120          | 4000h         | 2           | Command set/feature set enabled extension: none  |
| 121-129      | 0000h         | 18          | Reserved   |
| 130-133      | XXXXh         | 8           | Firmware date string   |
| 134-135      | 0000h         | 4           | Reserved   |
| 136-141      | XXXXh         | 12          | Firmware file name   |
| 142-147      | XXXXh         | 12          | Preformat file name  |
| 148-153      | XXXXh         | 12          | Anchor program file name   |
| 154-155      | XXXXh         | 4           | Firmware minor revision number   |
| 156-221      | 0000h         | 132         | Reserved   |
| 222          | 1001h         | 2           | Transport major version: Serial transport  |
| 223          | FFFFh         | 2           | Transport minor version: not reported  |
| 224-254      | 0000h         | 62          | Reserved   |
| 255          | XXA5h         | 2           | Integrity Word   |

Words 60, 61, 85, 88 first byte, 130 – 135, 154, 155 and 255 are determined by the running firmware, all other words are configured in the preformat by the preformat host tool (hsfmt.)

## 8.3. ATA SMART Functionality

The ATA Pass Through module of the Delkin eUSB firmware supports the following ATA SMART commands, determined by the Feature Register value.

| Value | Command                   |
|-------|---------------------------|
| D0h   | Read Data                 |
| D1h   | Read Attribute Thresholds |
| D8h   | Enable SMART Operations   |
| D9h   | Disable SMART Operations  |
| DAh   | Return Status             |

SMART commands with Feature Register values not mentioned in the above table are not supported and will be aborted.

### 8.3.1. SMART Enable Operations

COMMAND CODE: B0h with a Feature Register value of D8h

PROTOCOL: Non-data

INPUTS:

| Register      | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|---|---|---|---|---|---|---|
| Features      | D8h |   |   |   |   |   |   |   |
| Sector Count  |     |   |   |   |   |   |   |   |
| Sector Number |     |   |   |   |   |   |   |   |
| Cylinder Low  | 4Fh |   |   |   |   |   |   |   |
| Cylinder High | C2h |   |   |   |   |   |   |   |
| Device/Head   | 1   | 1 | 1 | 0 |   |   |   |   |
| Command       | B0h |   |   |   |   |   |   |   |

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid.

DESCRIPTION: This command enables access to the SMART capabilities of the eUSB controller firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

### 8.3.2. SMART Disable Operations

COMMAND CODE: B0h with a Feature Register value of D9h

PROTOCOL: 5Ah

INPUTS:

| Register      | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|---|---|---|---|---|---|---|
| Features      | D9h |   |   |   |   |   |   |   |
| Sector Count  |     |   |   |   |   |   |   |   |
| Sector Number |     |   |   |   |   |   |   |   |
| Cylinder Low  | 4Fh |   |   |   |   |   |   |   |
| Cylinder High | C2h |   |   |   |   |   |   |   |
| Device/Head   | 1   | 1 | 1 | 0 |   |   |   |   |
| Command       | B0h |   |   |   |   |   |   |   |

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if either the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command disables access to the SMART capabilities of the eUSB controller firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

### 8.3.3. SMART Read Data

COMMAND CODE: B0h with a Feature Register value of D0h

PROTOCOL: PIO data in.

INPUTS:

| Register      | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|---|---|---|---|---|---|---|
| Features      | D0h |   |   |   |   |   |   |   |
| Sector Count  |     |   |   |   |   |   |   |   |
| Sector Number |     |   |   |   |   |   |   |   |
| Cylinder Low  | 4Fh |   |   |   |   |   |   |   |
| Cylinder High | C2h |   |   |   |   |   |   |   |
| Device/Head   | 1   | 1 | 1 | 0 |   |   |   |   |
| Command       | B0h |   |   |   |   |   |   |   |

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command returns one sector of SMART data. The data structure returned is shown in Section 3.4.

### 8.3.4. SMART Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “SMART Read Data” command (D0h.)

| Byte      | F / V | Description   |
|-----------|-------|---|
| 0 – 1     | 0010h | SMART structure version   |
| 2 – 361   |       | Attribute entries 1 to 30 (12 bytes each)                           |
| 362       | 00h   | Off-line data collection status (no off-line data collection)       |
| 363       | 00h   | Self-test execution status byte (self-test completed)               |
| 364 – 365 | 0000h | Total time in seconds to complete off-line data collection activity |
| 366       | 00h   | --  |
| 367       | 00h   | Off-line data collection capability (no off-line data collection)   |
| 368 – 369 | 0003h | SMART capability  |
| 370       | 00h   | Error logging capability (no error logging)                         |
| 371       | 00h   | --  |
| 372       | 00h   | Short self-test routine recommended polling time (in minutes)       |
| 373       | 00h   | Extended self-test routine recommended polling time (in minutes)    |
| 374 – 385 | 00h   | Reserved  |
| 386 – 387 | 0042h | SMART Structure Version   |
| 388 – 391 |       | Firmware “Commit” Counter   |
| 392 - 395 |       | Firmware Wear Level Threshold                                       |
| 396       | 01h   | Global Wear Leveling Active   |
| 397       | 01h   | Global Bad Block Management active                                  |
| 398 – 401 |       | Average Flash Block Erase Count                                     |
| 402 – 405 |       | Number of Flash Blocks involved in Wear Leveling                    |
| 406 – 409 |       | Number of total ECC errors during firmware initialization           |
| 410 – 413 |       | Number of correctable ECC errors during firmware initialization     |
| 414 - 510 | 00h   | -   |
| 511       |       | Data structure checksum   |

The attributes that are defined for the eUSB firmware return their data in the attribute section of the SMART data, using a 12 byte data field.

The field at offset 386 gives a version number for the contents of the SMART data structure. For the controller in the Delkin eUSB, only version 4 is defined.

The byte at offset 396 is fixed to 1 for page-based firmware. All chips within an interleaved channel are used for wear leveling.

The byte at offset 397 is fixed to 1 for page-based firmware. Bad block management is always done within all chips of an interleaved channel.

### 8.3.5. Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks.

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 196   | Attribute ID – Reallocation Count   |
| 1 – 2  | 0003h | Flags – Pre-fail type, attribute value is updated during normal operation   |
| 3      |       | Attribute value. The value returned here is the percentage of remaining spare blocks summed over all flash chips, i.e. $(100 \times \text{current spare blocks} / \text{initial spare blocks})$ |
| 4      |       | Attribute value (worst value)   |
| 5 – 7  |       | Sum of the initial number of spare blocks for all flash chips   |
| 8 – 10 |       | Sum of the current number of spare blocks for all flash chips   |
| 11     | 00h   | Reserved  |

This attribute is used for the SMART Return Status command. If the attribute value field is less than the spare block threshold (currently fixed at 10), the SMART Return Status command will indicate a threshold exceeded condition.

### 8.3.6. Spare Block Count Worst Chip Attribute Threshold

This attribute gives information about the amount of available spare blocks on the interleave channel that has the lowest current number of spare blocks.

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 213   | Attribute ID – Spare Block Count Worst Channel (vendor specific)  |
| 1 – 2  | 0003h | Flags – Pre-fail type, attribute value is updated during normal operation   |
| 3      |       | Attribute value. The value returned here is from all interleaved channels the worst percentage of remaining spare blocks i.e. $(100 * \text{current spare blocks} / \text{initial spare blocks})$ . |
| 4      |       | Attribute value (worst value)   |
| 5 – 7  |       | Initial number of spare blocks of the interleave channel with the lowest current number of spare blocks   |
| 8 – 10 |       | Current number of spare blocks of the interleave channel with the lowest current number of spare blocks   |
| 11     | 00h   | Reserved  |

### 8.3.7. Erase Count Attribute

This attribute gives information about the amount of flash block erases that have been performed.

| Offset | Value | Description  |
|--------|-------|--|
| 0      | 229   | Attribute ID – Erase Count Usage (vendor specific)   |
| 1 – 2  | 000Xh | Flags – Pre-fail or Advisory type, attribute value is updated during normal operation  |
| 3      |       | Attribute value. The value returned here is an estimation of the remaining card life, in percent, based on the number of flash block erases compared to the target number of erase cycles per block. |
| 4      |       | Attribute value (worst value)  |
| 5 – 10 |       | Estimated total number of block erases.  |
| 11     | 00h   | Reserved   |

This attribute is used for the SMART Return Status command. If the attribute value field is less than the erase count threshold (currently fixed at 10), the SMART Return Status command will indicate a threshold exceeded condition.

The target number of erase cycles per flash block is taken from the MaxBlockEraseCount column in the Device Description file.

### 8.3.8. Total ECC Errors Attribute

This attribute gives information about the total number of ECC errors that have occurred on flash read commands during firmware runtime. This attribute is not used for the SMART Return Status command.

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 203   | Attribute ID – Number of ECC Errors                                       |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      | 64h   | Attribute value. This value is fixed at 100.                              |
| 4      | 64h   | Attribute value (worst value)   |
| 5 – 8  |       | Total number of ECC errors (correctable and uncorrectable)                |
| 9 – 10 |       | ---   |
| 11     | 00h   | Reserved  |

### 8.3.9. Correctable ECC Errors Attribute

This attribute gives information about the total number of correctable ECC errors that have occurred on flash read commands during firmware runtime. This attribute is not used for the SMART Return Status command.

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 204   | Attribute ID – Number of corrected ECC Errors                             |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      | 64h   | Attribute value. This value is fixed at 100.                              |
| 4      | 64h   | Attribute value (worst value)   |
| 5 – 8  |       | Total number of correctable ECC errors                                    |
| 9 – 10 |       | ---   |
| 11     | 00h   | Reserved  |

### 8.3.10. Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. This can be useful for interpretation of the number of correctable or total ECC errors. This attribute is not used for the SMART Return Status command.

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 232   | Attribute ID – Number of Reads (vendor specific)                          |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      | 64h   | Attribute value. This value is fixed at 100.                              |
| 4      | 64h   | Attribute value (worst value)   |
| 5 - 10 |       | Total number of flash read commands                                       |
| 11     | 00h   | Reserved  |

### 8.3.11. Power On Count Attribute

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 12    | Attribute ID – Power On Count (vendor specific)                           |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      | 64h   | Attribute value. This value is fixed at 100.                              |
| 4      | 64h   | Attribute value (worst value)   |
| 5 - 8  |       | Number of Power On cycles   |
| 9 – 10 |       | ---   |
| 11     | 00h   | Reserved  |

### 8.3.12. Total LBAs Written Attribute

This attribute gives the total amount of data written to the disk, in units of 32MB (65536 sectors.) This number can be converted to Terabytes Written (TBW) by dividing the raw attribute value by  $2^{15}$ .

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 241   | Attribute ID – Total LBAs Written (vendor specific)                       |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      | 64h   | Attribute value. This value is fixed at 100.                              |
| 4      | 64h   | Attribute value (worst value)   |
| 5 - 10 |       | Total number of LBAs written to the disk, divided by 65536                |
| 11     | 00h   | Reserved  |

### 8.3.13. Total LBAs Read Attribute

This attribute gives the total amount of data read from the disk, in units of 32MB (65536 sectors.) This number can be converted to Terabytes read by dividing the raw attribute value by  $2^{15}$ .

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 241   | Attribute ID – Total LBAs Read (vendor specific)                          |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      | 64h   | Attribute value. This value is fixed at 100.                              |
| 4      | 64h   | Attribute value (worst value)   |
| 5 - 10 |       | Total number of LBAs read from the disk, divided by 65536                 |
| 11     | 00h   | Reserved  |

### 8.3.14. Anchor Block Status Attribute

This attribute reports how many times the Anchor block of the card has been re-written, either by the Anchor block repair routine, or by a firmware update.

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 214   | Attribute ID – Anchor Block Status (vendor specific)                      |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      | 64h   | Attribute value. This value is fixed at 100.                              |
| 4      | 64h   | Attribute value (worst value)   |
| 5 – 8  |       | Anchor Block Write Count  |
| 9 – 10 |       | ---   |
| 11     | 00h   | Reserved  |

### 8.3.15. Trim Status Attribute

This attribute gives percent ratio for the disk space that is currently in the trimmed state.

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 215   | Attribute ID – Trim Status (vendor specific)                              |
| 1 – 2  | 0002h | Flags – Advisory type, attribute value is updated during normal operation |
| 3      |       | Attribute value.  |
| 4      |       | Attribute value (worst value)   |
| 5 - 10 |       | ---   |
| 11     | 00h   | Reserved  |

### 8.3.16. SMART Read Attribute Thresholds

COMMAND CODE: B0h with a Feature Register value of D1h

PROTOCOL: PIO data in.

INPUTS:

| Register      | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|---|---|---|---|---|---|---|
| Features      | D1h |   |   |   |   |   |   |   |
| Sector Count  |     |   |   |   |   |   |   |   |
| Sector Number |     |   |   |   |   |   |   |   |
| Cylinder Low  | 4Fh |   |   |   |   |   |   |   |
| Cylinder High | C2h |   |   |   |   |   |   |   |
| Device/Head   | 1   | 1 | 1 | 0 |   |   |   |   |
| Command       | B0h |   |   |   |   |   |   |   |

NORMAL OUTPUTS: None required.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid or if SMART is not enabled.

DESCRIPTION: This command returns one sector of SMART attribute thresholds. The data structure returned is:

| Offset    | Value | Description   |
|-----------|-------|---|
| 0 - 1     | 001h  | SMART structure version                             |
| 2 – 361   |       | Attribute threshold entries 1 to 30 (12 bytes each) |
| 362 – 379 | 00h   | Reserved  |
| 380 – 510 | 00h   | ---   |
| 511       |       | Data structure checksum                             |

### 8.3.17. Spare Block Count Attribute Threshold

| Offset | Value | Description                              |
|--------|-------|--|
| 0      | 196   | Attribute ID – Reallocation Count        |
| 1      | 0Ah   | Spare Block Count Threshold, fixed at 10 |
| 2 - 11 | 00h   | Reserved                                 |



**8.3.18. Spare Block Count Worst Channel Attribute Threshold**

| Offset | Value | Description  |
|--------|-------|--|
| 0      | 213   | Attribute ID – Spare Block Count Worst Channel (vendor specific) |
| 1      | 0Ah   | Spare Block Count Worst Channel Threshold, fixed at 10           |
| 2 - 11 | 00h   | Reserved   |

**8.3.19. Erase Count Attribute Threshold**

| Offset | Value | Description  |
|--------|-------|--|
| 0      | 229   | Attribute ID – Erase Count Usage (vendor specific) |
| 1      | 0Ah   | Erase Count Threshold, fixed at 10                 |
| 2 - 11 | 00h   | Reserved   |

**8.3.20. Total ECC Errors Attribute Threshold**

| Offset | Value | Description                                     |
|--------|-------|---|
| 0      | 203   | Attribute ID – Number of ECC errors             |
| 1      | 00h   | No threshold for the Total ECC Errors Attribute |
| 2 - 11 | 00h   | Reserved  |

**8.3.21. Correctable ECC Errors Attribute Threshold**

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 204   | Attribute ID – Number of corrected ECC errors         |
| 1      | 00h   | No threshold for the Correctable ECC Errors Attribute |
| 2 - 11 | 00h   | Reserved  |

**8.3.22. UDMA CRC Errors Attribute Threshold**

| Offset | Value | Description                                    |
|--------|-------|--|
| 0      | 199   | Attribute ID –UDMA CRC error rate              |
| 1      | 00h   | No threshold for the UDMA CRC Errors Attribute |
| 2 - 11 | 00h   | Reserved                                       |

**8.3.23. Total Number of Reads Attribute Threshold**

| Offset | Value | Description  |
|--------|-------|--|
| 0      | 232   | Attribute ID – Number of Reads (vendor specific)     |
| 1      | 00h   | No threshold for the Total Number of Reads Attribute |
| 2 - 11 | 00h   | Reserved   |

**8.3.24. Power On Count Attribute Threshold**

| Offset | Value | Description                                   |
|--------|-------|---|
| 0      | 12    | Attribute ID – Power On Count                 |
| 1      | 00h   | No threshold for the Power On Count Attribute |
| 2 - 11 | 00h   | Reserved                                      |

**8.3.25. Total LBAs Written Attribute Threshold**

| Offset | Value | Description   |
|--------|-------|---|
| 0      | 241   | Attribute ID – Total LBAs Written (vendor specific) |
| 1      | 00h   | No threshold for the Total LBAs Written Attribute   |
| 2 - 11 | 00h   | Reserved  |

**8.3.26. Total LBAs Read Attribute Threshold**

| Offset | Value | Description                                      |
|--------|-------|--|
| 0      | 242   | Attribute ID – Total LBAs Read (vendor specific) |
| 1      | 00h   | No threshold for the Total LBAs Read Attribute   |
| 2 - 11 | 00h   | Reserved   |

**8.3.27. Anchor Block Status Attribute Threshold**

| Offset | Value | Description  |
|--------|-------|--|
| 0      | 214   | Attribute ID – Anchor Block Status (vendor specific) |
| 1      | 00h   | No threshold for the Anchor Block Status Attribute   |
| 2 - 11 | 00h   | Reserved   |

**8.3.28. Trim Status Attribute Threshold**

| Offset | Value | Description                                  |
|--------|-------|--|
| 0      | 215   | Attribute ID – Trim Status (vendor specific) |
| 1      | 00h   | No threshold for the Trim Status Attribute   |
| 2 - 11 | 00h   | Reserved                                     |

**8.3.29. SMART Return Status**

COMMAND CODE: B0h with a Feature Register value of DAh

PROTOCOL: Non-data

INPUTS:

| Register      | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|---|---|---|---|---|---|---|
| Features      | DAh |   |   |   |   |   |   |   |
| Sector Count  |     |   |   |   |   |   |   |   |
| Sector Number |     |   |   |   |   |   |   |   |
| Cylinder Low  | 4Fh |   |   |   |   |   |   |   |
| Cylinder High | C2h |   |   |   |   |   |   |   |
| Device/Head   | 1   | 1 | 1 | 0 |   |   |   |   |
| Command       | B0h |   |   |   |   |   |   |   |

NORMAL OUTPUTS: Returns a status indication as described below.

ERROR OUTPUTS: Aborted if the signature in the Cylinder registers is invalid or if SMART is not enabled.

**DESCRIPTION:** This command checks the device reliability status. If a threshold exceeded condition exists for either the Spare Block Count Worst Channel attribute or the Erase Count attribute, the device will set the Cylinder Low register to F4h and the Cylinder High register to 2Ch. If no threshold exceeded condition exists, the device will set the Cylinder Low register to 4Fh and the Cylinder High register to C2h.

**WARNING:** This product may contain chemicals known to the State of California to cause cancer, birth defects, or other reproductive harm. For more information go to [www.p65warnings.ca.gov](http://www.p65warnings.ca.gov).