S-85S1P Series

SUPPLY VOLTAGE DIVIDED OUTPUT, 5.5 V INPUT, 200 mA SYNCHRONOUS STEP-DOWN SWITCHING REGULATOR WITH 260 nA QUIESCENT CURRENT

www.ablic.com

Rev.1.5_01

The S-85S1P Series introduces own distinctive low power consumption control and COT (Constant On-Time) control and features ultra low current consumption and fast transient response. PWM / PFM switching control automatically switches to PFM control when under light load, and the IC operates at ultra low current consumption of 260 nA quiescent current. The S-85S1P Series realizes high efficiency in a wide range of load current consumption and provides strong support for extended period operation of mobile devices and wearable devices which are equipped with compact batteries.
The function of the supply voltage divided output is prepared in the S-85S1P Series. The supply voltage divided output is a function that divides the input voltage (V_{IN}) of the DC-DC converter into $V_{IN}/2$ or $V_{IN}/3$ and outputs the voltage. For example, this function makes it possible that the IC connects to a low voltage microcontroller A/D converter directly and the microcontroller monitors a battery voltage.

■ Features

DC-DC converter block

- Ultra low current consumption: 260 nA quiescent current
- Efficiency (when under 100 μA load): 90.5%
- Fast transient response: COT control
- Input voltage: 2.2 V to 5.5 V
- Output voltage: 0.7 V to 2.5 V, in 0.05 V step
  2.6 V to 3.9 V, in 0.1 V step
- Output voltage accuracy: ±1.5% ($1.0\text{ V} \le V_{OUT} \le 3.9\text{ V}$)
  ±15 mV ($0.7\text{ V} \le V_{OUT} < 1.0\text{ V}$)
- Switching frequency: 1.0 MHz (at PWM operation)
- High side power MOS FET on-resistance: 420 mΩ
- Low side power MOS FET on-resistance: 320 mΩ
- Soft-start function: 1 ms typ.
- Under voltage lockout function (UVLO): 1.8 V typ. (detection voltage)
- Thermal shutdown function: 135°C typ. (detection temperature)
- Overcurrent protection function: 450 mA (at L = 2.2 μH)
- Automatic recovery type short-circuit protection function: Hiccup control
- Input and output capacitors: Ceramic capacitor compatible

Supply voltage divider block

- Low current consumption: 280 nA typ.
- Input voltage: 1.5 V to 5.5 V
- Output voltage: $V_{IN}/2$ (S-85S1PCxx)
  $V_{IN}/3$ (S-85S1PDxx)

Overall

- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

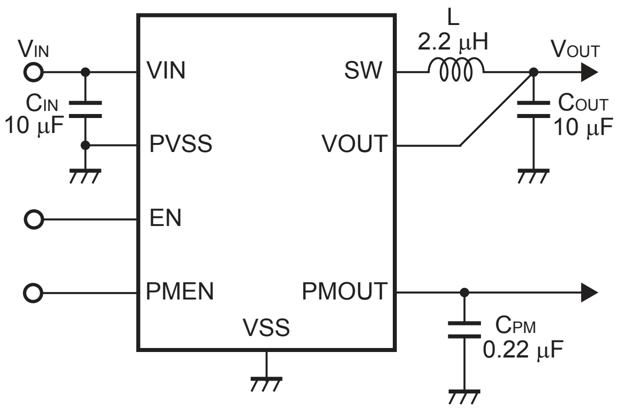
■ Applications

- Wearable device
- Bluetooth device
- Wireless sensor network device
- Healthcare equipment
- Smart meter
- Portable game device

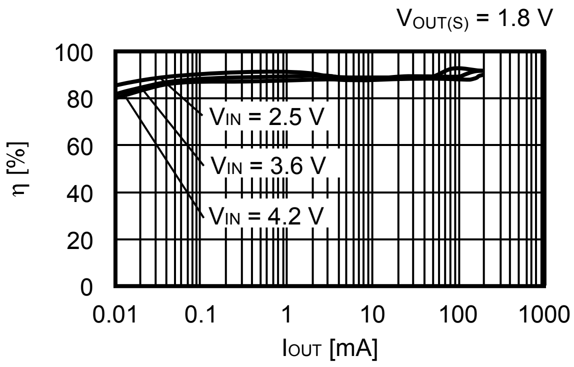
■ Package

- SNT-8A
  (2.46 mm × 1.97 mm × t0.5 mm max.)

■ Typical Application Circuit



■ Efficiency



■ Block Diagram

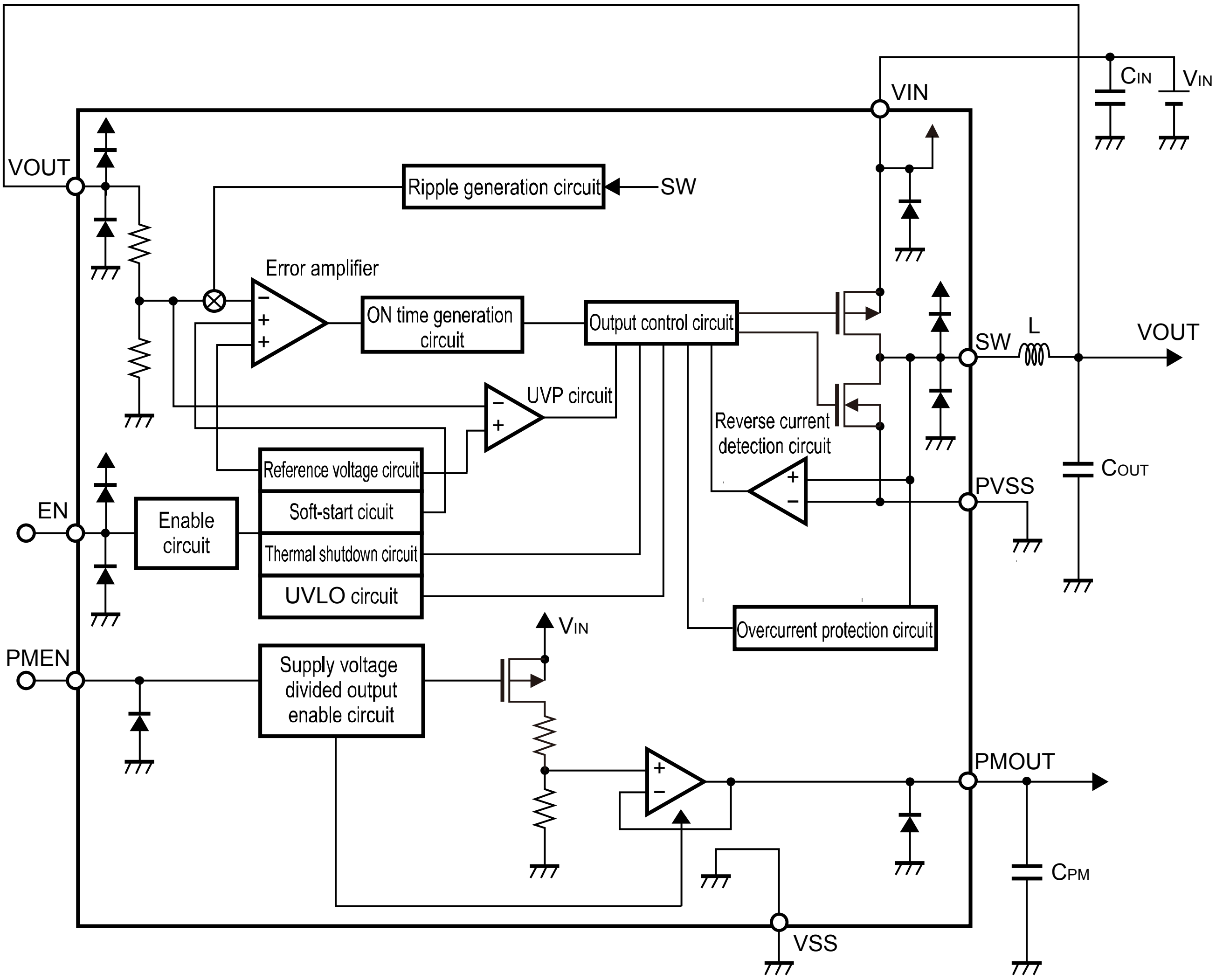

VOUT
Ripple generation circuit
SW
Error amplifier
ON time generation circuit
Output control circuit
UVP circuit
Reference voltage circuit
Soft-start cicuit
Thermal shutdown circuit
UVLO circuit
EN
Enable circuit
PMEN
Supply voltage divided output enable circuit
VIN
CIN
VIN
SW
L
VOUT
Reverse current detection circuit
PVSS
COUT
Overcurrent protection circuit
VIN
PMOUT
CPM
VSS

Figure 1

■ Product Name Structure

Users can select supply voltage divider block output voltage and DC-DC converter block output voltage for the S-85S1P Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Package**" regarding the package, "**3. Product name list**" regarding details of the product name.

1. Product name

S-85S1P x xx - I8T1 U

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package name abbreviation and packing specification[*1]
I8T1: SNT-8A, Tape

DC-DC converter block output voltage[*2, *3]
07 to 39
(e.g., when the output voltage is 0.7 V, it is expressed as 07.)

Supply voltage divider block output voltage
C: $V_{IN}/2$
D: $V_{IN}/3$

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".
***3.** In the range from 0.7 V to 2.5 V, the products which have 0.05 V step are also available.
Contact our sales office when the product is necessary.

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

Table 2

Output Voltage (V_{OUT})	S-85S1PCxx	S-85S1PDxx
0.7 V ± 15 mV	S-85S1PC07-I8T1U	S-85S1PD07-I8T1U
0.8 V ± 15 mV	S-85S1PC08-I8T1U	S-85S1PD08-I8T1U
0.9 V ± 15 mV	S-85S1PC09-I8T1U	S-85S1PD09-I8T1U
1.0 V ± 1.5%	S-85S1PC10-I8T1U	S-85S1PD10-I8T1U
1.1 V ± 1.5%	S-85S1PC11-I8T1U	S-85S1PD11-I8T1U
1.2 V ± 1.5%	S-85S1PC12-I8T1U	S-85S1PD12-I8T1U
1.3 V ± 1.5%	S-85S1PC13-I8T1U	S-85S1PD13-I8T1U
1.4 V ± 1.5%	S-85S1PC14-I8T1U	S-85S1PD14-I8T1U
1.5 V ± 1.5%	S-85S1PC15-I8T1U	S-85S1PD15-I8T1U
1.6 V ± 1.5%	S-85S1PC16-I8T1U	S-85S1PD16-I8T1U
1.7 V ± 1.5%	S-85S1PC17-I8T1U	S-85S1PD17-I8T1U
1.8 V ± 1.5%	S-85S1PC18-I8T1U	S-85S1PD18-I8T1U
1.9 V ± 1.5%	S-85S1PC19-I8T1U	S-85S1PD19-I8T1U
2.0 V ± 1.5%	S-85S1PC20-I8T1U	S-85S1PD20-I8T1U
2.1 V ± 1.5%	S-85S1PC21-I8T1U	S-85S1PD21-I8T1U
2.2 V ± 1.5%	S-85S1PC22-I8T1U	S-85S1PD22-I8T1U
2.3 V ± 1.5%	S-85S1PC23-I8T1U	S-85S1PD23-I8T1U
2.4 V ± 1.5%	S-85S1PC24-I8T1U	S-85S1PD24-I8T1U
2.5 V ± 1.5%	S-85S1PC25-I8T1U	S-85S1PD25-I8T1U
2.6 V ± 1.5%	S-85S1PC26-I8T1U	S-85S1PD26-I8T1U
2.7 V ± 1.5%	S-85S1PC27-I8T1U	S-85S1PD27-I8T1U
2.8 V ± 1.5%	S-85S1PC28-I8T1U	S-85S1PD28-I8T1U
2.9 V ± 1.5%	S-85S1PC29-I8T1U	S-85S1PD29-I8T1U
3.0 V ± 1.5%	S-85S1PC30-I8T1U	S-85S1PD30-I8T1U
3.1 V ± 1.5%	S-85S1PC31-I8T1U	S-85S1PD31-I8T1U
3.2 V ± 1.5%	S-85S1PC32-I8T1U	S-85S1PD32-I8T1U
3.3 V ± 1.5%	S-85S1PC33-I8T1U	S-85S1PD33-I8T1U
3.4 V ± 1.5%	S-85S1PC34-I8T1U	S-85S1PD34-I8T1U
3.5 V ± 1.5%	S-85S1PC35-I8T1U	S-85S1PD35-I8T1U
3.6 V ± 1.5%	S-85S1PC36-I8T1U	S-85S1PD36-I8T1U
3.7 V ± 1.5%	S-85S1PC37-I8T1U	S-85S1PD37-I8T1U
3.8 V ± 1.5%	S-85S1PC38-I8T1U	S-85S1PD38-I8T1U
3.9 V ± 1.5%	S-85S1PC39-I8T1U	S-85S1PD39-I8T1U

Remark Please contact our sales office for products with specifications other than the above.

■ Pin Configuration

1. SNT-8A

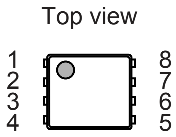


Figure 2

Table 3

Pin No.	Symbol	Description
1	PMOUT	Supply voltage divided output pin
2	VOUT	Voltage output pin
3	VSS	GND pin
4	SW	External inductor connection pin
5	PVSS	Power GND pin
6	VIN	Power supply pin
7	EN	Enable pin "H" : Enable (normal operation) "L" : Disable (standby)
8	PMEN	Supply voltage divided output enable pin "H" : Enable (normal operation) "L" : Disable (standby)

■ Absolute Maximum Ratings

Table 4

(Unless otherwise specified: Ta = +25°C, V_{SS} = 0 V)

Item		Symbol	Absolute Maximum Rating	Unit
VIN pin voltage		V_{IN}	$V_{SS} - 0.3$ to $V_{SS} + 6.0$	V
EN pin voltage	DC-DC converter block	V_{EN}	$V_{SS} - 0.3$ to $V_{IN} + 0.3 \leq V_{SS} + 6.0$	V
PMEN pin voltage	Supply voltage divider block	V_{PMEN}	$V_{SS} - 0.3$ to $V_{SS} + 6.0$	V
VOUT pin voltage	DC-DC converter block	V_{OUT}	$V_{SS} - 0.3$ to $V_{IN} + 0.3 \leq V_{SS} + 6.0$	V
PMOUT pin voltage	Supply voltage divider block	V_{PMOUT}	$V_{SS} - 0.3$ to $V_{IN} + 0.3 \leq V_{SS} + 6.0$	V
SW pin voltage		V_{SW}	$V_{SS} - 0.3$ to $V_{IN} + 0.3 \leq V_{SS} + 6.0$	V
PVSS pin voltage		V_{PVSS}	$V_{SS} - 0.3$ to $V_{SS} + 0.3 \leq V_{SS} + 6.0$	V
Operation temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance[*1]	θ_{JA}	SNT-8A	Board A	−	211	−	°C/W
			Board B	−	173	−	°C/W
			Board C	−	−	−	°C/W
			Board D	−	−	−	°C/W
			Board E	−	−	−	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. DC-DC converter block

Table 6

(V_{IN} = 3.6 V[*1], Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating input voltage	V_{IN}	−	2.2	3.6	5.5	V
Output voltage[*2]	V_{OUT}	1.0 V ≤ V_{OUT} ≤ 3.9 V, no external parts	$V_{OUT(S)} \times 0.985$	$V_{OUT(S)}$	$V_{OUT(S)} \times 1.015$	V
		0.7 V ≤ V_{OUT} <1.0 V, no external parts	$V_{OUT(S)} - 0.015$	$V_{OUT(S)}$	$V_{OUT(S)} + 0.015$	V
Current consumption during shutdown	I_{SSS}	V_{EN} = 0 V	−	1	100	nA
Current consumption during switching off	I_{SS1}	$V_{OUT} = V_{OUT(S)} + 0.1$ V, $V_{EN} = V_{IN}$, no external parts, no switching operation	−	260	500	nA
High level input voltage	V_{SH}	V_{IN} = 2.2 V to 5.5 V, EN pin	1.1	−	−	V
Low level input voltage	V_{SL}	V_{IN} = 2.2 V to 5.5 V, EN pin	−	−	0.3	V
High level input current	I_{SH}	V_{IN} = 2.2 V to 5.5 V, EN pin, $V_{EN} = V_{IN}$	−100	−	100	nA
Low level input current	I_{SL}	V_{IN} = 2.2 V to 5.5 V, EN pin, V_{EN} = 0 V	−100	−	100	nA
High side power MOS FET on-resistance	R_{HFET}	I_{SW} = 100 mA	−	420	−	mΩ
Low side power MOS FET on-resistance	R_{LFET}	I_{SW} = −100 mA	−	320	−	mΩ
High side power MOS FET leakage current	I_{HSW}	V_{IN} = 2.2 V to 5.5 V, V_{EN} = 0 V, V_{SW} = 0 V	−	1	100	nA
Low side power MOS FET leakage current	I_{LSW}	V_{IN} = 2.2 V to 5.5V, V_{EN} = 0 V, $V_{SW} = V_{IN}$	−100	1	−	nA
Current limit[*3]	I_{LIM}	L = 2.2 μH	−	450	−	mA
ON time[*4]	t_{ON}	$t_{ON(S)} = 1/f_{SW}$[*5] $\times V_{OUT}/V_{IN}$, $V_{OUT} = V_{OUT(S)} \times 0.9$	$t_{ON(S)}/1.3$	$t_{ON(S)}$	$t_{ON(S)}/0.7$	ns
Minimum OFF time	$t_{OFF(MIN)}$	−	−	100	−	ns
UVLO detection voltage	V_{UVLO-}	When V_{IN} falls	1.7	1.8	1.9	V
UVLO release voltage	V_{UVLO+}	When V_{IN} rises	1.9	2.0	2.1	V
UVP detection voltage	V_{UVP}	−	−	$V_{OUT(S)} \times 0.7$	−	V
Soft-start wait time	t_{SSW}	Time until V_{OUT} starts rising	−	1.5	−	ms
Soft-start time	t_{SS}	Time until V_{OUT} reaches 90% after it starts rising	−	1.0	−	ms
Thermal shutdown detection temperature	T_{SD}	Junction temperature	−	135	−	°C
Thermal shutdown release temperature	T_{SR}	Junction temperature	−	115	−	°C

***1.** $V_{IN} = V_{OUT(S)} + 1.0$ V ($V_{OUT(S)} \geq 2.6$ V)

***2.** V_{OUT}: Actual output voltage
$V_{OUT(S)}$: Set output voltage

***3.** The current limit changes according to the L value for the inductor to be used, input voltage, and output voltage.
Refer to "■ **Operation**" for details.

***4.** t_{ON}: Actual ON time
$t_{ON(S)}$: Set ON time

***5.** f_{SW}: Switching frequency (1 MHz)

2. Supply voltage divider block

Table 7

(V_{IN} = 3.6 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating input voltage	V_{IN}	–		1.5	3.6	5.5	V
Output voltage[*1]	$V_{PMOUT(S)}$	$-10\ \mu A \leq I_{PMOUT} \leq 10\ \mu A$	S-85S1PCxx	–	$V_{IN}/2$	–	V
			S-85S1PDxx	–	$V_{IN}/3$	–	V
Load current	I_{PMOUT}	–		–10	–	10	μA
Output offset voltage	V_{POF}	$-10\ \mu A \leq I_{PMOUT} \leq 10\ \mu A$	S-85S1PCxx	–30	–	30	mV
			S-85S1PDxx	–20	–	20	mV
Output impedance	R_{PS}	$-10\ \mu A \leq I_{PMOUT} \leq 10\ \mu A$		–	–	1000	Ω
Set-up time	t_{PU}	C_{PM} = 0.22 μF, no load	S-85S1PCxx	–	2.2	10	ms
			S-85S1PDxx	–	1.1	10	ms
Current consumption during operation[*2]	I_{SS1P}	$V_{PMEN} = V_{IN}$, no load (V_{EN} = 0 V)		–	280	550	nA
PMEN pin input voltage "H"	V_{PSH}	V_{IN} = 3.6 V, Determined by V_{PMOUT} output level		1.0	–	–	V
PMEN pin input voltage "L"	V_{PSL}	Determined by V_{PMOUT} output level		–	–	0.25	V
PMEN pin input current "H"	I_{PSH}	$V_{PMEN} = V_{IN}$		–100	–	100	nA
PMEN pin input current "L"	I_{PSL}	V_{PMEN} = 0 V		–100	–	100	nA
Discharge shunt resistance during power-off	R_{PLOW}	V_{PMEN} = 0 V, V_{PMOUT} = 0.1 V		–	2.8	–	kΩ

***1.** $V_{PMOUT(S)}$: Set output voltage
$V_{PMOUT(S)} + V_{POF}$: Actual output voltage

***2.** Current consumption when only the supply voltage divider block is in operation.

■ Operation

1. DC-DC converter block

1. 1 Fast transient response

Distinctive COT (Constant On-Time) control is used for DC-DC converter control.
The S-85S1P Series monitors the output voltage (V_{OUT}) using a comparator and if V_{OUT} falls below the targeted value, the high side power MOS FET will turn on for a certain amount of time. Since the high side power MOS FET turns on and V_{OUT} rises immediately after the load current fluctuates rapidly and V_{OUT} falls, the fast transient response is realized.

The S-85S1P Series outputs ON time in proportion to V_{OUT} and in inverse proportion to power supply voltage. Therefore, when in continuous mode, even if the power supply voltage or V_{OUT} settings would change, it always operates at a quasi-fixed frequency of 1 MHz.

1. 2 PWM / PFM switching control

The S-85S1P Series automatically switches between the pulse width modulation method (PWM) and pulse frequency modulation method (PFM) according to the load current. If the output current (I_{OUT}) is large, the IC will operate at PWM control. If I_{OUT} is small, the IC will operate at PFM control and skip the pulse according to the load current. This reduces switching loss and improves efficiency when under light load.
The S-85S1P Series has a built-in reverse current detection circuit. The reverse current detection circuit monitors the current flowing through the inductor. If the bottom of ripple current in the inductor falls to 0 mA, the high side power MOS FET and low side power MOS FET will turn off and switching operation will stop. Switching frequency will fall from 1.0 MHz by skipping a pulse. This means that the smaller I_{OUT} is, the more the switching frequency (f_{SW}) will drop, and it reduces switching loss.

1. 3 Ultra low current consumption

When in discontinuous mode, the S-85S1P Series reduces current consumption to 260 nA typ. by intermittently operating a control circuit and a protection circuit. When under light load, the high side power MOS FET and low side power MOS FET will turn off. When switching operation stops and a certain amount of time elapses, only the necessary circuits will operate.
Under voltage lockout function (UVLO), thermal shutdown function, current limit function, and automatic recovery type short-circuit protection function are prepared in the S-85S1P Series, and each protection function will carry out detection operation for a certain amount of time from when the high side power MOS FET turns on under light load. It is thus able to realize ultra low current consumption. When under heavy load, the IC changes to continuous mode as a result of the fact that the high side power MOS FET and low side power MOS FET turn on continuously, so all the IC, including the protection circuits, will operate.

1. 4 EN pin

This pin starts and stops switching operation. When the EN pin is set to "L", the operation of all internal circuits, including the high side power MOS FET, is stopped, reducing current consumption. Current consumption increases when a voltage of 0.3 V to V_{IN} − 0.3 V is applied to the EN pin. When not using the EN pin, connect it to the VIN pin. Since the EN pin is neither pulled down nor pulled up internally, do not use it in the floating status. The structure of the EN pin is shown in **Figure 3**.

Table 8

EN Pin	Internal Circuit	VOUT Pin Voltage
"H"	Enable (normal operation)	V_{OUT}[*1]
"L"	Disable (standby)	"High-Z"

***1.** Refer to ***2** in **Table 6** in "**■ Electrical Characteristics**".

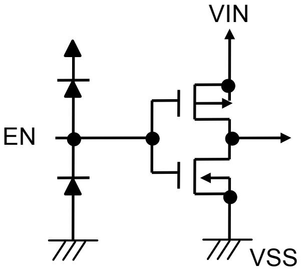


Figure 3

1. 5 Under voltage lockout function (UVLO)

The S-85S1P Series has a built-in UVLO circuit to prevent the IC from malfunctioning due to a transient status at power-on or a momentary drop in the supply voltage. When UVLO status is detected, the high side power MOS FET and low side power MOS FET will turn off, and the SW pin will change to "High-Z". For this reason, switching operation will stop. The soft-start function is reset if UVLO status is detected once, and is restarted by releasing the UVLO status.
Note that the other internal circuits operate normally and the status is different from the disabled status.
Also, there is a hysteresis width for avoiding malfunctions due to generation of noise etc. in the input voltage.

1. 6 Thermal shutdown function

The S-85S1P Series has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 135°C typ., the thermal shutdown circuit becomes the detection status, and the switching operation is stopped. When the junction temperature decreases to 115°C typ., the thermal shutdown circuit becomes the release status, and the switching operation is restarted.
If the thermal shutdown circuit becomes the detection status due to self-heating, the switching operation is stopped and output voltage (V_{OUT}) decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the switching operation is restarted, thus the self-heating is generated again. Repeating this procedure makes the waveform of V_{OUT} into a pulse-like form. Switching operation stopping and starting can be stopped by either setting the EN pin to "L", lowering the output current (I_{OUT}) to reduce internal power consumption, or decreasing the ambient temperature.

Table 9

Thermal Shutdown Circuit	VOUT Pin Voltage
Release: 115°C typ.*1	V_{OUT}
Detection: 135°C typ.*1	"High-Z"

***1.** Junction temperature

1. 7 Overcurrent protection function

The S-85S1P Series has a built-in current limit circuit.
The overcurrent protection circuit monitors the current that flows through the low side power MOS FET and limits current to prevent thermal destruction of the IC due to an overload, magnetic saturation in the inductor, etc.

When a current exceeding the current limit (I_{LIM}) flows through the low side power MOS FET, the current limit circuit operates and prohibits turning on the high side power MOS FET until the current falls below the low side current limit (I_{LIMDET}). If the value of the current that flows through the low side power MOS FET falls to the I_{LIMDET} or lower, the S-85S1P Series returns to normal operation. I_{LIMDET} is fixed at 270 mA typ. in the IC, and I_{LIM} will vary depending on the external parts to be used.
The relation between I_{LIM}, the inductor value (L), the input voltage (V_{IN}), and the output voltage (V_{OUT}) are shown in the following expression.

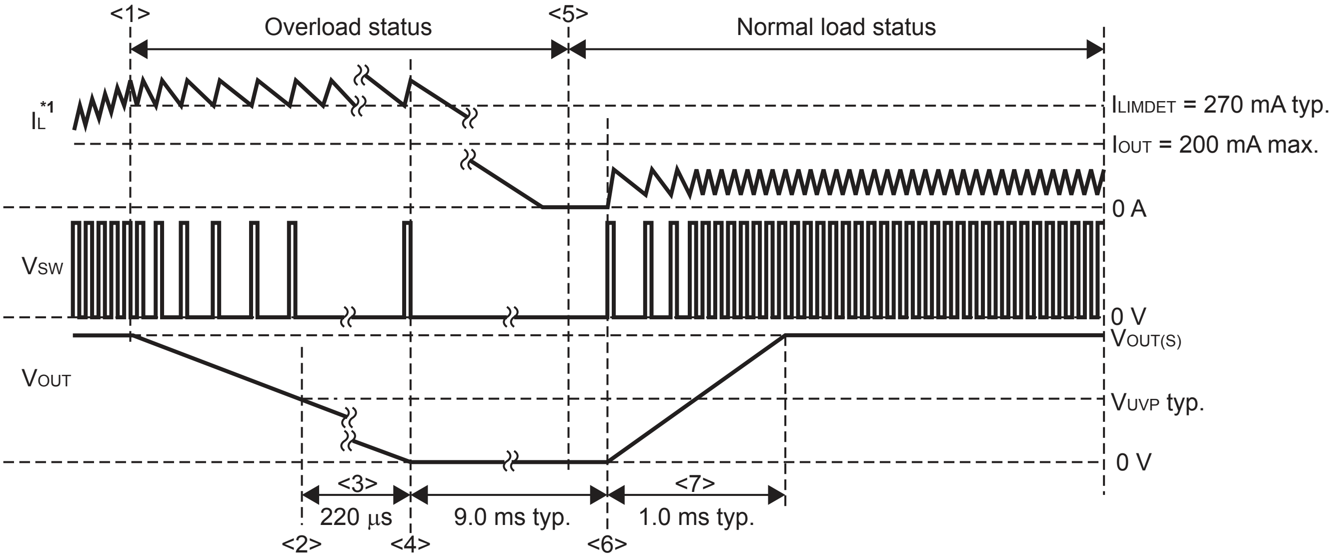
$$I_{LIM} = I_{LIMDET} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

1. 8 Automatic recovery type short-circuit protection function (Hiccup control)

The S-85S1P Series has a built-in automatic recovery type short-circuit protection function for Hiccup control. Hiccup control is a method for periodically carrying out automatic recovery when the IC detects overcurrent and stops the switching operation.

1. 8. 1 When over load status is released

<1> Overcurrent detection
<2> Under voltage protection circuit (UVP circuit) detects a drop in the output voltage (V_{OUT}).
<3> 220 μs elapse
<4> Switching operation stop (for 9 ms typ.)
<5> Overload status release
<6> The IC restarts, soft-start function starts.
In this case, it is unnecessary to input an external reset signal for restart.
<7> V_{OUT} reaches $V_{OUT(S)}$ after 1.0 ms typ. elapses.

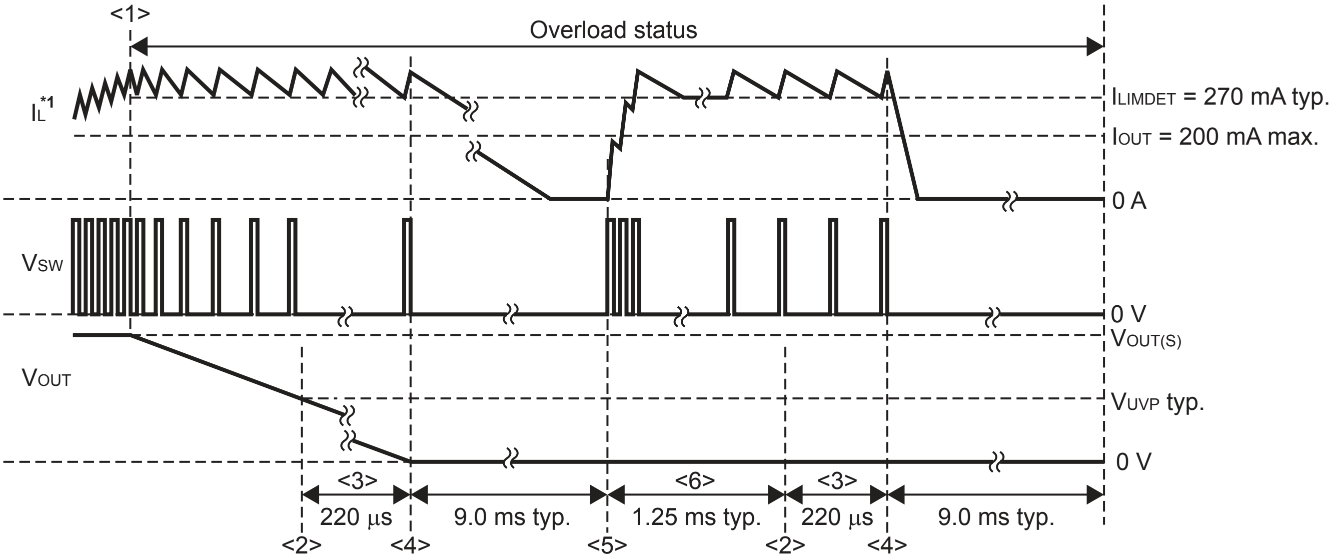

<1>
Overload status
<5>
Normal load status
IL*1
ILIMDET = 270 mA typ.
IOUT = 200 mA max.
0 A
VSW
0 V
VOUT(S)
VOUT
VUVP typ.
0 V
<3>
220 μs
9.0 ms typ.
<7>
1.0 ms typ.
<2>
<4>
<6>

*1. Inductor current

Figure 4

1. 8. 2 When over load status continues

<1> Overcurrent detection
<2> The UVP circuit detects a drop in V_{OUT}.
<3> 220 μs elapse
<4> Switching operation stop (for 9 ms typ.)
<5> The IC restarts, soft-start function starts.
<6> The status returns to <2> when over load status continues after 1.25 ms typ. elapses.


<1>
Overload status
IL*1
ILIMDET = 270 mA typ.
IOUT = 200 mA max.
0 A
VSW
0 V
VOUT(S)
VOUT
VUVP typ.
0 V
<3>
220 μs
9.0 ms typ.
<6>
1.25 ms typ.
<3>
220 μs
9.0 ms typ.
<2>
<4>
<5>
<2>
<4>

*1. Inductor current

Figure 5

1. 9 Pre-bias compatible soft-start function

The S-85S1P Series has a built-in pre-bias compatible soft-start circuit.
If the pre-bias compatible soft-start circuit starts when electrical charge remains in the output voltage (V_{OUT}) as a result of power supply restart, etc., or when V_{OUT} is biased beforehand (pre-bias status), switching operation is stopped until the soft-start voltage exceeds the internal feedback voltage, and then V_{OUT} is maintained. If the soft-start voltage exceeds the internal feedback voltage, switching operation will restart and V_{OUT} will rise to the output voltage setting value ($V_{OUT(S)}$). This allows $V_{OUT(S)}$ to be reached without lowering the pre-biased V_{OUT}.
In soft-start circuits which are not pre-bias compatible, a large current flows as a result of the discharge of the residual electric charge through the low side power MOS FET when switching operation starts, which could cause damage, however in a pre-bias compatible soft-start circuit, the IC is protected from the large current when switching operation starts, and it makes power supply design for the application circuit simpler.

In the S-85S1P Series, V_{OUT} reaches $V_{OUT(S)}$ gradually due to the soft-start circuit.
In the following cases, rush current and V_{OUT} overshoot are reduced.

- At power-on
- When the EN pin changes from "L" to "H".
- When UVLO operation is released.
- When thermal shutdown is released.
- At short-circuit recovery

In addition, the soft-start circuit operates under the following conditions.
The soft-start circuit starts operating after "H" is input to the EN pin and the soft-start wait time (t_{SSW}) = 1.5 ms typ. elapses. The soft-start time (t_{SS}) is set to 1.0 ms typ.

- At power supply restart (the IC restart)
- At UVLO detection (after UVLO release)
- At thermal shutdown detection (after thermal shutdown release)
- After Hiccup control

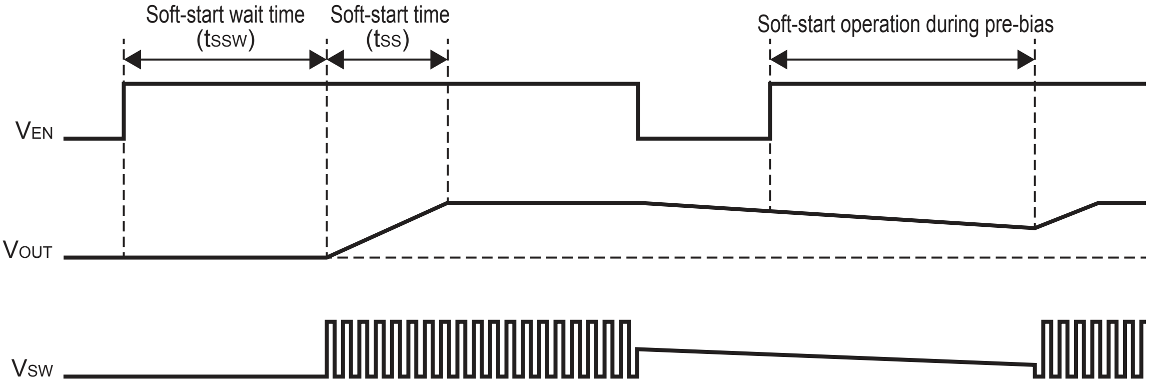


Figure 6

2. Supply voltage divider block

The supply voltage divided output is a function that divides the input voltage (V_{IN}) of the DC-DC converter into $V_{IN}/2$ or $V_{IN}/3$ and outputs the voltage. For example, the microcontroller can monitor battery voltage by inputting the output voltage (V_{PMOUT}) to the A/D converter in the microcontroller. Connecting the IC and the microcontroller makes it possible that it is used as a remained battery capacity monitor for lithium-ion rechargeable batteries, coin batteries, and other batteries.

V_{IN} is divided into $V_{IN}/2$ in S-85S1PCxx, and $V_{IN}/3$ in S-85S1PDxx.
Low output impedance is realized since the buffer amp in the supply voltage divider block constitutes a voltage follower. Each the supply voltage divider block and DC-DC converter block operate independently. When the PMEN pin is "L" and the supply voltage divider block is in standby status, the electrical charge in the output capacitor connected to the PMOUT pin is discharged by an impedance of approximately 2.8 kΩ.

2. 1 Basic operation

Figure 7 shows the block diagram of the supply voltage divider block to describe basic operation.
Reference voltage (V_{refpm}) is generated by dividing the input voltage (V_{IN}) to $V_{IN}/2$ or $V_{IN}/3$ using the dividing resistance (R_{pm1} and R_{pm2}). Since the buffer amplifier constitutes a voltage follower, it can perform the feedback control so that V_{PMOUT} and V_{refpm} are the same. Low output impedance is realized by the buffer amplifier, while outputting V_{PMOUT} according to V_{IN}.
When "L" is input to the PMEN pin the current which flows to R_{pm1} and R_{pm2} and the current which flows to the buffer amplifier can be stopped. The buffer amplifier output is pulled down to V_{SS} by the built-in N-channel transistor, and V_{PMOUT} is set to the V_{SS} level.
The difference, the output offset voltage (V_{POF}), is generated between V_{PMOUT} and $V_{PMOUT(S)}$, and it is expressed with $V_{PMOUT} = V_{PMOUT(S)} + V_{POF}$.
In addition, V_{PMOUT} will change slightly according to the load current, and the value of change is expressed as the output impedance (R_{PS}).

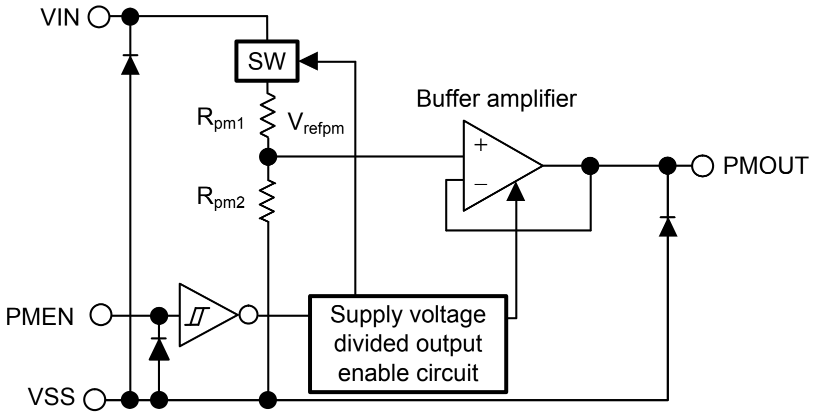


Figure 7

2. 2 PMEN pin

The PMEN pin controls the supply voltage divided output enable circuit.
When "H" is input to the PMEN pin, the supply voltage divided output enable circuit operates. This enables the supply voltage divided output and allows for monitoring of the power supply voltage. When "L" is input to the PMEN pin, the supply voltage divided output enable circuit stops. This disables the supply voltage divided output, reducing the IC current consumption. In addition, the PMEN pin has absolutely no effect on the operation of the DC-DC converter block.

Table 10

PMEN Pin	Supply Voltage Divided Output	Output Voltage (V_{PMOUT})
"H"	Enable (normal operation)	V_{PMOUT}[*1]
"L"	Disable (standby)	V_{SS} level

***1.** Refer to ***1** in **Table 7** in "■ **Electrical Characteristics**".

Figure 8 shows the internal equivalent circuit structure in relation to the PMEN pin. The PMEN pin is neither pulled up nor pulled down, so do not use it in the floating status. When not using the PMEN pin, connect it to the VIN pin. Note that the current consumption increases when a voltage of 0.25 V to V_{IN} – 0.3 V is applied to the PMEN pin.

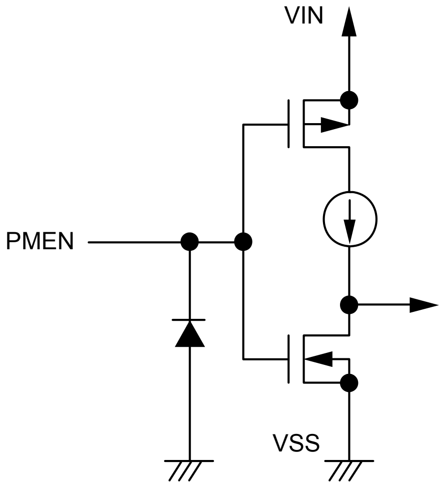


Figure 8

2. 3 PMEN pin voltage and output voltage (V_{PMOUT})

Figure 9 shows the relation between the PMEN pin voltage and the supply voltage divided output.
When "H" is input to the PMEN pin, the supply voltage divided output is enabled. Once set-up time (t_{PU}) = 10 ms max.[*1] elapses, the output voltage (V_{PMOUT}) will settle and the power supply voltage can be monitored.
When "L" is input to the PMEN pin, the supply voltage divided output is disabled. V_{PMOUT} is set to the V_{SS} level by the built-in N-channel transistor.
By inputting "H" and "L" alternately to the PMEN pin, allowing for minimization of current consumption during the period when the power supply voltage is not monitored.

***1.** Ta = +25°C, V_{IN} = 3.6 V, C_{PM} = 0.22 μF, no load

Active "H"

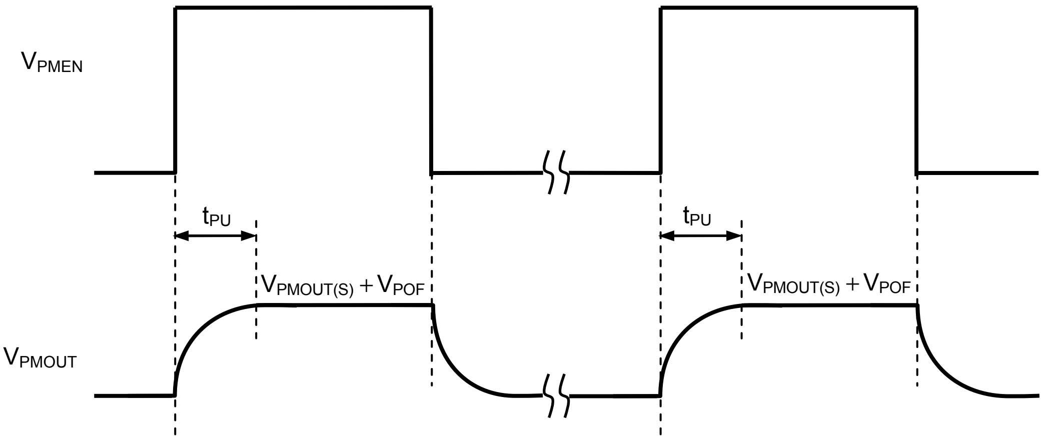


Figure 9

Remark $V_{PMEN} = V_{IN} \leftrightarrow V_{SS}$

■ Typical Application

Figure 10 shows the circuit diagram of the typical application in the S-85S1P Series, and **Figure 11** shows the timing chart.

As shown in **Figure 10**, connect the PMOUT pin to an analog input pin (AIN pin) of the A/D converter in the microcontroller. The microcontroller can monitor the battery voltage by inputting the output voltage (V_{PMOUT}) to the A/D converter.
The input voltage from the battery is converted to output voltage by the switching operation, and the microcontroller starts driving with the voltage. The supply voltage divided output can be controlled by inputting "H" and "L" signals output from the microcontroller I/O pin to the PMEN pin. Control the supply voltage divided output according to the A/D converter operation timing.

When inputting "H" to the PMEN pin, the microcontroller monitors the battery voltage. The IC current consumption can be minimized by inputting "L" to the PMEN pin when battery voltage is not monitored.

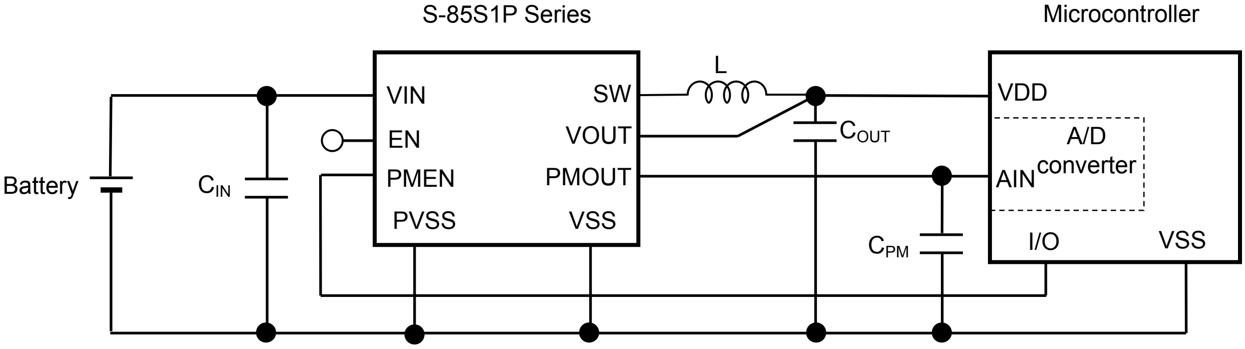

S-85S1P Series
Microcontroller
L
VIN
EN
PMEN
PVSS
SW
VOUT
PMOUT
VSS
COUT
CPM
Battery
CIN
VDD
A/D converter
AIN
I/O
VSS

Figure 10

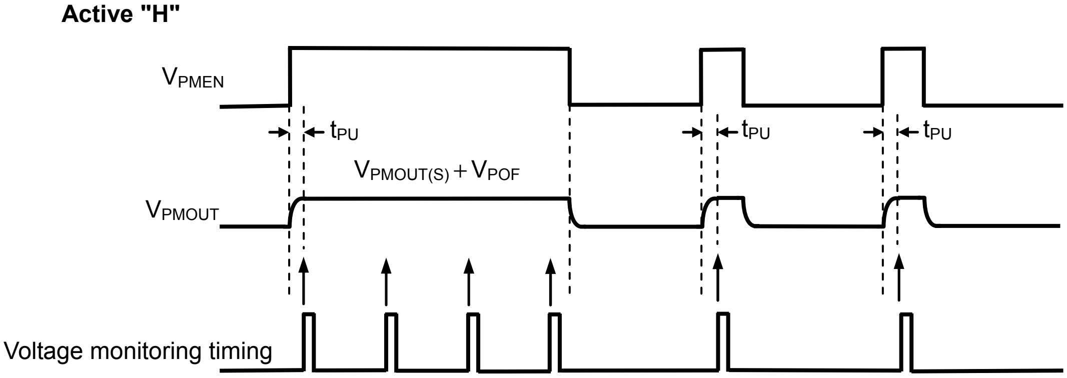

Active "H"
VPMEN
tPU
tPU
tPU
VPMOUT(S) + VPOF
VPMOUT
Voltage monitoring timing

Figure 11

■ Typical Circuit

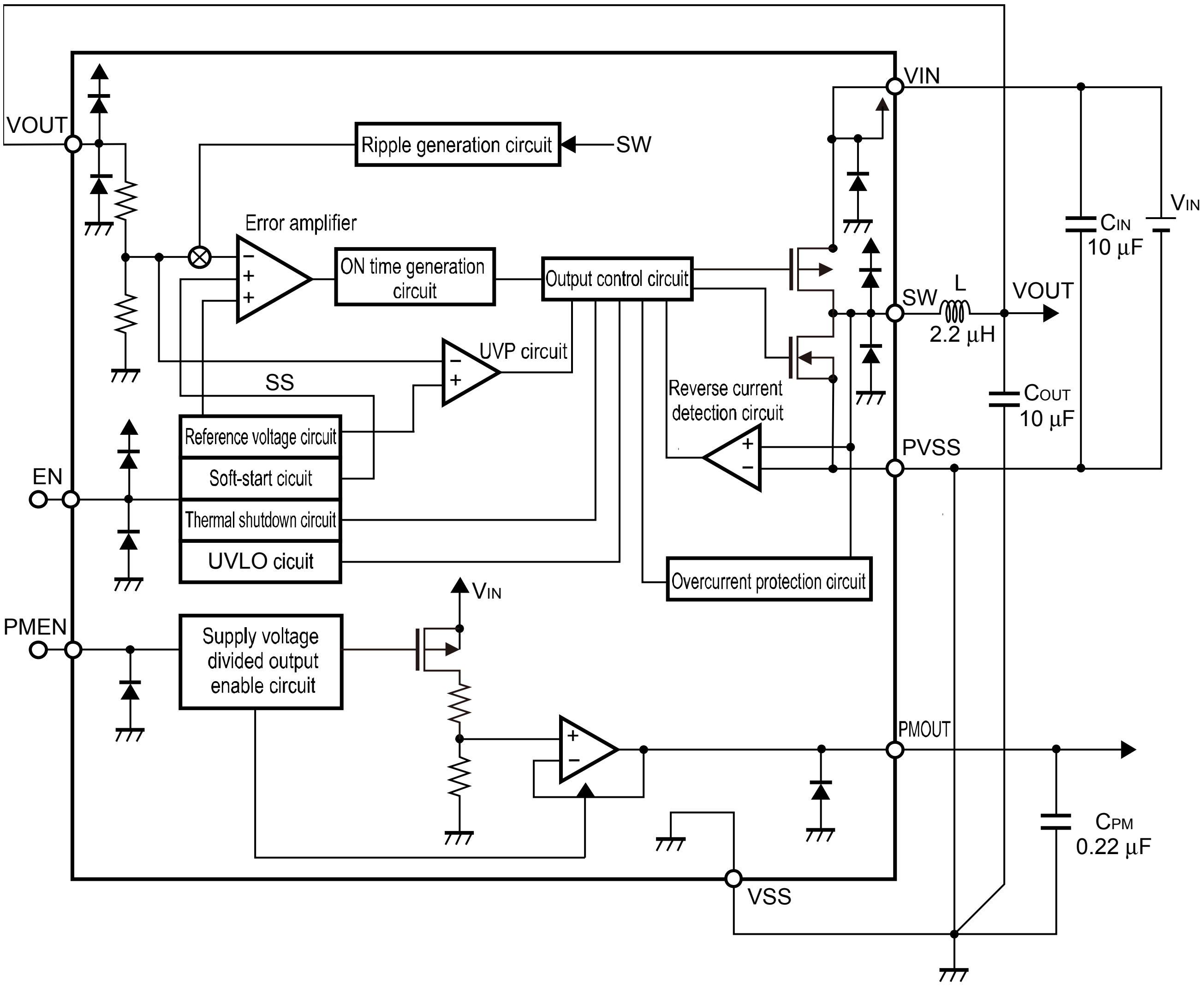

VIN
VOUT
Ripple generation circuit
SW
Error amplifier
ON time generation circuit
Output control circuit
CIN
10 µF
VIN
SW
L
2.2 µH
VOUT
UVP circuit
SS
Reverse current detection circuit
COUT
10 µF
PVSS
Reference voltage circuit
Soft-start cicuit
EN
Thermal shutdown circuit
UVLO cicuit
Overcurrent protection circuit
VIN
PMEN
Supply voltage divided output enable circuit
PMOUT
CPM
0.22 µF
VSS

Figure 12

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

■ External Parts Selection

Selectable values and recommended values for external parts are shown in **Table 11**.
Use ceramic capacitors for C_{IN} and C_{OUT}.

Table 11

Item	Input Capacitor (C_{IN})	Output Capacitor (C_{OUT})	Inductor (L)	Supply Voltage Divider Block Output Capacitor (C_{PM})
Selectable value	2.2 μF or larger	4.7 μF to 100 μF	1.5 μH to 10 μH	0.10 μF to 0.22 μF
Recommended value	10 μF	10 μF	2.2 μH	−

1. DC-DC converter block input capacitor (C_{IN})

C_{IN} can lower the power supply impedance, average the input current, improve the efficiency and noise tolerance. Select a capacitor according to the impedance of the power supply to be used. Also take into consideration the DC bias characteristics of the capacitor to be used.

2. DC-DC converter block output capacitor (C_{OUT})

C_{OUT} is used to smooth output voltage. If the capacitance is large, the overshoot and undershoot during load transient and output ripple voltage can be improved even more. Select a proper capacitor after the sufficient evaluation under actual conditions.

Table 12 Recommended Capacitors (C_{IN}, C_{OUT}) List (at $V_{OUT(S)} \leq 3.3$ V)

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
Murata Manufacturing Co., Ltd.	GRM155R60J106ME15	10 μF	6.3 V	1.0 mm × 0.5 mm × 0.5 mm
TDK Corporation	C1608X5R0J106K080AB	10 μF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm
Murata Manufacturing Co., Ltd.	GRM185R60J106ME15	10 μF	6.3 V	1.6 mm × 0.8 mm × 0.5 mm

Table 13 Recommended Capacitors (C_{IN}, C_{OUT}) List (at $V_{OUT(S)} > 3.3$ V)

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	C1608X5R0J106K080AB	10 μF	6.3 V	1.6 mm × 0.8 mm × 0.8 mm
Murata Manufacturing Co., Ltd.	GRM185R60J106ME15	10 μF	6.3 V	1.6 mm × 0.8 mm × 0.5 mm

3. DC-DC converter block inductor (L)

When selecting L, note the allowable current. If a current exceeding this allowable current flows through the inductor, magnetic saturation may occur, and there may be risks which substantially lower efficiency and damage the IC as a result of large current.
Therefore, select an inductor so that peak current value (I_{PK}), even during overcurrent detection, does not exceed the allowable current.
When prioritizing the load response, select an inductor with a small L value such as 2.2 μH. When prioritizing the efficiency, select an inductor with a large L value such as 10 μH. I_{PK} is calculated using the following expression.

$$I_{PK} = I_{OUT} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

Table 14 Recommended Inductors (L) List

Manufacturer	Part Number	Inductance	Rated Current	Dimensions (L × W × H)
ALPS ELECTRIC CO., LTD.	GLUHK2R201A	2.2 μH	1700 mA	2.0 mm × 1.6 mm × 1.0 mm
Murata Manufacturing Co., Ltd.	DFE201210S-2R2M=P2	2.2 μH	2000 mA	2.0 mm × 1.2 mm × 1.0 mm
Würth Elektronik GmbH & Co. KG	74438343022	2.2 μH	1100 mA	2.0 mm × 1.6 mm × 1.0 mm
Murata Manufacturing Co., Ltd.	LQM2MPN2R2MGH	2.2 μH	1300 mA	2.0 mm × 1.6 mm × 0.9 mm
TDK Corporation	MLP2016G2R2M	2.2 μH	850 mA	2.0 mm × 1.6 mm × 1.0 mm
Coilcraft, Inc.	PFL2015-222ME	2.2 μH	1050 mA	2.2 mm × 1.45 mm × 1.5 mm

4. Supply voltage divider block output capacitor (C_{PM})

When selecting C_{PM}, take into consideration the operation stability. If the capacitance is large, the rising time until V_{PMOUT} reaches the intended voltage (set-up time (t_{PU})) will be longer.

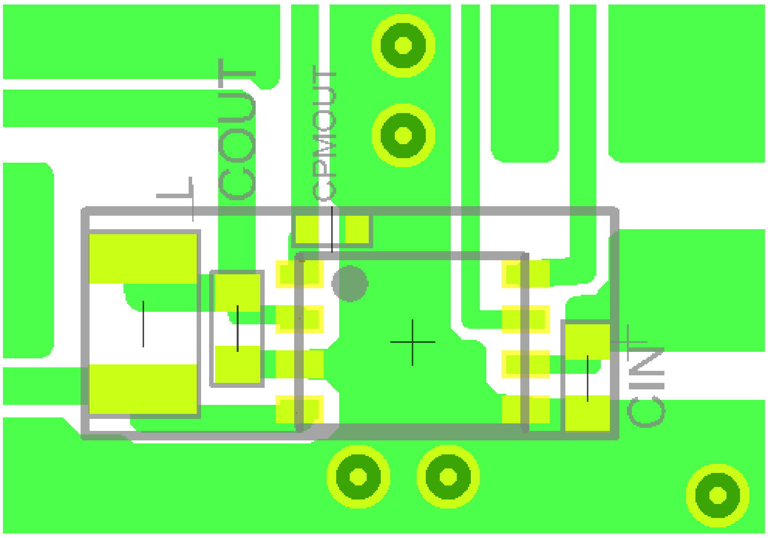
Table 15 Recommended Capacitors (C_{PM}) List

Manufacturer	Part Number	Capacitance	Withstanding Voltage	Dimensions (L × W × H)
TDK Corporation	CGA2B2X5R1A104M050BA	0.10 μF	6.3 V	1.0 mm × 0.5 mm × 0.5 mm
TDK Corporation	C0603X5R0J224M030BB	0.22 μF	6.3 V	0.6 mm × 0.3 mm × 0.3 mm
Murata Manufacturing Co., Ltd.	GRM033R60J104ME19	0.10 μF	6.3 V	0.6 mm × 0.3 mm × 0.3 mm
Murata Manufacturing Co., Ltd.	GRM033R60J224ME90	0.22 μF	6.3 V	0.6 mm × 0.3 mm × 0.3 mm

■ Board Layout Guidelines

Note the following cautions when determining the board layout for the S-85S1P Series.

- Place C_{IN} as close to the VIN pin and the PVSS pin as possible.
- Make the VIN pattern and GND pattern as wide as possible.
- Place thermal vias in the GND pattern to ensure sufficient heat dissipation.
- Keep thermal vias near C_{IN} and C_{OUT} approximately 3 mm to 4 mm away from capacitor pins.
- Large current flows through the SW pin. Make the wiring area of the pattern to be connected to the SW pin small to minimize parasitic capacitance and emission noise.
- Do not wire the SW pin pattern under the IC.



Total size: 5.7 mm × 2.4 mm = 13.7 mm^2

Figure 13 Reference Board Pattern

Caution The above pattern diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to determine the pattern.

Remark Refer to the land drawing of SNT-8A and "**SNT Package User's Guide**".

■ Precautions

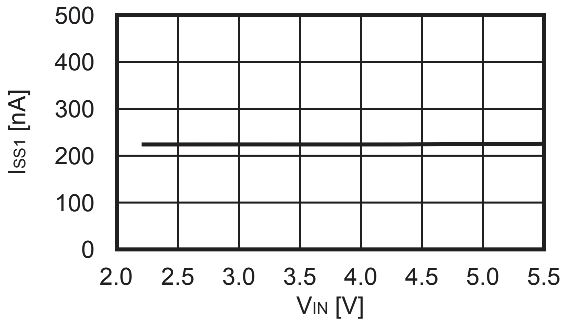
- Mount external capacitors and inductors as close as possible to the IC, and make single GND.
- Characteristic ripple voltage and spike noise occur in the IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply to be used, fully check them using an actually mounted model.
- The 10 μF capacitor connected between the VIN pin and the VSS pin is a bypass capacitor. It stabilizes the power supply in the IC when application is used with a heavy load, and thus effectively works for stable switching regulator operation. Allocate the bypass capacitor as close to the IC as possible, prioritized over other parts.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- The power dissipation of the IC greatly varies depending on the size and material of the board to be connected. Perform sufficient evaluation using an actual application before designing.
- ABLIC Inc. assumes no responsibility for the way in which this IC is used on products created using this IC or for the specifications of that product, nor does ABLIC Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

■ Characteristics (Typical Data)

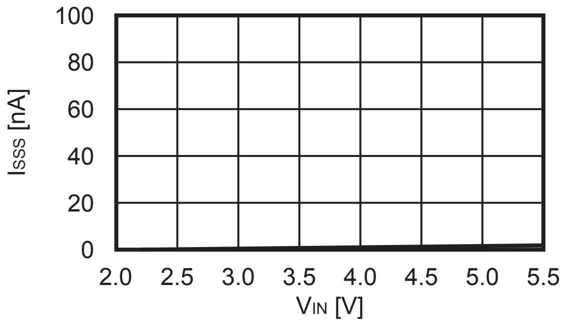
1. Example of major power supply dependence characteristics (Ta = +25°C)

DC-DC converter block

1. 1 Current consumption during switching off (I_{SS1}) vs. Input voltage (V_{IN})

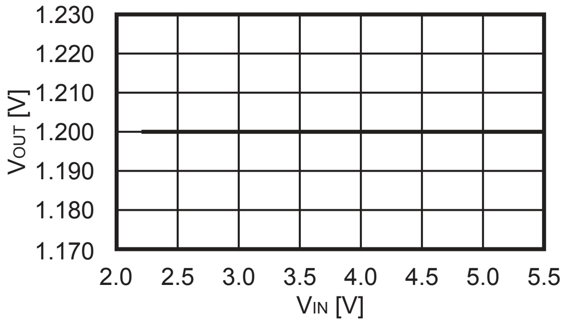


1. 2 Current consumption during shutdown (I_{SSS}) vs. Input voltage (V_{IN})



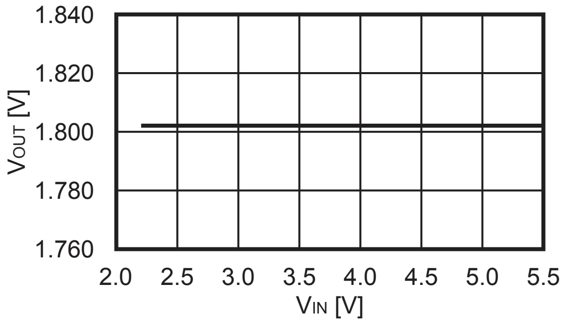
1. 3 Output voltage (V_{OUT}) vs. Input voltage (V_{IN})

$V_{OUT(S)}$ = 1.2 V



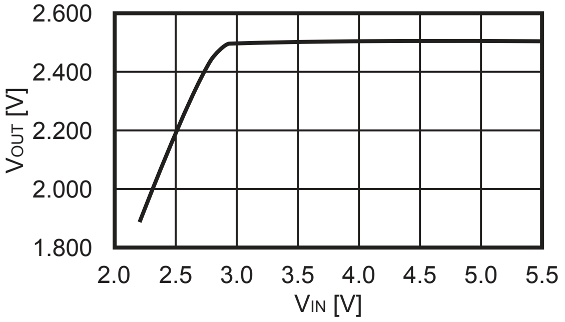
1. 4 Output voltage (V_{OUT}) vs. Input voltage (V_{IN})

$V_{OUT(S)}$ = 1.8 V



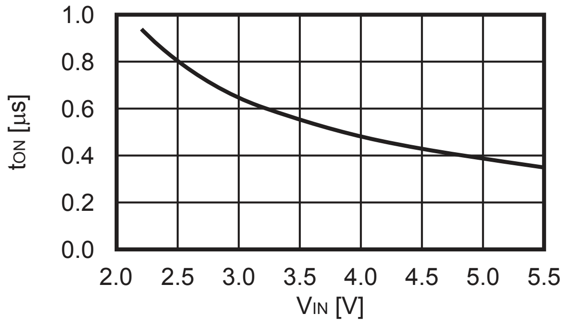
1. 5 Output voltage (V_{OUT}) vs. Input voltage (V_{IN})

$V_{OUT(S)}$ = 2.5 V



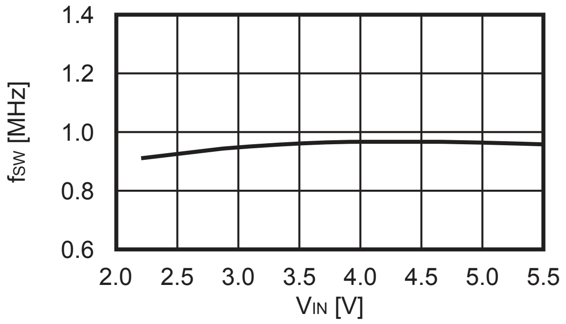
1. 6 ON time (t_{ON}) vs. Input voltage (V_{IN})

$V_{OUT(S)}$ = 1.8 V

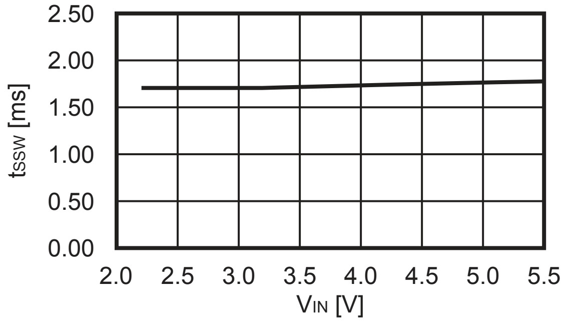


1. 7 Switching frequency (f_{SW}) vs. Input voltage (V_{IN})

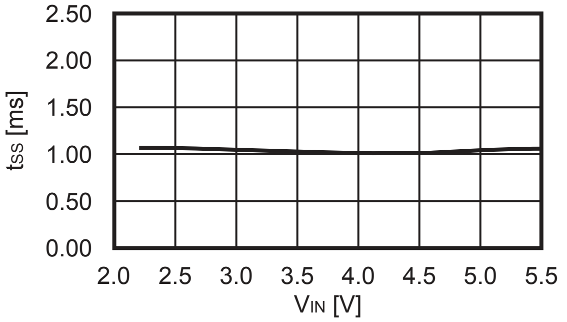
$V_{OUT(S)}$ = 1.8 V



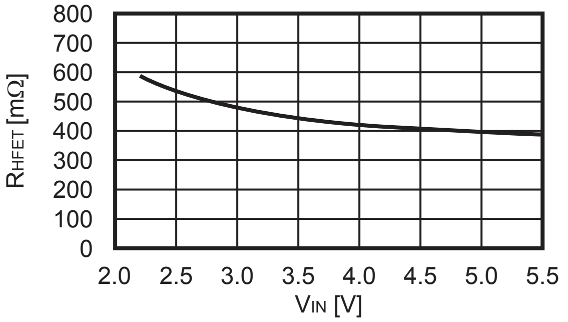
1. 8 Soft-start wait time (t_{SSW}) vs. Input voltage (V_{IN})



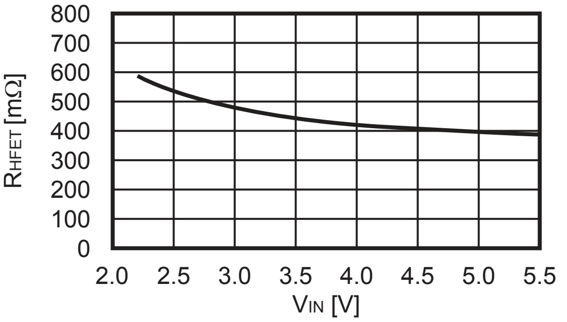
1. 9 Soft-start time (t_{SS}) vs. Input voltage (V_{IN})



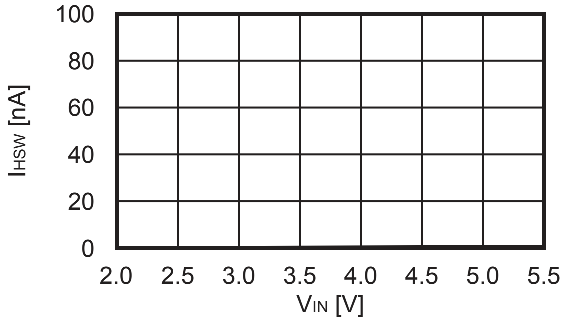
1. 10 High side power MOS FET on-resistance (R_{HFET}) vs. Input voltage (V_{IN})



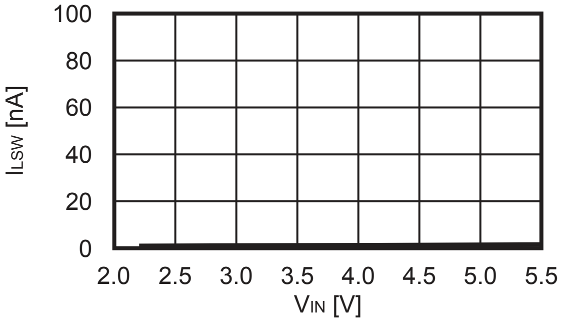
1. 11 Low side power MOS FET on-resistance (R_{LFET}) vs. Input voltage (V_{IN})



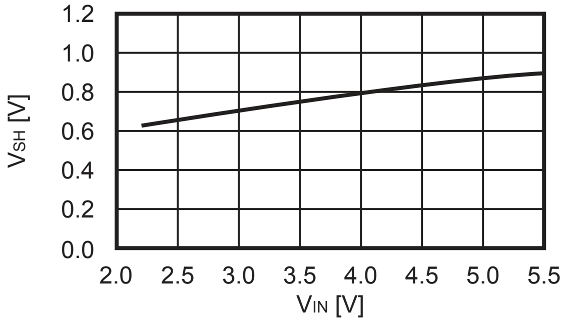
1. 12 High side power MOS FET leakage current (I_{HSW}) vs. Input voltage (V_{IN})



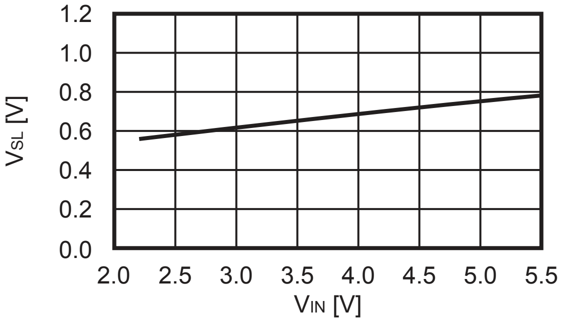
1. 13 Low side power MOS FET leakage current (I_{LSW}) vs. Input voltage (V_{IN})



1. 14 High level input voltage (V_{SH}) vs. Input voltage (V_{IN})



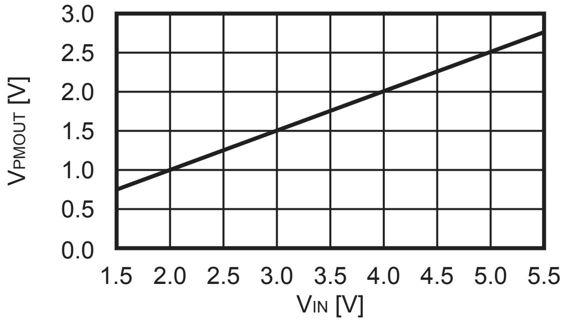
1. 15 Low level input voltage (V_{SL}) vs. Input voltage (V_{IN})



Supply voltage divider block

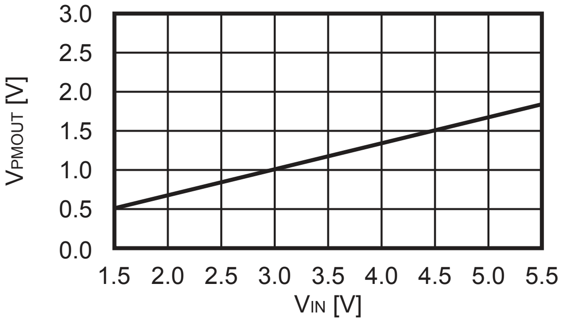
1. 16 Output voltage (V_{PMOUT}) vs. Input voltage (V_{IN})

$V_{PMOUT(S)} = V_{IN}/2$

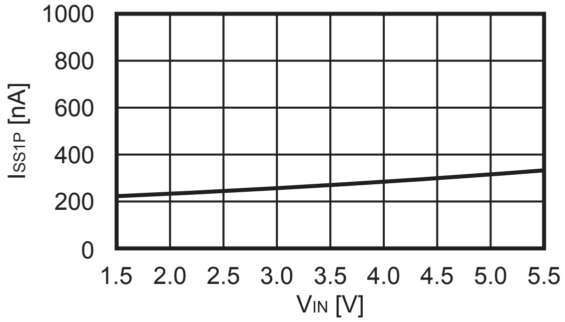


1. 17 Output voltage (V_{PMOUT}) vs. Input voltage (V_{IN})

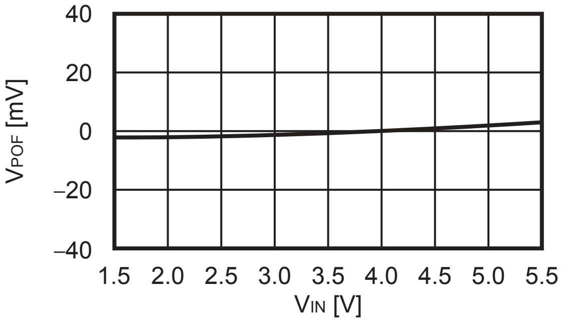
$V_{PMOUT(S)} = V_{IN}/3$



1. 18 Current consumption during operation (I_{SS1P}) vs. Input voltage (V_{IN})

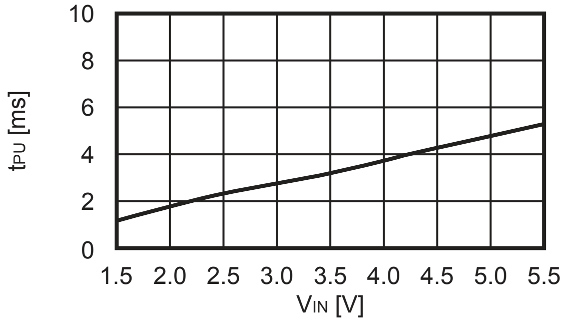


1. 19 Output offset voltage (V_{POF}) vs. Input voltage (V_{IN})



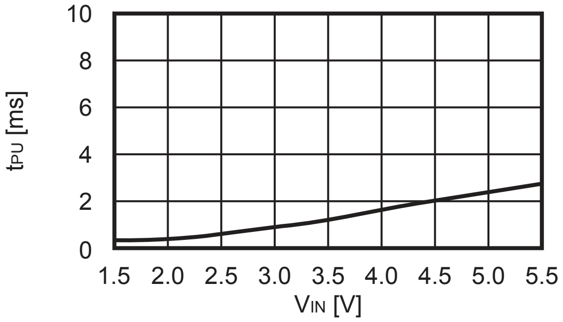
1. 20 Set-up time (t_{PU}) vs. Input voltage (V_{IN})

$V_{PMOUT(S)} = V_{IN}/2$, $C_{PM} = 0.22\ \mu F$

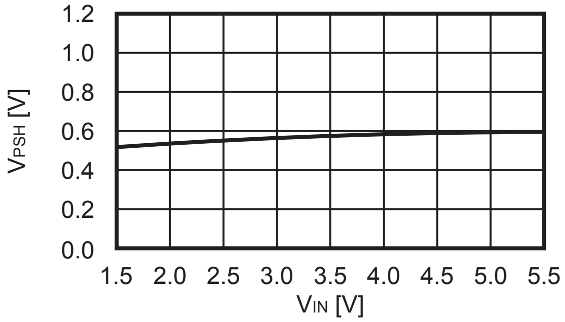


1. 21 Set-up time (t_{PU}) vs. Input voltage (V_{IN})

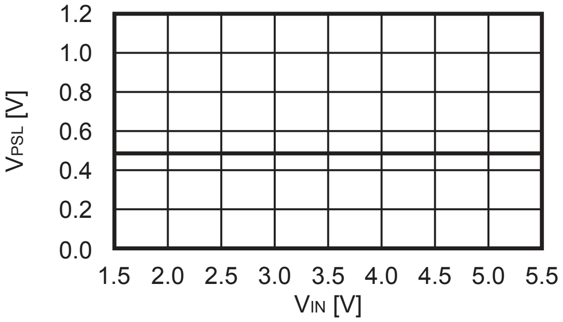
$V_{PMOUT(S)} = V_{IN}/3$, $C_{PM} = 0.22\ \mu F$



1. 22 PMEN pin input voltage "H" (V_{PSH}) vs. Input voltage (V_{IN})



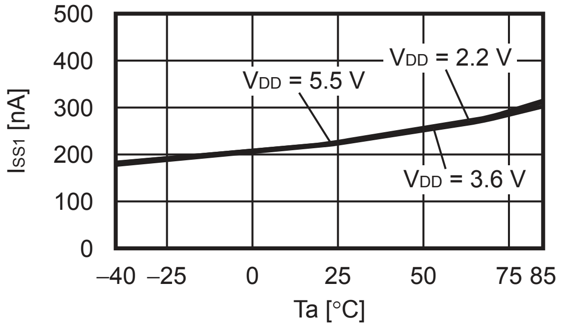
1. 23 PMEN pin input voltage "L" (V_{PSL}) vs. Input voltage (V_{IN})



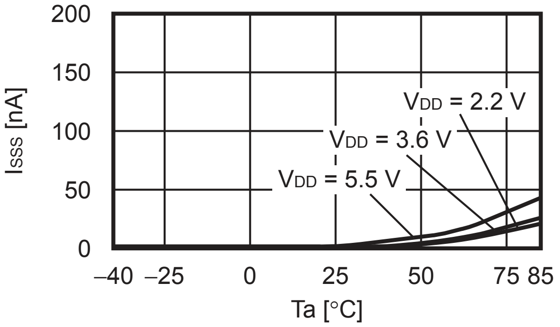
2. Example of major temperature characteristics (Ta = –40°C to +85°C)

DC-DC converter block

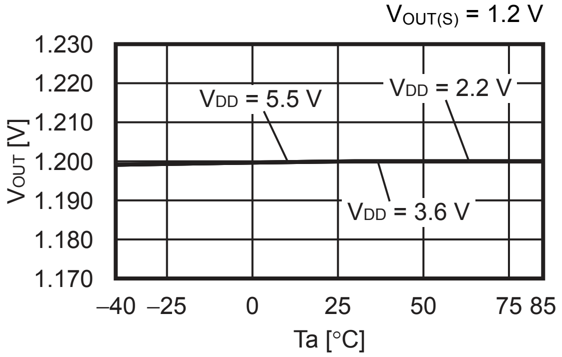
2. 1 Current consumption during switching off (I_{SS1}) vs. Temperature (Ta)



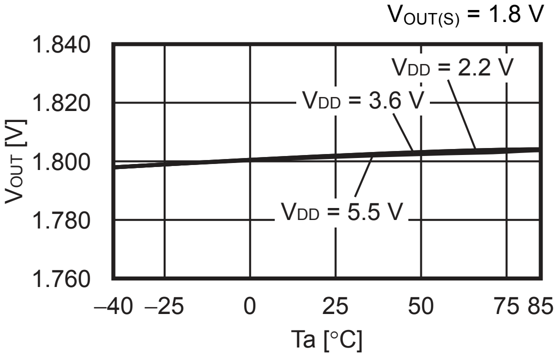
2. 2 Current consumption during shutdown (I_{SSS}) vs. Temperature (Ta)



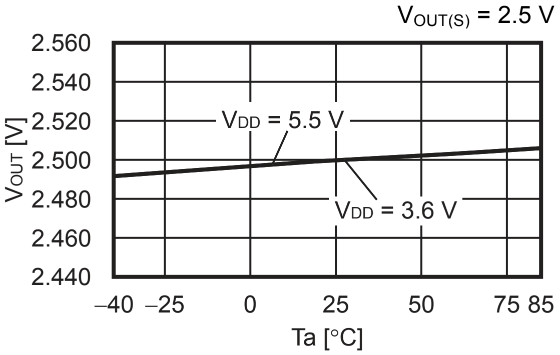
2. 3 Output voltage (V_{OUT}) vs. Temperature (Ta)



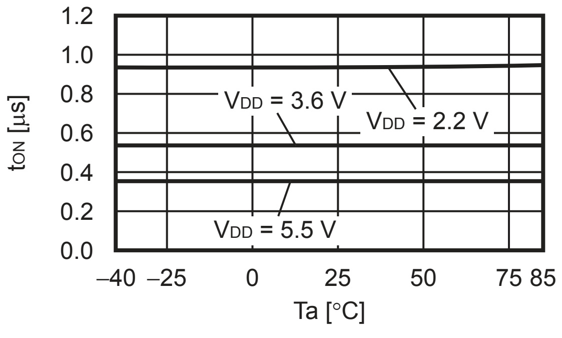
2. 4 Output voltage (V_{OUT}) vs. Temperature (Ta)



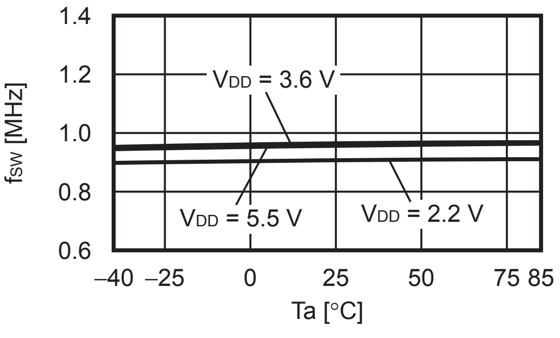
2. 5 Output voltage (V_{OUT}) vs. Temperature (Ta)



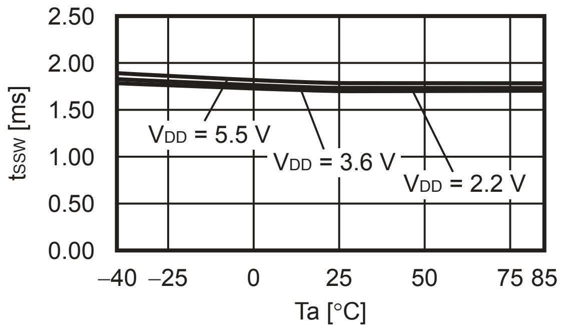
2. 6 ON time (t_{ON}) vs. Temperature (Ta)



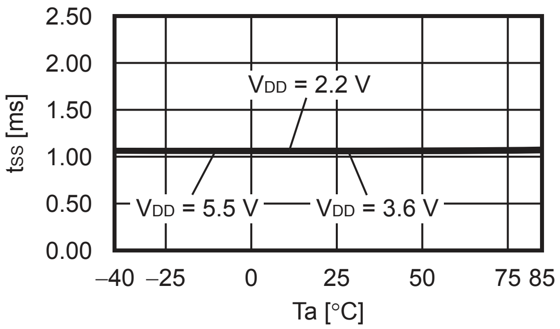
2. 7 Switching frequency (f_{SW}) vs. Temperature (Ta)



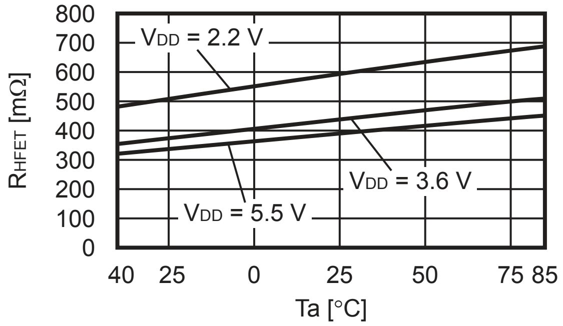
2. 8 Soft-start wait time (t_{SSW}) vs. Temperature (Ta)



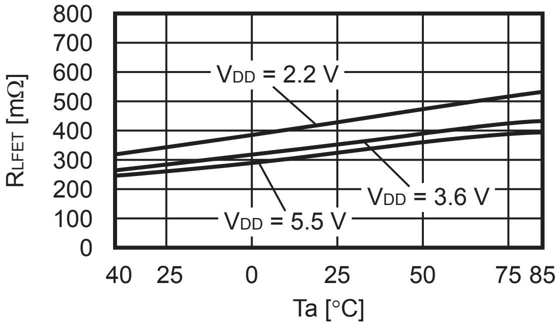
2. 9 Soft-start time (t_{SS}) vs. Temperature (Ta)



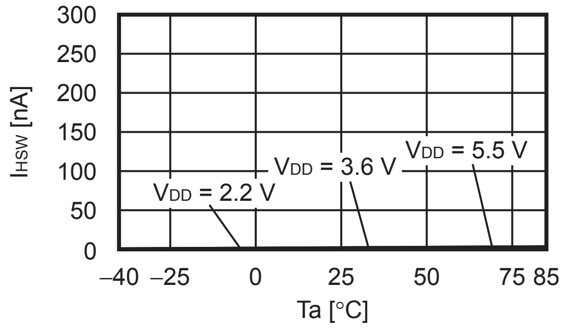
2. 10 High side power MOS FET on-resistance (R_{HFET}) vs. Temperature (Ta)



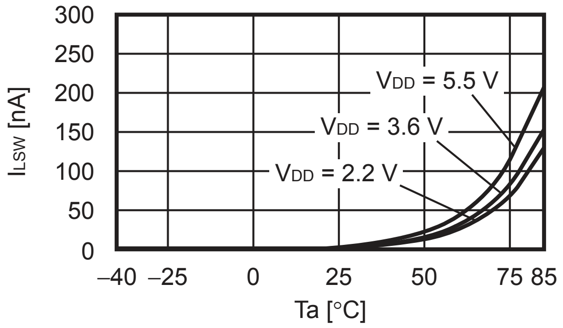
2. 11 Low side power MOS FET on-resistance (R_{LFET}) vs. Temperature (Ta)



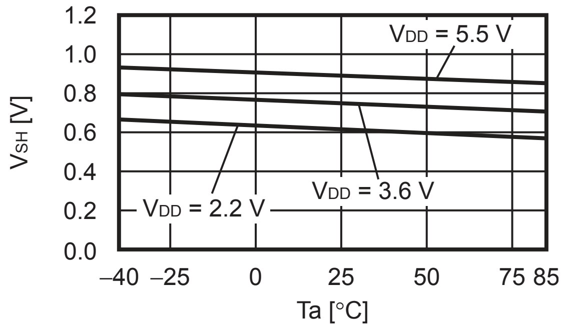
2. 12 High side power MOS FET leakage current (I_{HSW}) vs. Temperature (Ta)



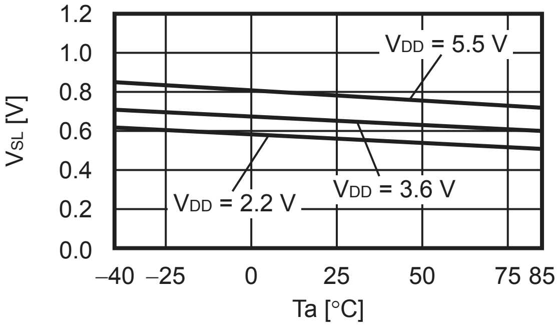
2. 13 Low side power MOS FET leakage current (I_{LSW}) vs. Temperature (Ta)



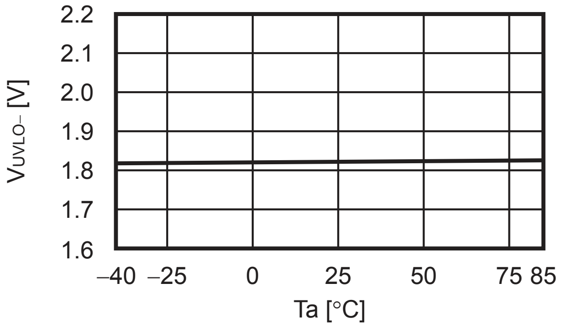
2. 14 High level input voltage (V_{SH}) vs. Temperature (Ta)



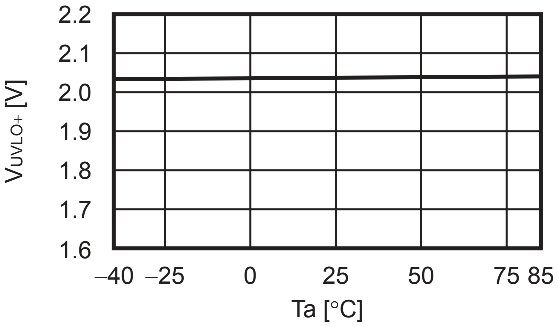
2. 15 Low level input voltage (V_{SL}) vs. Temperature (Ta)



2. 16 UVLO detection voltage (V_{UVLO-}) vs. Temperature (Ta)



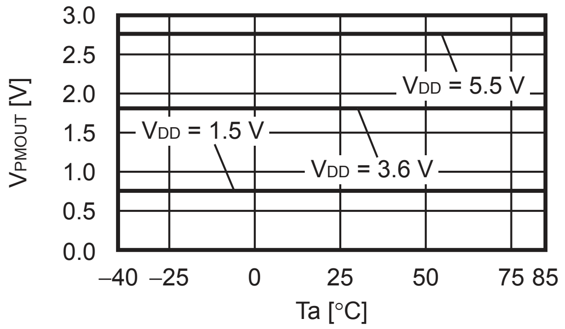
2. 17 UVLO release voltage (V_{UVLO+}) vs. Temperature (Ta)



Supply voltage divider block

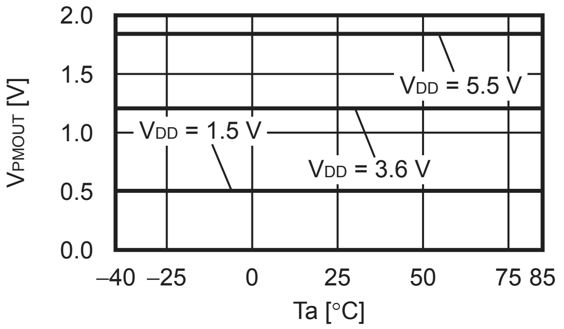
2. 18 Output voltage (V_{PMOUT}) vs. Temperature (Ta)

$V_{PMOUT(S)} = V_{IN}/2$

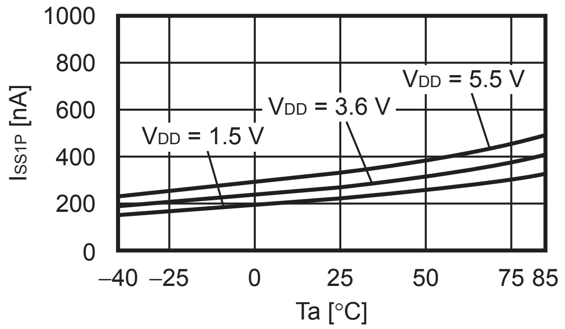


2. 19 Output voltage (V_{PMOUT}) vs. Temperature (Ta)

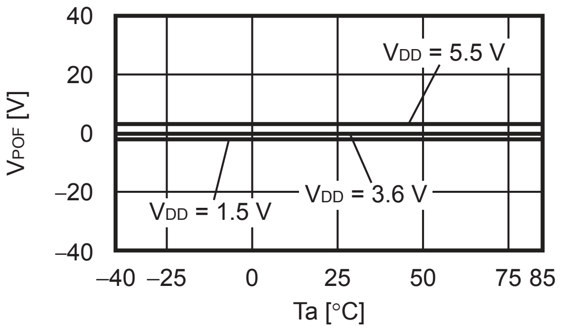
$V_{PMOUT(S)} = V_{IN}/3$



2. 20 Current consumption during operation (I_{SS1P}) vs. Temperature (Ta)

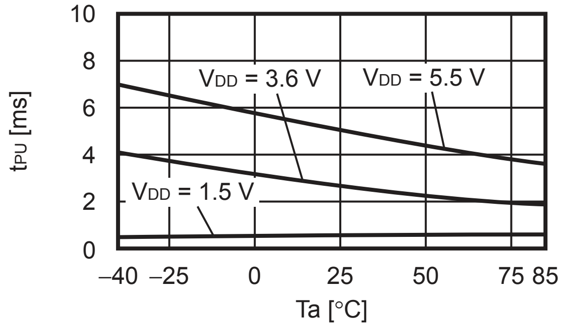


2. 21 Output offset voltage (V_{POF}) vs. Temperature (Ta)



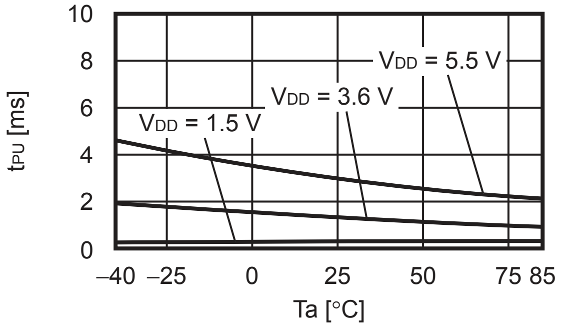
2. 22 Set-up time (t_{PU}) vs. Temperature (Ta)

$V_{PMOUT(S)} = V_{IN}/2$, $C_{PM} = 0.22\ \mu F$

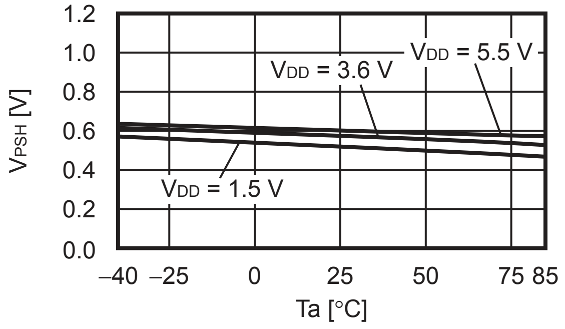


2. 23 Set-up time (t_{PU}) vs. Temperature (Ta)

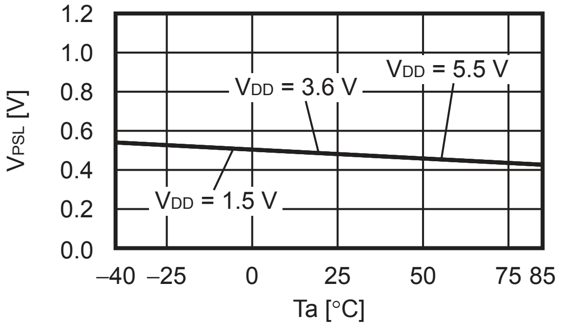
$V_{PMOUT(S)} = V_{IN}/3$, $C_{PM} = 0.22\ \mu F$



2. 24 PMEN pin input voltage (V_{PSH}) vs. Temperature (Ta)



2. 25 PMEN pin input voltage (V_{PSL}) vs. Temperature (Ta)



3. Transient response characteristics

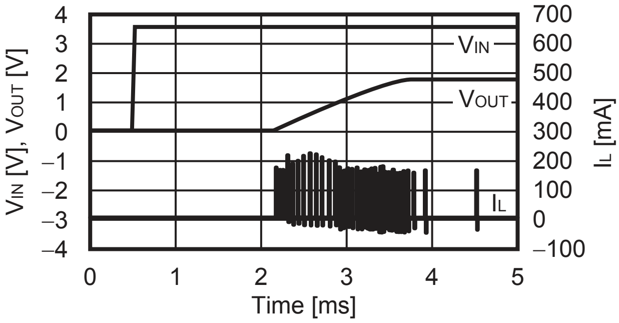
The external parts shown in **Table 16** are used in "**3. Transient response characteristics**".

Table 16

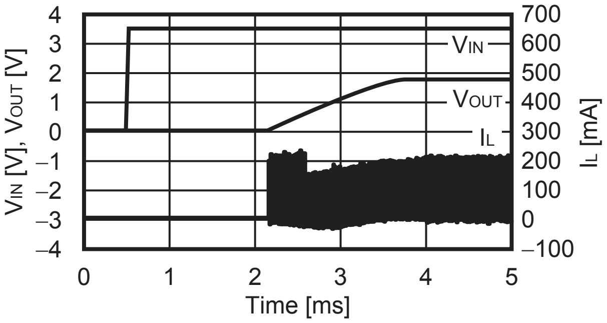
Element Name	Constant	Manufacturer	Part Number
Inductor	2.2 μH	ALPS ELECTRIC CO., LTD.	GLUHK2R201A
Input capacitor	10 μF	TDK Corporation	C1608X5R0J106K080AB
Output capacitor	10 μF	TDK Corporation	C1608X5R0J106K080AB

3. 1 Power-on (V_{OUT} = 1.8 V, V_{IN} = 0 V → 3.6 V, Ta = +25°C)

3. 1. 1 I_{OUT} = 0.1 mA

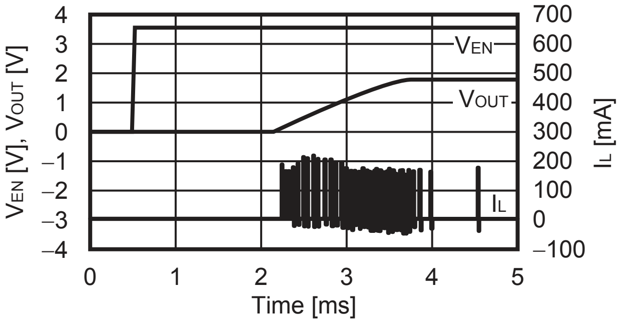


3. 1. 2 I_{OUT} = 200 mA

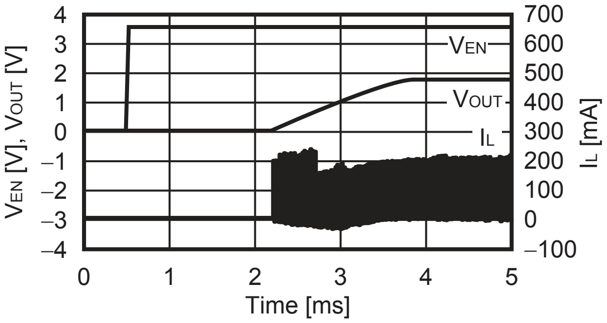


3. 2 Transient response characteristics of EN pin
(V_{OUT} = 1.8 V, V_{IN} = 3.6 V, V_{EN} = 0 V → 3.6 V, Ta = +25°C)

3. 2. 1 I_{OUT} = 0.1 mA

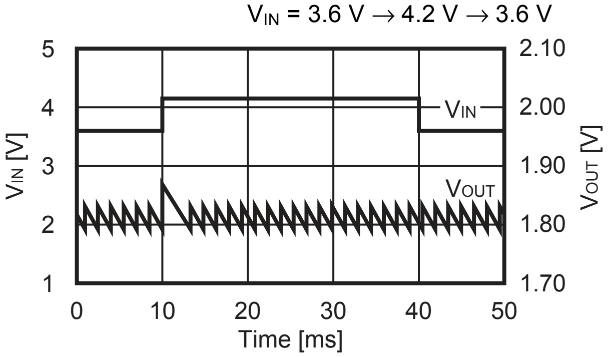


3. 2. 2 I_{OUT} = 200 mA

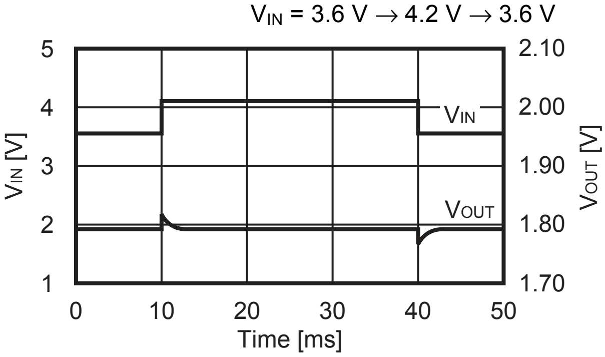


3. 3 Power supply fluctuation (V_{OUT} = 1.8 V, Ta = +25°C)

3. 3. 1 I_{OUT} = 0.1 mA

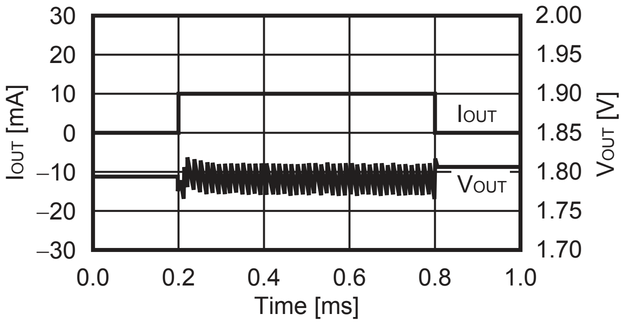


3. 3. 2 I_{OUT} = 200 mA

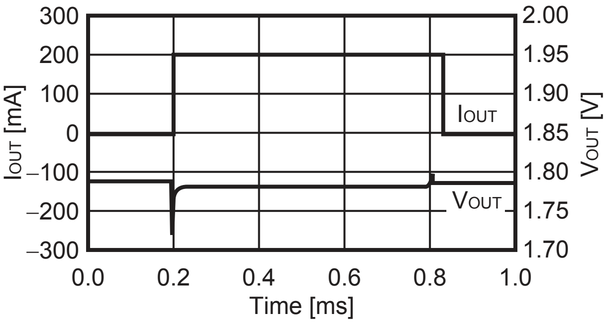


3. 4 Load fluctuation (V_{OUT} = 1.8 V, V_{IN} = 3.6 V, Ta = +25°C)

3. 4. 1 I_{OUT} = 0.1 mA → 10 mA → 0.1 mA



3. 4. 2 I_{OUT} = 0.1 mA → 200 mA → 0.1 mA



■ Reference Data

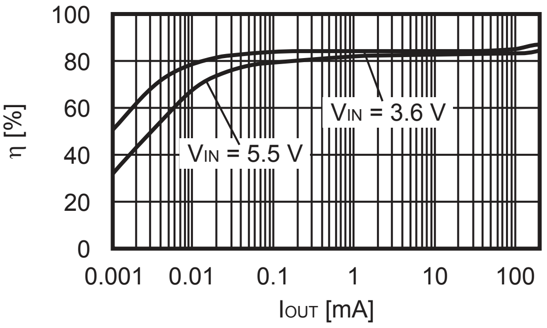
The external parts shown in **Table 17** are used in "**■ Reference Data**".

Table 17

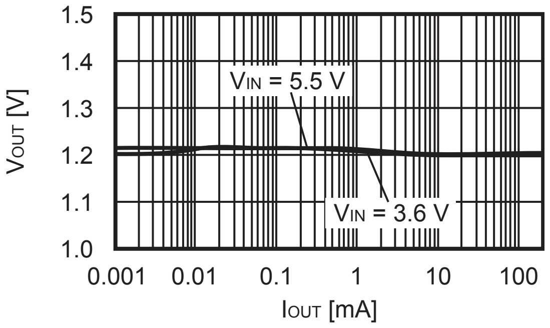
Condition	Inductor (L)	Input Capacitor (C_{IN})	Output Capacitor (C_{OUT})
<1>	GLUHK2R201A (2.2 μH) ALPS ELECTRIC CO., LTD	C1005X5R0J106M050BC (10 μF) TDK Corporation	C1005X5R0J106M050BC (10 μF) TDK Corporation
<2>	DFE201210S (2.2 μH) Toko Ink.	C1005X5R0J106M050BC (10 μF) TDK Corporation	C1005X5R0J106M050BC (10 μF) TDK Corporation

1. V_{OUT} = 1.2 V (External parts: Condition<1>)

1. 1 Efficiency (η) vs. Output current (I_{OUT})

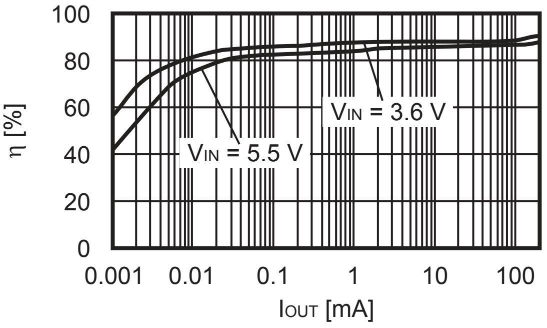


1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

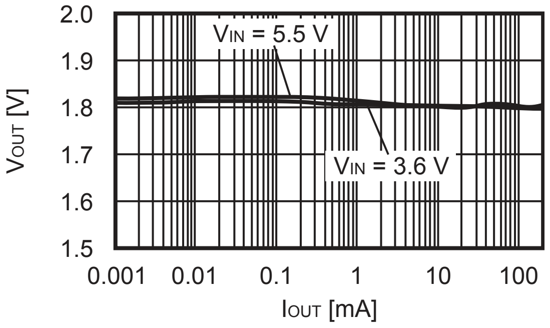


2. V_{OUT} = 1.8 V (External parts: Condition<1>)

2. 1 Efficiency (η) vs. Output current (I_{OUT})

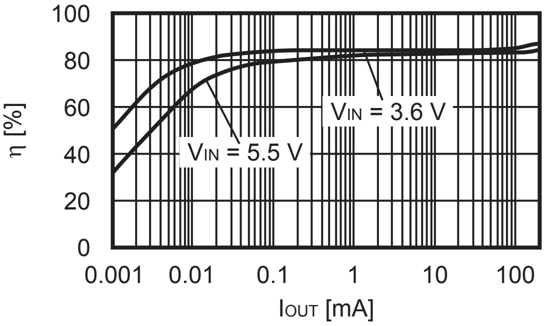


2. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

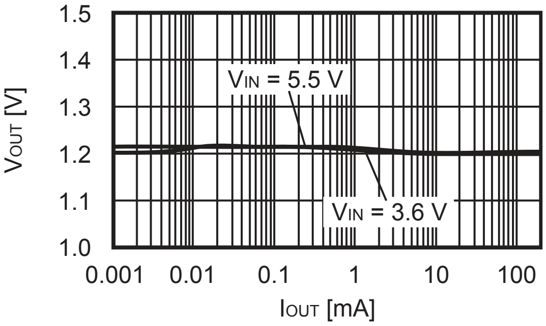


3. V_{OUT} = 1.2 V (External parts: Condition<2>)

3. 1 Efficiency (η) vs. Output current (I_{OUT})

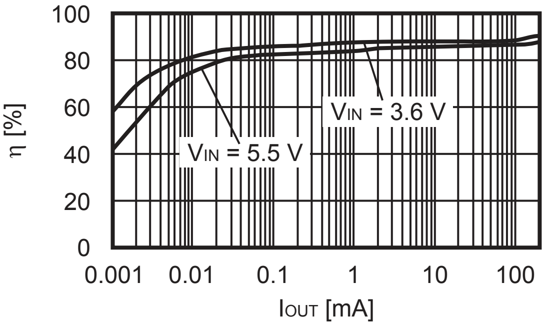


3. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

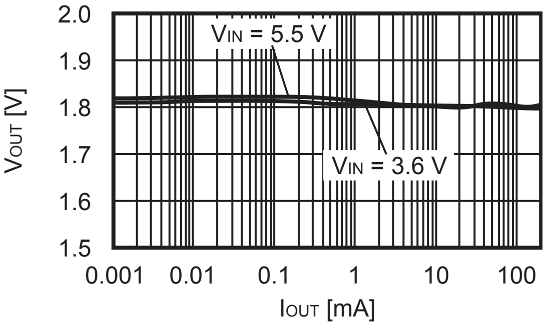


4. V_{OUT} = 1.8 V (External parts: Condition<2>)

4. 1 Efficiency (η) vs. Output current (I_{OUT})

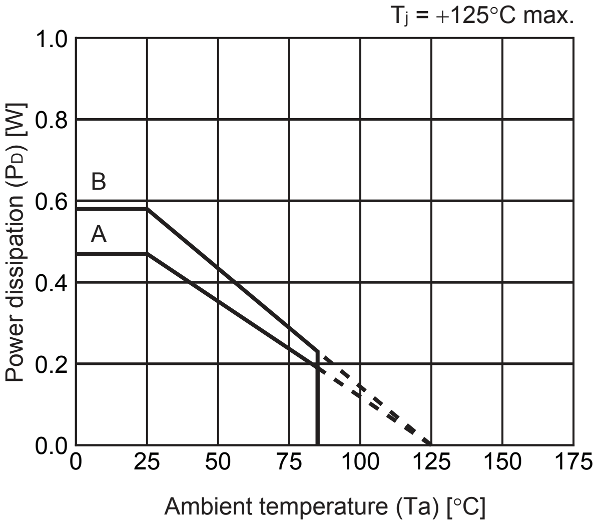


4. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})



■ Power Dissipation

SNT-8A

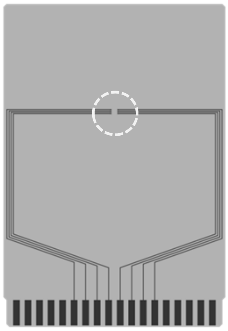


Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	−
D	−
E	−

SNT-8A Test Board

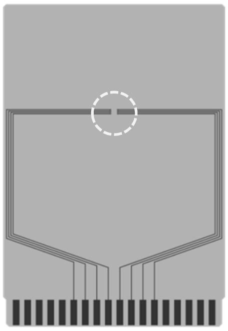
◌ IC Mount Area

(1) Board A

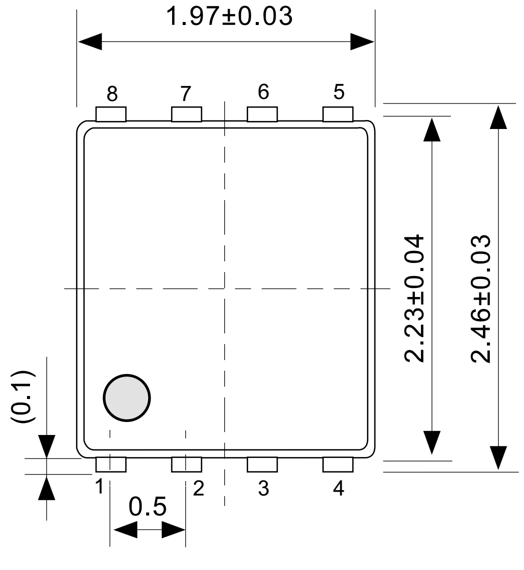


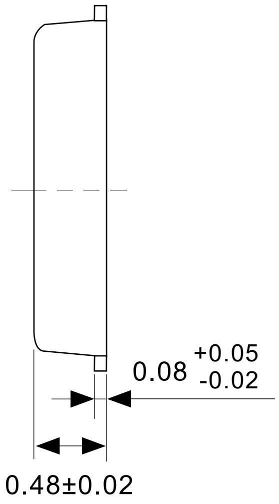
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

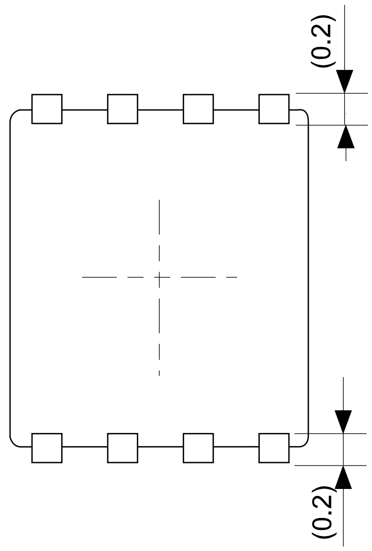
(2) Board B

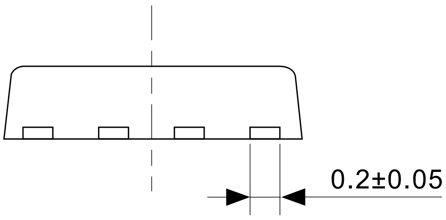


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-


1.97±0.03
8
7
6
5
2.23±0.04
2.46±0.03
(0.1)
1
2
3
4
0.5

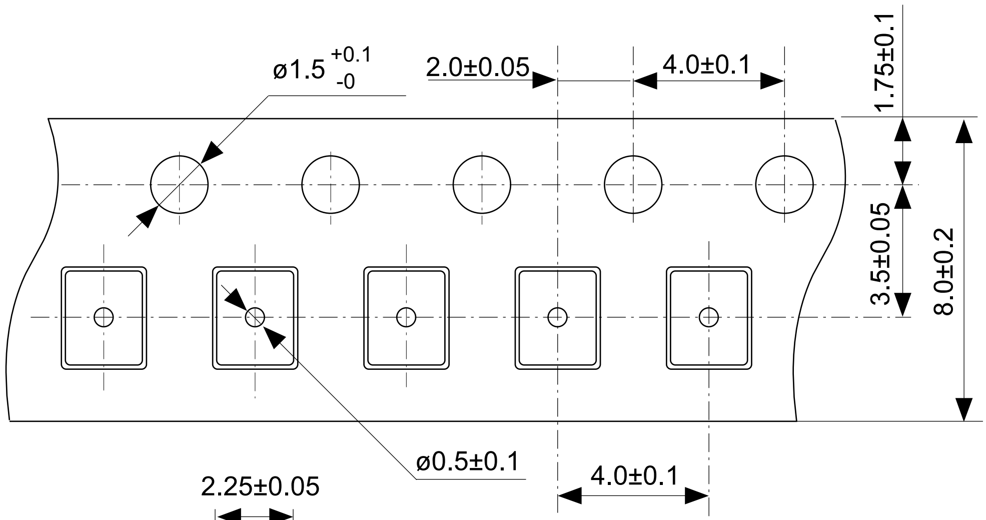

0.08 +0.05 -0.02
0.48±0.02

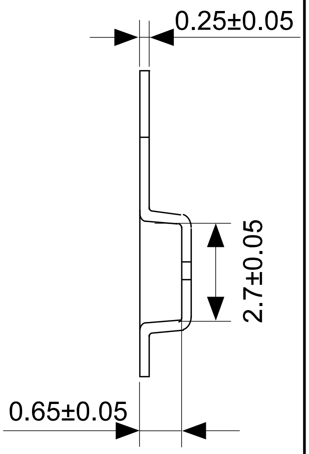


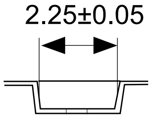


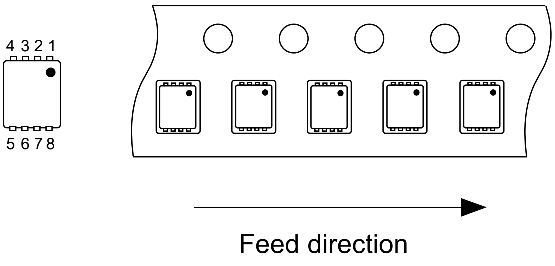
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	


ø1.5 +0.1 -0
2.0±0.05
4.0±0.1
1.75±0.1
3.5±0.05
8.0±0.2
ø0.5±0.1
4.0±0.1


0.25±0.05
2.7±0.05
0.65±0.05

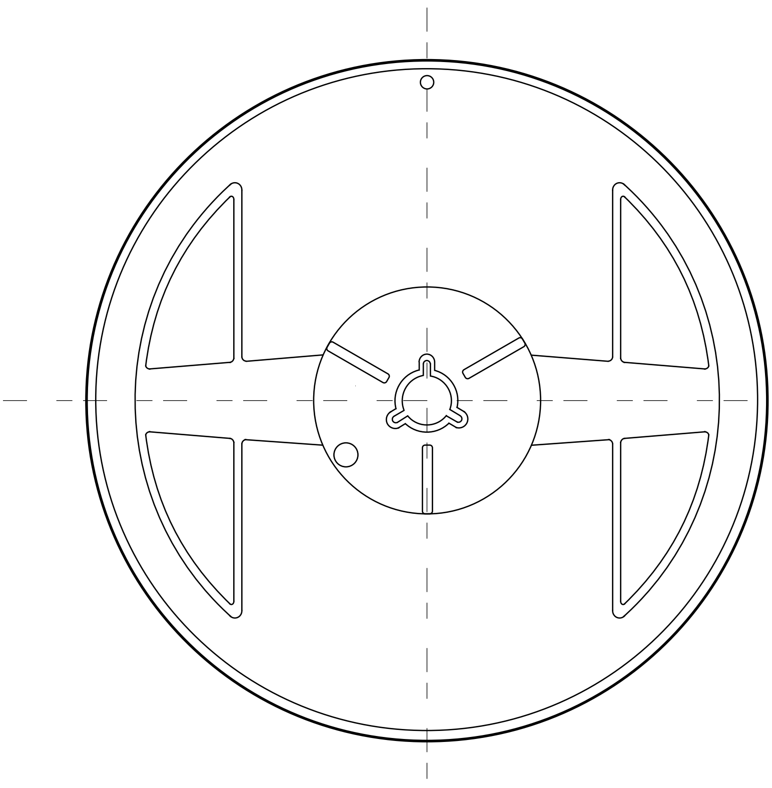


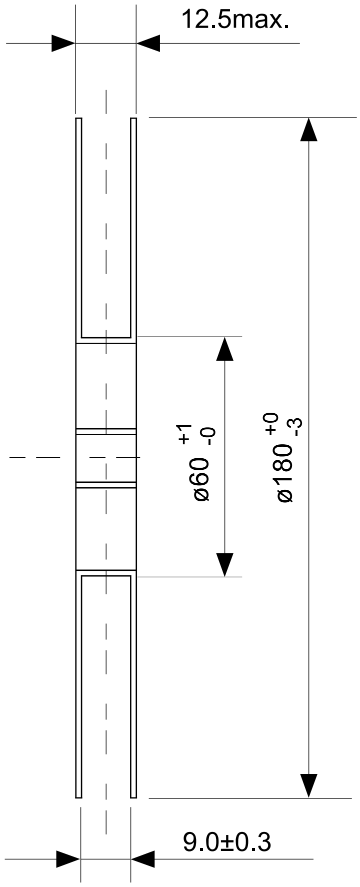

4 3 2 1
5 6 7 8
Feed direction

No. PH008-A-C-SD-2.0

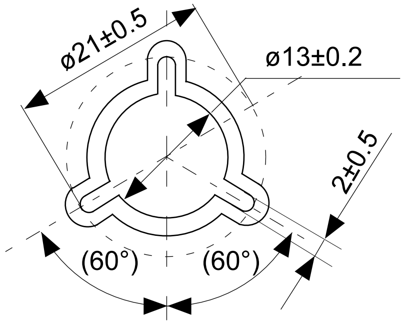
TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



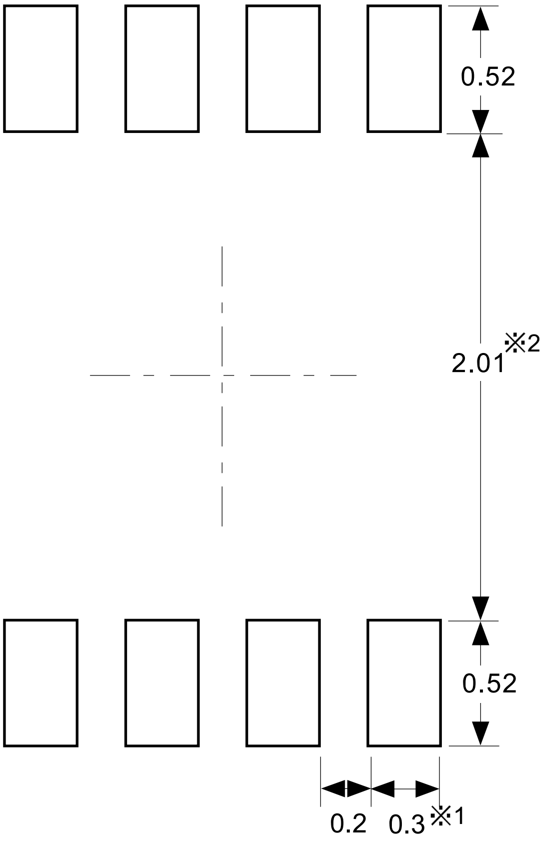

12.5max.
ø60 +1 -0
ø180 +0 -3
9.0±0.3

Enlarged drawing in the central part


ø21±0.5
ø13±0.2
2±0.5
(60°)
(60°)

No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意　1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution　1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度（从焊盘模式表面起）请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm

ABLIC Inc.

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07