S1D13513 Display Controller

August 2007

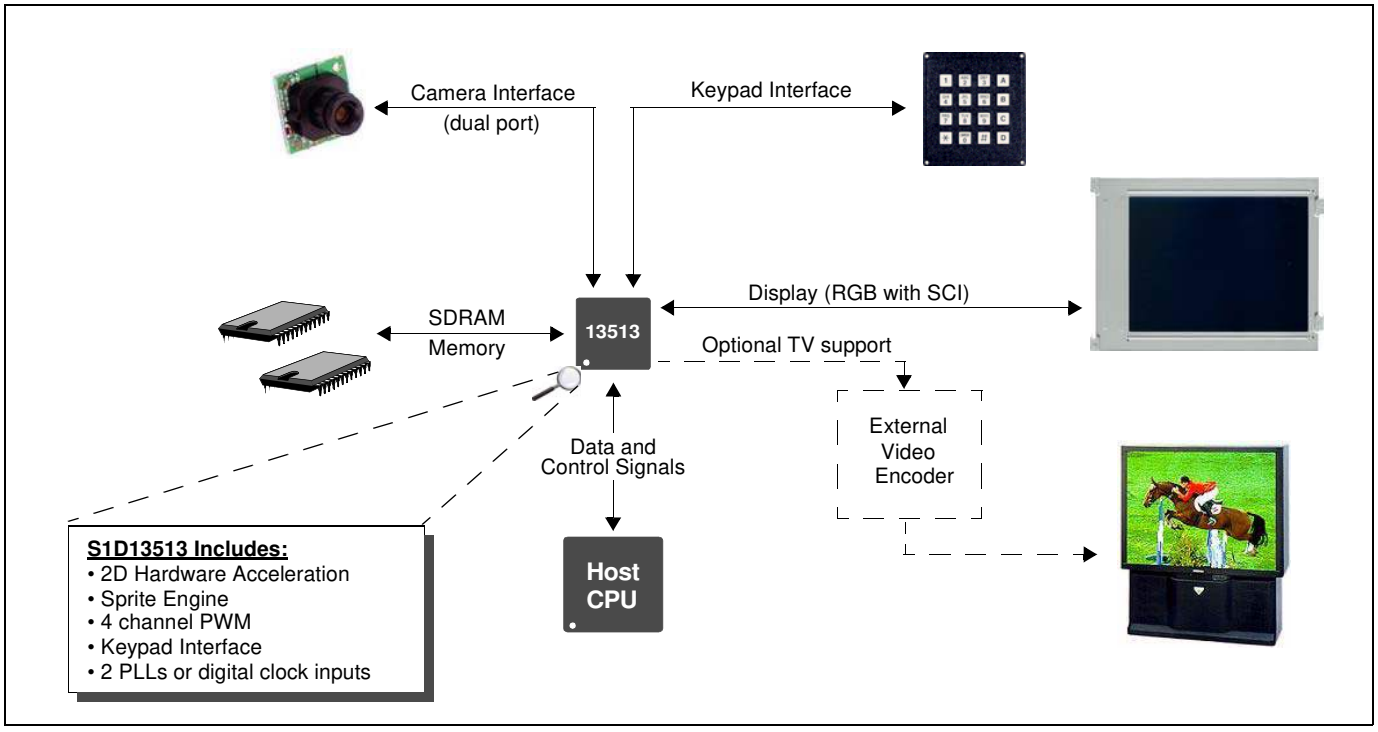
The S1D13513 is a highly integrated Display Controller capable of outputting to LCD or TV. With the flexibility of an external SDRAM memory interface, this low cost, low power, device supports a wide range of CPUs, panels, and a camera port that can be configured as 2x 8-bit ports. The S1D13513 feature set and architecture are designed to meet the requirements of embedded systems such as Mobile Communications, Hand-Held PC's, Office Automation, and Automotive applications.

The S1D13513 features both Sprite and 2D BitBLT engines designed to reduce the load on the Host, while increasing the performance of graphics intensive operations. Additionally, the S1D13513 offers such features as multiple windows, alpha blending, gamma correction, and mirror/rotation function which allow user configurability of various images on the Main/PIP1/PIP2 displays. While focusing on devices targeted by the Microsoft Windows CE Operating System, the S1D13513's impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

■ FEATURES

- Direct and Indirect CPU interfaces
- Serial Host Interface
- Memory interface for x16 or x32 external SDRAM (x32 available on S1D13513 PBGA only)
- Programmable resolutions and color depths
- Support for single RGB panel with serial command interface
- YUV DIgital Output (YUV 4:2:2) which supports NTSC/PAL TV output via an external video encoder
- Clocks can be selected from two embedded PLLs or digital clock inputs
- Two built-in Crystal inputs
- Dual port Camera interface with resize function
- Sprite Engine
- 2D Hardware Acceleration Engine
- Overlay features
- Multiple Windows (Layers) with Alpha Blending
- Gamma Correction
- 4 Channel PWM for Backlight control
- Keypad Interface with 5x5 matrix support
- Software initiated Power Save Mode
- Low Operating Voltage
- Package: PBGA 256-pin and QFP 208-pin (QFP does not support all features)

■ SYSTEM BLOCK DIAGRAM



■ DESCRIPTION

External Display Buffer

- Uses external SDRAM or mobile SDRAM as display buffer
- Supports x16 / x32 SDRAM interface (Size: 8M byte, 16M byte, 32Mbyte or 64Mbyte) (x32 and 32/64Mbyte not supported for QFP package)
- SDRAM clock: 100MHz Maximum
- Automatic re-entry into self refresh mode
- Provides linear access to first 1M bytes and four configurable 256KB windows into the remaining memory

Display Support

- RGB Interface single panel
  - 16/18/24-bit Color TFT (24-bit not supported for QFP)
  - Optional serial command interface
- 8-bit Monochrome passive panel
- 8-bit Color Type 2 passive panel
- YUV Digital Output (YUV 4:2:2) which supports NTSC/PAL TV Output via an external Video Encoder
- Color Depths up to 32 bpp
- Example resolutions
  1024x768 at a color depth of 16 bpp (x32 SDRAM only)
  800x600 at a color depth of 16 bpp (x32 SDRAM only)
  640x480 at a color depth of 32 bpp (x32 SDRAM only)

Display Features

- Multiple window (layer) support
- Mirror and 180° rotation functions
- Double Buffering support
- Alpha Blending
- Gamma Correction
- Pseudo Color Expansion
- Hardware cursor support via the Sprite engine
- Camera image can be displayed on the PIP1/PIP2 window
- Interrupts available
  - Supports maskable non-display (Vsync) interrupt
  - Supports delayed version of Vsync Interrupt

CPU Interface

- Direct and indirect interface support for most popular CPU interfaces
- Serial Host Interface
- Supports 20-50MHz Host bus clock
- Registers are memory-mapped - M/R# input selects between memory and register address space

Digital Video

- Dual Camera / Video Input port can be configured as 2x 8-bit camera ports
  - Supports ITU-R BT656 (CCIR-656) YUV format
  - Supports resize function of the video in stream
  - Supports raw JPEG capture from JPEG capable camera
- Captures YUV data into SDRAM as YUV 4:2:2 format
- View Image can be displayed to LCD or TV
- Resize function built-in for both View and Capture path

Acceleration

- 2D BitBLT Engine (Read, Write, Move, and Fill BLTs)
- 2D Sprite Engine (up to 16 sprites)
- Unified Command FIFO for both BitBLT and Sprite

Miscellaneous

- Internal system clock: 50MHz maximum (half of SDRAM clock)
- 4 channel PWM for backlight control
- I2C Interface (typically used for camera)
- Keypad Interface with 5 x 5 matrix support
- Software initiated power save mode
- Multiple General Purpose IO pins
- Flexible clock structure:
  - Two embedded PLLs
  - Two built-in crystal inputs
  - Four digital clock inputs
  - Clocks dynamically turned off when modules are not needed
- $CORE_{VDD}$ 1.8 volts and IO_{VDD} 3.3 volts
- Package: PBGA 256-pin and QFP 208-pin

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13513 Technical Documentation
- CPU Independent Software Utilities
- S1D13513 Evaluation Boards
- Royalty Free source level driver code

Japan
Seiko Epson Corporation
IC International Sales Group
421-8, Hino, Hino-shi
Tokyo 191-8501, Japan
Tel: 042-587-5812
Fax: 042-587-5564
http://www.epson.co.jp/

North America
Epson Electronics America, Inc.
2580 Orchard Parkway
San Jose, CA 95131, USA
Tel: (408) 922-0200
Fax: (408) 922-0238
http://www.eea.epson.com/

Taiwan
Epson Taiwan Technology & Trading Ltd.
14F, No. 7
Song Ren Road
Taipei 110
Tel: 02-8786-6688
Fax: 02-8786-6677
http://www.epson.com.tw/

Hong Kong
Epson Hong Kong Ltd.
20/F., Harbour Centre
25 Harbour Road
Wanchai, Hong Kong
Tel: 2585-4600
Fax: 2827-4346
http://www.epson.com.hk/

Europe
Epson Europe Electronics GmbH
Riesstrasse 15
80992 Munich, Germany
Tel: 089-14005-0
Fax: 089-14005-110
http://www.epson-electronics.de/

Singapore
Epson Singapore Pte Ltd
1 HarbourFront Place #03-02
HarbourFront Tower One
Singapore, 098633
Tel: (65) 6586-5500
Fax: (65) 6271-3182
http://www.epson.com.sg/