# SN74LV4051A-Q1 8-Channel Analog Multiplexer/Demultiplexer

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 2-V to 5.5-V $V_{CC}$ Operation
- Supports Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

## 2 Applications

- Automotive Infotainment and Cluster
- Telematics, eCall

## 3 Description

This 8-channel CMOS analog multiplexer and demultiplexer is designed for 2-V to 5.5-V $V_{CC}$ operation.

The SN74LV4051A handles analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

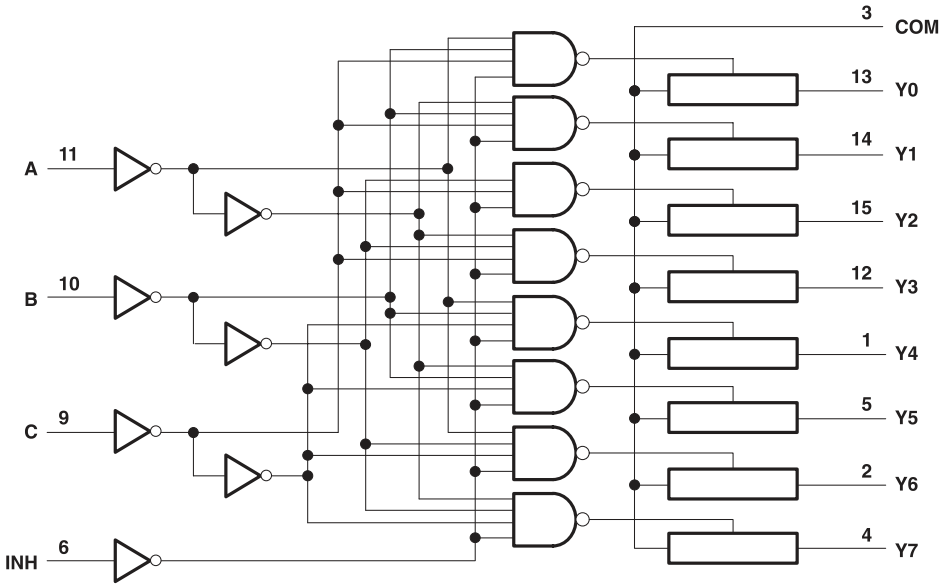
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LV4051A-Q1 | TSSOP (16) | 5.00 mm × 4.40 mm |
| | SOIC (16) | 10.30 mm × 7.50 mm |
| | | 9.90 mm × 3.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**



# Table of Contents

**1 Features** ... 1
**2 Applications** ... 1
**3 Description** ... 1
**4 Revision History** ... 2
**5 Pin Configuration and Functions** ... 3
**6 Specifications** ... 5
6.1 Absolute Maximum Ratings ... 5
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 6
6.6 Switching Characteristics $V_{CC}$ = 3.3 V ± 0.3 V ... 7
6.7 Switching Characteristics $V_{CC}$ = 5 V ± 0.5 V ... 7
6.8 Analog Switch Characteristics ... 7
6.9 Operating Characteristics ... 7
**7 Parameter Measurement Information** ... 8
**8 Detailed Description** ... 11
8.1 Overview ... 11
8.2 Functional Block Diagram ... 11
8.3 Feature Description ... 11
8.4 Device Functional Modes ... 11
**9 Application and Implementation** ... 12
9.1 Application Information ... 12
9.2 Typical Application ... 12
**10 Power Supply Recommendations** ... 13
**11 Layout** ... 13
11.1 Layout Guidelines ... 13
11.2 Layout Example ... 13
**12 Device and Documentation Support** ... 14
12.1 Trademarks ... 14
12.2 Electrostatic Discharge Caution ... 14
12.3 Glossary ... 14
**13 Mechanical, Packaging, and Orderable Information** ... 14

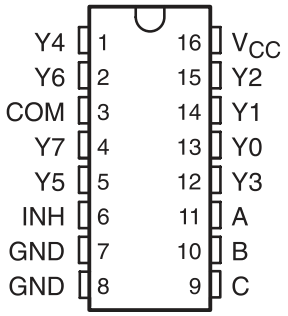
## 4 Revision History

**Changes from Revision D (June 2011) to Revision E** **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 5

# 5 Pin Configuration and Functions

**D, DW, or PW Package**
**16 Pins**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| Y4 | 1 | I(1) | Input to mux |
| Y6 | 2 | I(1) | Input to mux |
| COM | 3 | O(1) | Output of mux |
| Y7 | 4 | I(1) | Input to mux |
| Y5 | 5 | I(1) | Input to mux |
| INH | 6 | I(1) | Enables the outputs of the device. Logic low level with turn the outputs on, high level will turn them off. |
| GND | 7 | — | Ground |
| GND | 8 | — | Ground |
| C | 9 | I | Selector line for outputs (see *Device Functional Modes* for specific information) |
| B | 10 | I | Selector line for outputs (see *Device Functional Modes* for specific information) |
| A | 11 | I | Selector line for outputs (see *Device Functional Modes* for specific information) |
| Y3 | 12 | I(1) | Input to mux |
| Y0 | 13 | I(1) | Input to mux |
| Y1 | 14 | I(1) | Input to mux |
| Y2 | 15 | I(1) | Input to mux |
| Vcc | 16 | I | Device power input |

(1) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins Y0-Y7 may be considered outputs (O) and the COM pin may be considered inputs (I).

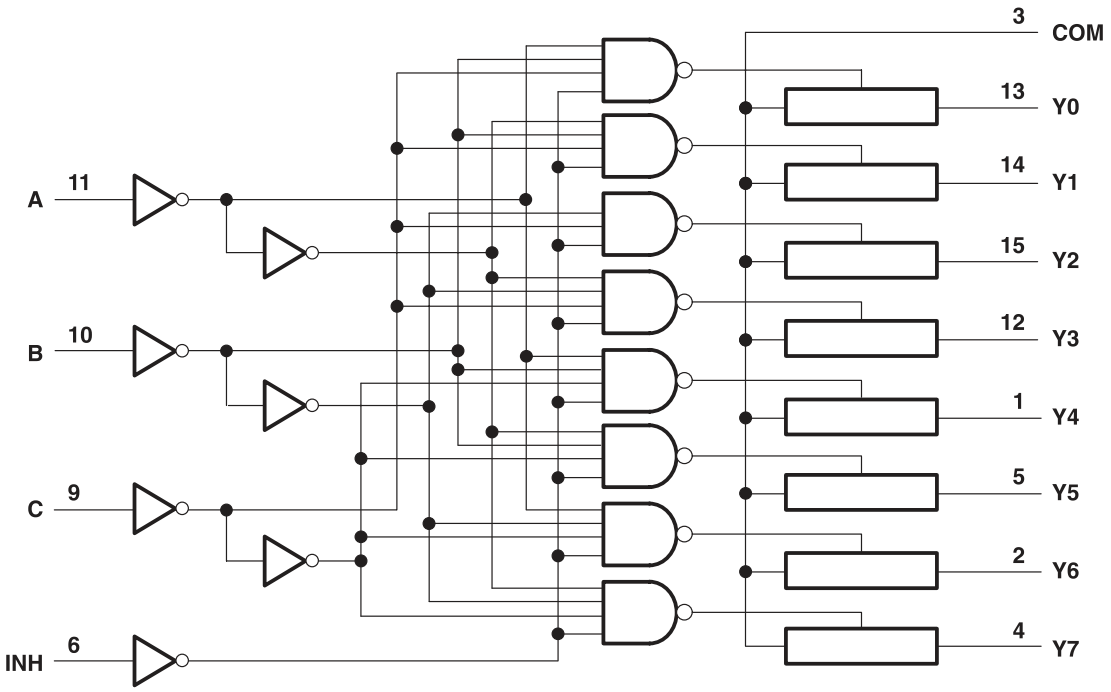



**Figure 1. Logic Diagram (Positive Logic)**

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 V | V |
| $V_I$ | Input voltage(2) | | –0.5 | 7 V | |
| $V_{IO}$ | Switch I/O voltage(2) (3) | | –0.5 | $V_{CC}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | –20 | | mA |
| $I_{IOK}$ | I/O diode current | $V_{IO} < 0$ | –50 | | |
| $I_T$ | Switch through current | $V_{IO}$ = 0 to $V_{CC}$ | –25 | 25 | |
| | Continuous current through $V_{CC}$ or GND | | –50 | 50 | |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5 V maximum.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins (1, 8, 9, and 16) | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

See(1)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2(2) | | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | $V_{CC}$ × 0.3 | |
| $V_I$ | Control input voltage | | 0 | | 5.5 | V |
| $V_{IO}$ | Input/output voltage | | 0 | | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | 20 | |
| $T_A$ | Operating free-air temperature | SN74LV4051ATDRQ1,SN74LV4051ATDWRQ1 SN74LV4051ATPWRQ1 | –40 | | 105 | °C |
| $T_A$ | Operating free-air temperature | SN74LV4051AQPWRQ1 | –40 | | 125 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | SN74LV4051A-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | DW | PW | D | |
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 85.1 | 92.4 | 113.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 47.2 | 52.9 | 48.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.8 | 49.5 | 58.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 17.8 | 15.5 | 6.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 49.3 | 49.2 | 57.8 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = -40 to 105°C | | | $T_A$ = -40 to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $r_{on}$ | On-state switch resistance | $I_T$ = 2 mA, $V_I$ = $V_{CC}$ or GND, $V_{INH}$ = $V_{IL}$ (see Figure 2) | 2.3 V | | 38 | 180 | | | 225 | | | 225 | Ω |
| | | | 3 V | | 30 | 150 | | | 190 | | | 190 | |
| | | | 4.5 V | | 22 | 75 | | | 100 | | | 100 | |
| $r_{on(p)}$ | Peak on-state resistance | $I_T$ = 2 mA, $V_I$ = $V_{CC}$ or GND, $V_{INH}$ = $V_{IL}$ | 2.3 V | | 113 | 500 | | | 600 | | | 600 | Ω |
| | | | 3 V | | 54 | 180 | | | 225 | | | 225 | |
| | | | 4.5 V | | 31 | 100 | | | 125 | | | 125 | |
| $\Delta r_{on}$ | Difference in on-state resistance between switch | $I_T$ = 2 mA, $V_I$ = $V_{CC}$ or GND, $V_{INH}$ = $V_{IL}$ | 2.3 V | | 2.1 | 30 | | | 40 | | | 40 | Ω |
| | | | 3 V | | 1.4 | 20 | | | 30 | | | 30 | |
| | | | 4.5 V | | 1.3 | 15 | | | 20 | | | 20 | |
| $I_I$ | Control input current | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | | ±1 | | | ±2 | μA |
| $I_{S(off)}$ | Off-state switch leakage current | $V_I$ = $V_{CC}$ and $V_O$ = GND, or $V_I$ = GND and $V_O$ = $V_{CC}$, $V_{INH}$ = $V_{IH}$ (see Figure 3) | 5.5 V | | | ±0.1 | | | ±1 | | | ±2 | μA |
| $I_{S(on)}$ | On-state switch leakage current | $V_I$ = $V_{CC}$ or GND, $V_{INH}$ = $V_{IL}$ (see Figure 4) | 5.5 V | | | ±0.1 | | | ±1 | | | ±2 | μA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | | | | 20 | | | 40 | μA |
| $C_{IC}$ | Control input capacitance | f = 10 MHz | 3.3 V | | 2 | | | | | | | | pF |
| $C_{IS}$ | Common terminal capacitance | | 3.3 V | | 23.4 | | | | | | | | pF |
| $C_{OS}$ | Switch terminal capacitance | | 3.3 V | | 5.7 | | | | | | | | pF |
| $C_F$ | Feedthrough capacitance | | | | 0.5 | | | | | | | | pF |

## 6.6 Switching Characteristics $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | $T_A$ = -40 to 105°C | | $T_A$ = -40 to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 50 pF (see Figure 5) | | 2.5 | 9 | | 12 | | 14 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 50 pF (see Figure 6) | | 5.5 | 20 | | 25 | | 25 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 50 pF (see Figure 6) | | 8.8 | 20 | | 25 | | 25 | ns |

## 6.7 Switching Characteristics $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | $T_A$ = -40 to 105°C | | | $T_A$ = -40 to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ $t_{PHL}$ | Propagation delay time | COM or Yn | Yn or COM | $C_L$ = 50 pF (see Figure 5) | | 1.5 | 6 | | | 8 | | | 10 | ns |
| $t_{PZH}$ $t_{PZL}$ | Enable delay time | INH | COM or Yn | $C_L$ = 50 pF (see Figure 6) | | 4 | 14 | | | 18 | | | 18 | ns |
| $t_{PHZ}$ $t_{PLZ}$ | Disable delay time | INH | COM or Yn | $C_L$ = 50 pF (see Figure 6) | | 6.2 | 14 | | | 18 | | | 18 | ns |

## 6.8 Analog Switch Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | |
| Frequency response (switch on) | COM or Yn | Yn or COM | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (sine wave)(1) (see Figure 7) | | 2.3 V | | 20 | | MHz |
| | | | | | 3 V | | 25 | | |
| | | | | | 4.5 V | | 35 | | |
| Crosstalk (control input to signal output) | INH | COM or Yn | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz (square wave) (seeFigure 8 ) | | 2.3 V | | 20 | | mV |
| | | | | | 3 V | | 35 | | |
| | | | | | 4.5 V | | 60 | | |
| Feedthrough attenuation (switch off) | COM or Yn | Yn or COM | $C_L$ = 50 pF, $R_L$ = 600 Ω, $f_{in}$ = 1 MHz(2) (see Figure 9) | | 2.3 V | | –45 | | dB |
| | | | | | 3 V | | –45 | | |
| | | | | | 4.5 V | | –45 | | |
| Sine-wave distortion | COM or Yn | Yn or COM | $C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 1 kkHz (sine wave) (see Figure 10) | $V_I$ = 2 Vp-p | 2.3 V | | 0.1% | | |
| | | | | $V_I$ = 2.5 Vp-p | 3 V | | 0.1% | | |
| | | | | $V_I$ = 4 Vp-p | 4.5 V | | 0.1% | | |

(1) Adjust $f_{in}$ voltage to obtain 0-dBm output. Increase fin frequency until dB meter reads −3 dB.
(2) Adjust $f_{in}$ voltage to obtain 0-dBm input.

## 6.9 Operating Characteristics

$V_{CC}$ = 3.3 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, f = 10 MHz | 5.9 | pF |

# 7 Parameter Measurement Information

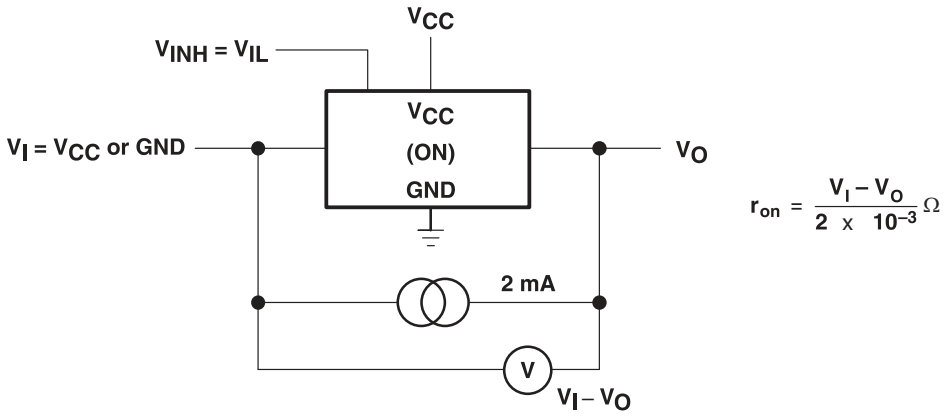
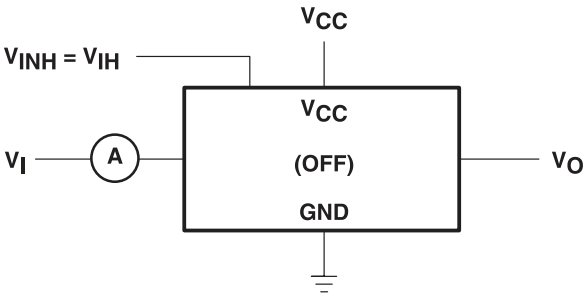



**Figure 2. On-State Resistance Test Circuit**




Condition 1: $V_I$ = 0, $V_O$ = $V_{CC}$
Condition 2: $V_I$ = $V_{CC}$, $V_O$ = 0

**Figure 3. Off-State Switch Leakage-Current Test Circuit**

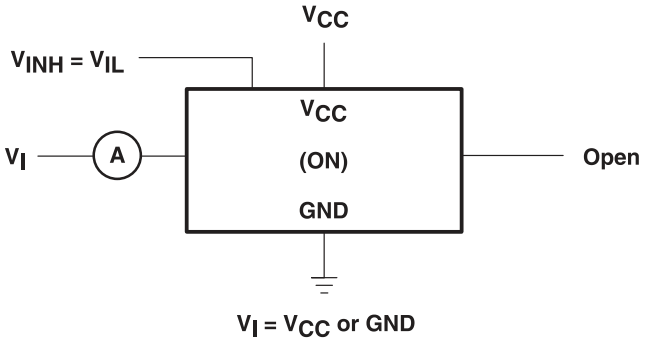



**Figure 4. On-State Switch Leakage-Current Test Circuit**

## Parameter Measurement Information (continued)

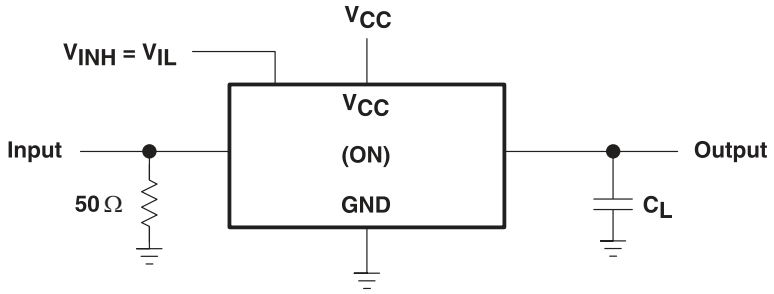
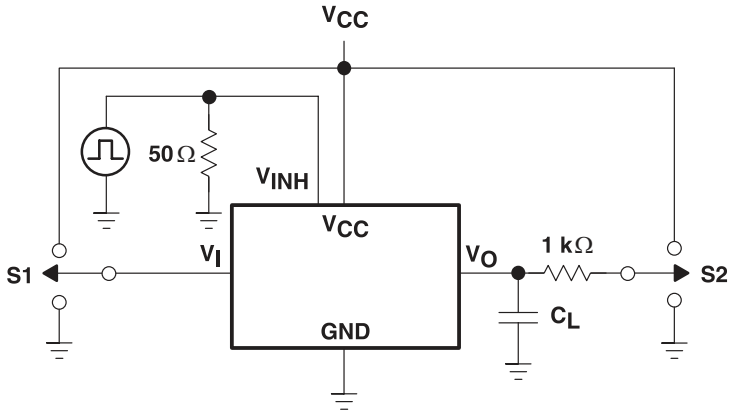
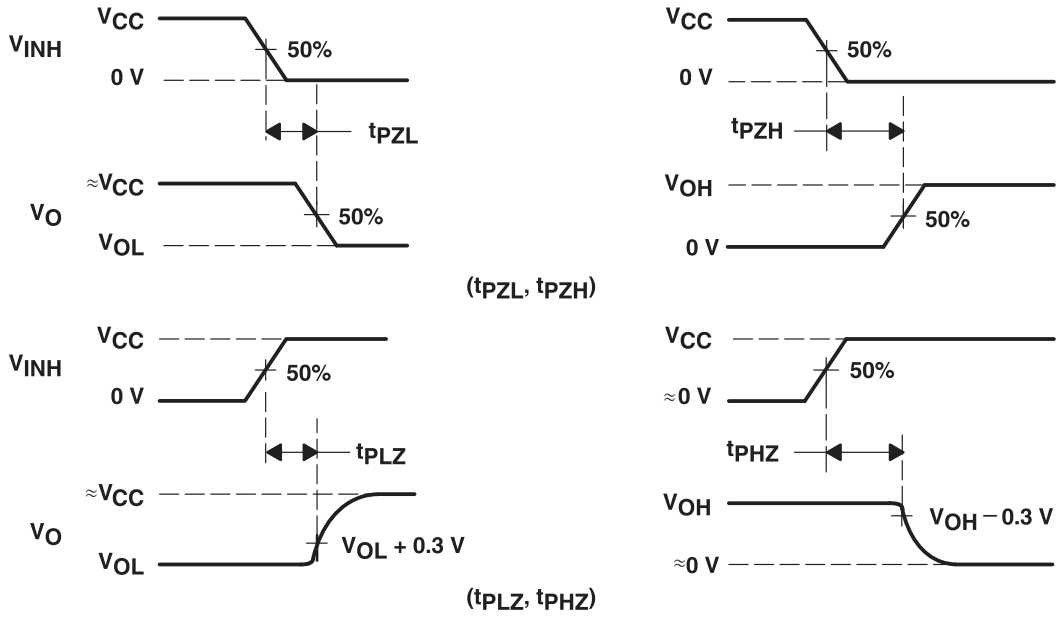



**Figure 5. Propagation Delay Time, Signal Input to Signal Output**




| TEST | S1 | S2 |
|---|---|---|
| $t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | GND<br>$V_{CC}$ | $V_{CC}$<br>GND |

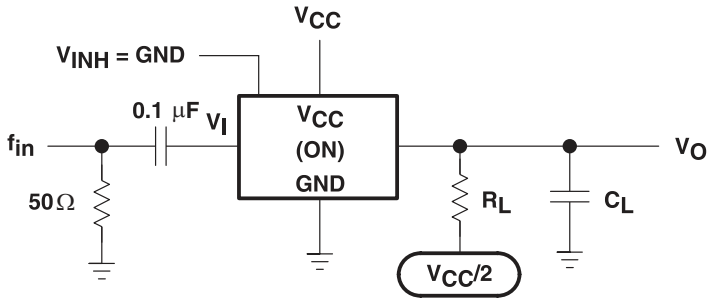
TEST CIRCUIT




VOLTAGE WAVEFORMS

**Figure 6. Switching Time ($t_{PZL}$, $t_{PLZ}$, $t_{PZH}$, $t_{PHZ}$), Control to Signal Output**

## Parameter Measurement Information (continued)




NOTE A: $f_{in}$ is a sine wave.

**Figure 7. Frequency Response (Switch On)**

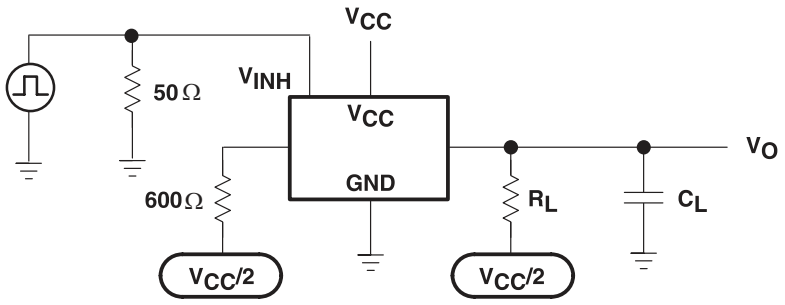



**Figure 8. Crosstalk (Control Input, Switch Output)**

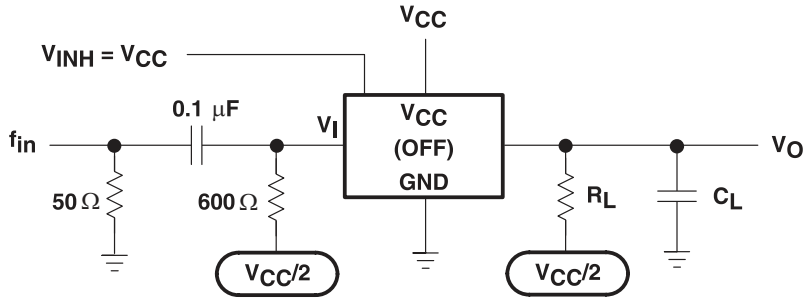



**Figure 9. Feedthrough Attenuation (Switch Off)**

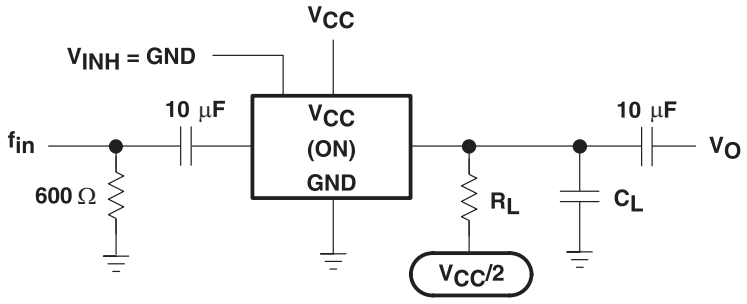


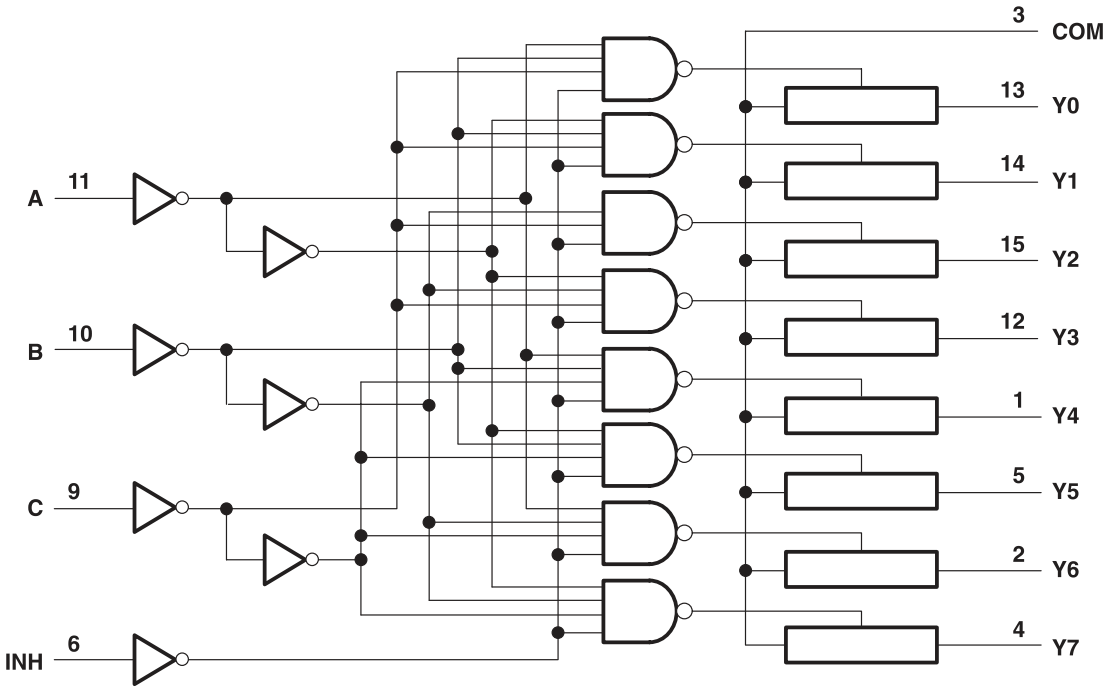

**Figure 10. Sine-Wave Distortion**

# 8 Detailed Description

## 8.1 Overview

This device is an 8-channel analog multiplexer. A multiplexer is used when several signals must share the same device or resource. This device allows the selection of one of these signals at a time, for analysis or propagation.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

This device contains one 8-channel multiplexer for use in a variety of applications, and can also be configured as demultiplexer by using the COM pin as an input and the Yx pins as outputs. This device is qualified for automotive applications and has an extended temperature range of –40°C to 125°C (maximum depends on package type).

## 8.4 Device Functional Modes

**Table 1. Function Table**

| INPUTS | | | | ON CHANNEL |
|---|---|---|---|---|
| INH | C | B | A | |
| L | L | L | L | Y0 |
| L | L | L | H | Y1 |
| L | L | H | L | Y2 |
| L | L | H | H | Y3 |
| L | H | L | L | Y4 |
| L | H | L | H | Y5 |
| L | H | H | L | Y6 |
| L | H | H | H | Y7 |
| H | X | X | X | None |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In the example below, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller unit (MCU).

## 9.2 Typical Application

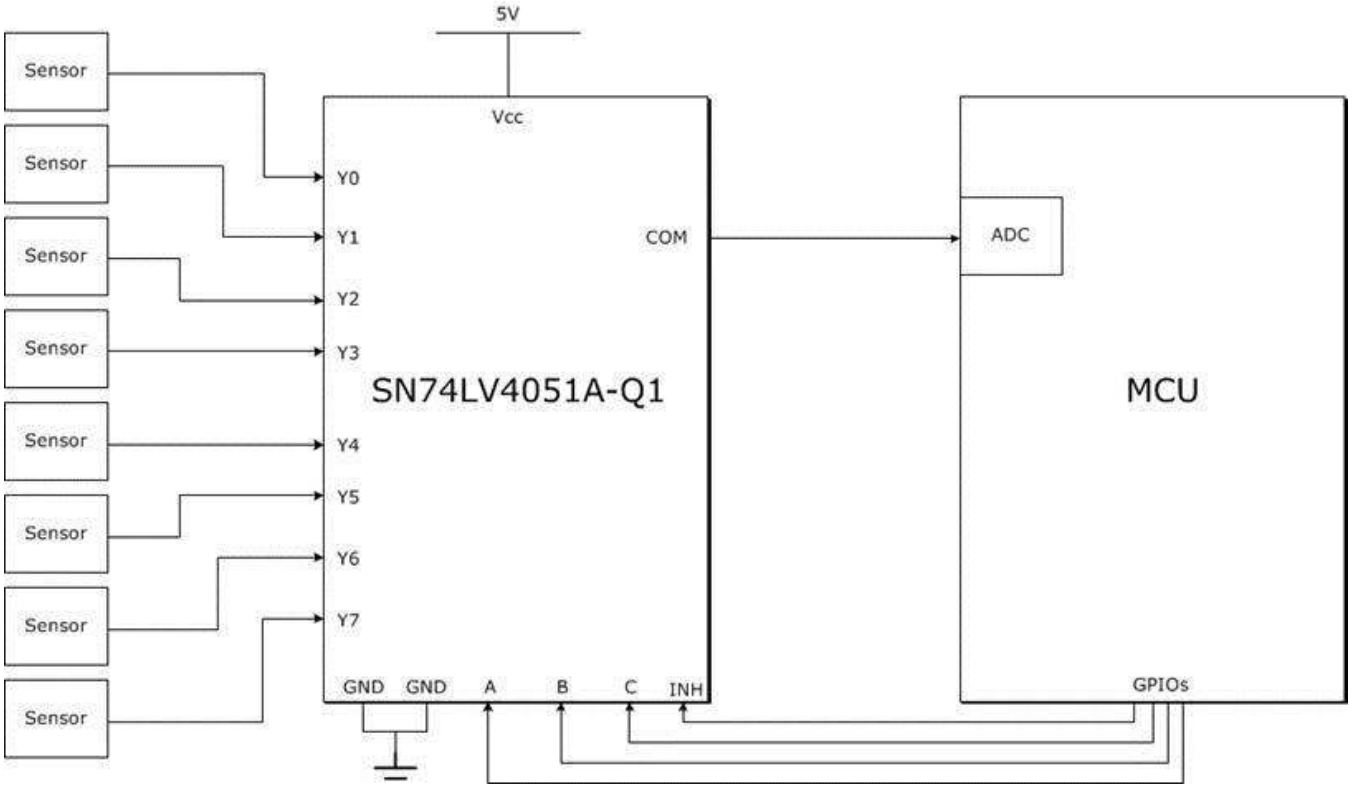



**Figure 11. Example of Multiplexer Use With Analog Sensors and the ADC of an MCU**

### 9.2.1 Design Requirements

Designing with the SN74LV4051A-Q1 device requires a stable input voltage between 2 V (see *Recommended Operating Conditions* for details) and 5.5 V. Another important design consideration is the characteristics of the signal being multiplexed, to ensure no important information is lost due to timing or incompatibility with this device.

### 9.2.2 Detailed Design Procedure

Normally, processing eight different analog signals would require eight separate ADCs, but Figure 11 shows how to achieve this using only one ADC and four GPIOs (general-purpose input/outputs).

# 10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the Vcc pin of this device. If this is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher voltage rail.

# 11 Layout

## 11.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are more than 1 inch long. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω,as required by the application. Do not place this device too close to high-voltage switching components, as they may cause interference.

## 11.2 Layout Example

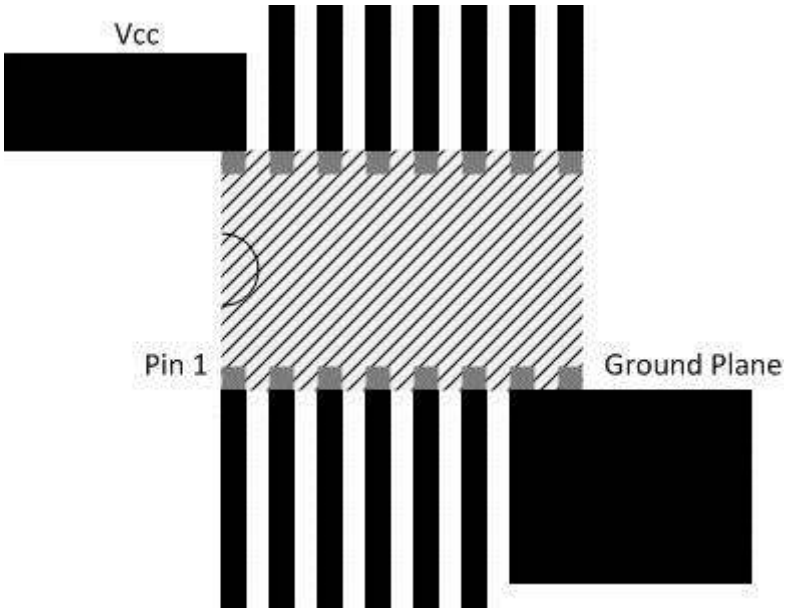



**Figure 12. Layout Schematic**

# 12 Device and Documentation Support

## 12.1 Trademarks

All trademarks are the property of their respective owners.

## 12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CLV4051ATDWRG4Q1 | LIFEBUY | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051AQ | |
| CLV4051ATPWRG4Q1 | LIFEBUY | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051AQ | |
| SN74LV4051AQPWRQ1 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4051AQ1 | Samples |
| SN74LV4051ATDRQ1 | LIFEBUY | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051AQ | |
| SN74LV4051ATDWRQ1 | LIFEBUY | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051AQ | |
| SN74LV4051ATPWRQ1 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | L4051AQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV4051A-Q1 :**

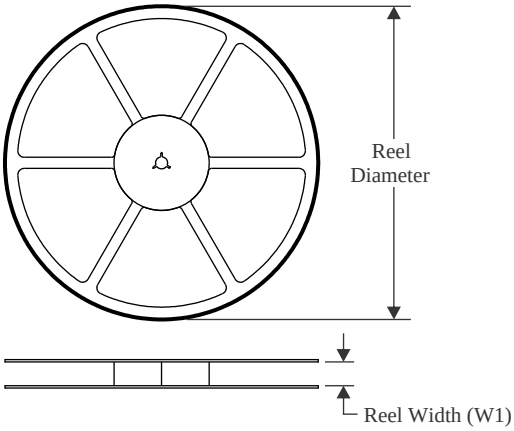
- Catalog : SN74LV4051A
- Enhanced Product : SN74LV4051A-EP

NOTE: Qualified Version Definitions:

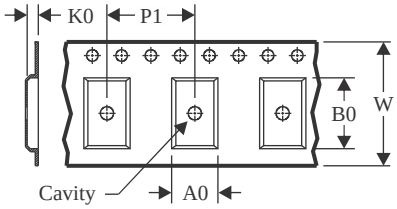
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

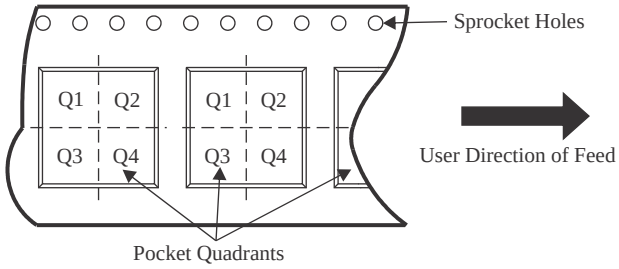



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

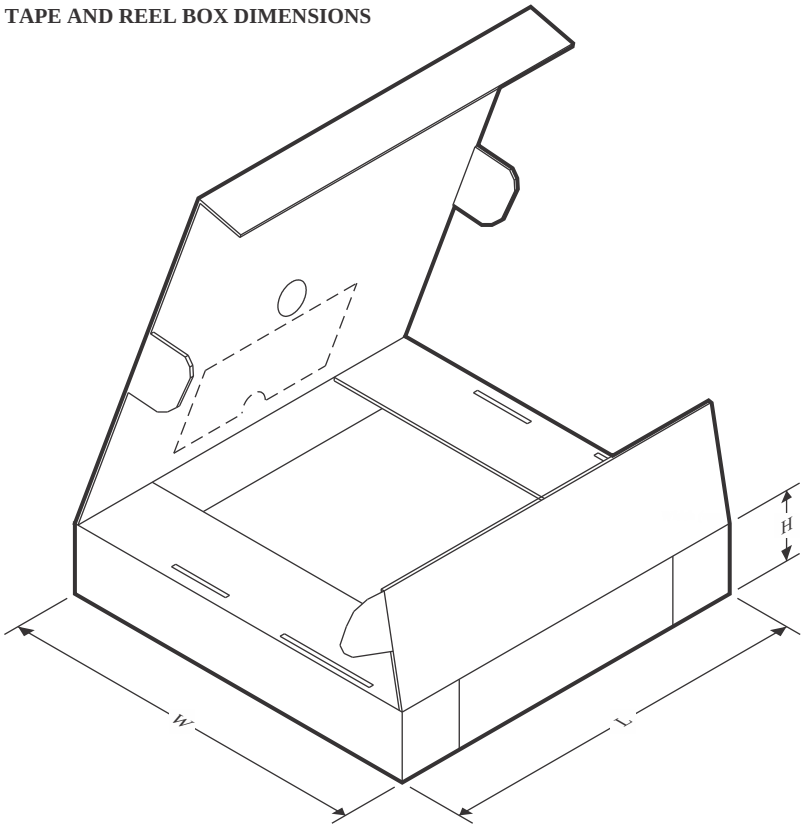
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CLV4051ATDWRG4Q1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| CLV4051ATPWRG4Q1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4051AQPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV4051ATDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| SN74LV4051ATPWRQ1 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

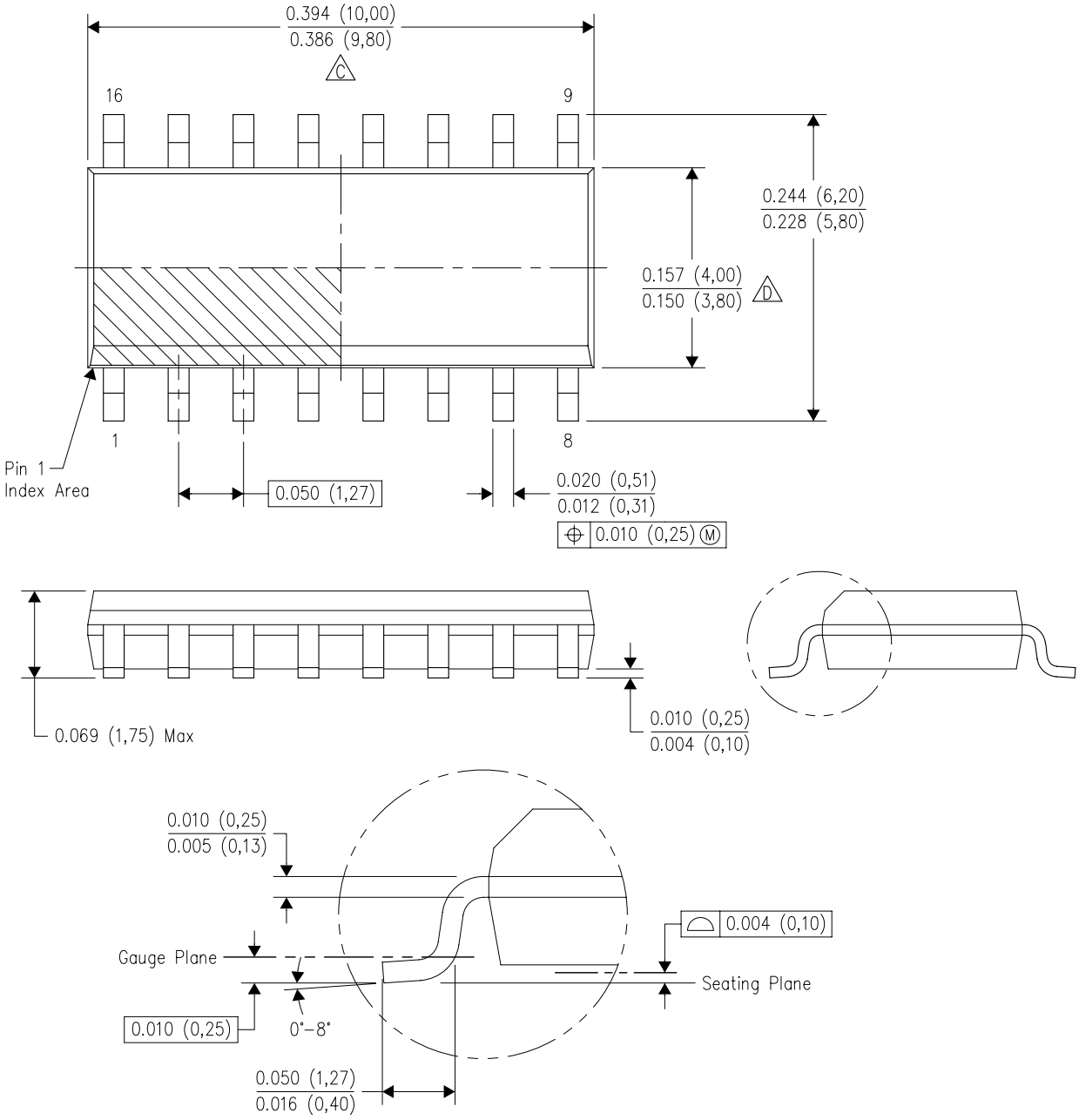
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CLV4051ATDWRG4Q1 | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| CLV4051ATPWRG4Q1 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV4051AQPWRQ1 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV4051ATDWRQ1 | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74LV4051ATPWRQ1 | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

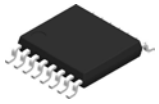
D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

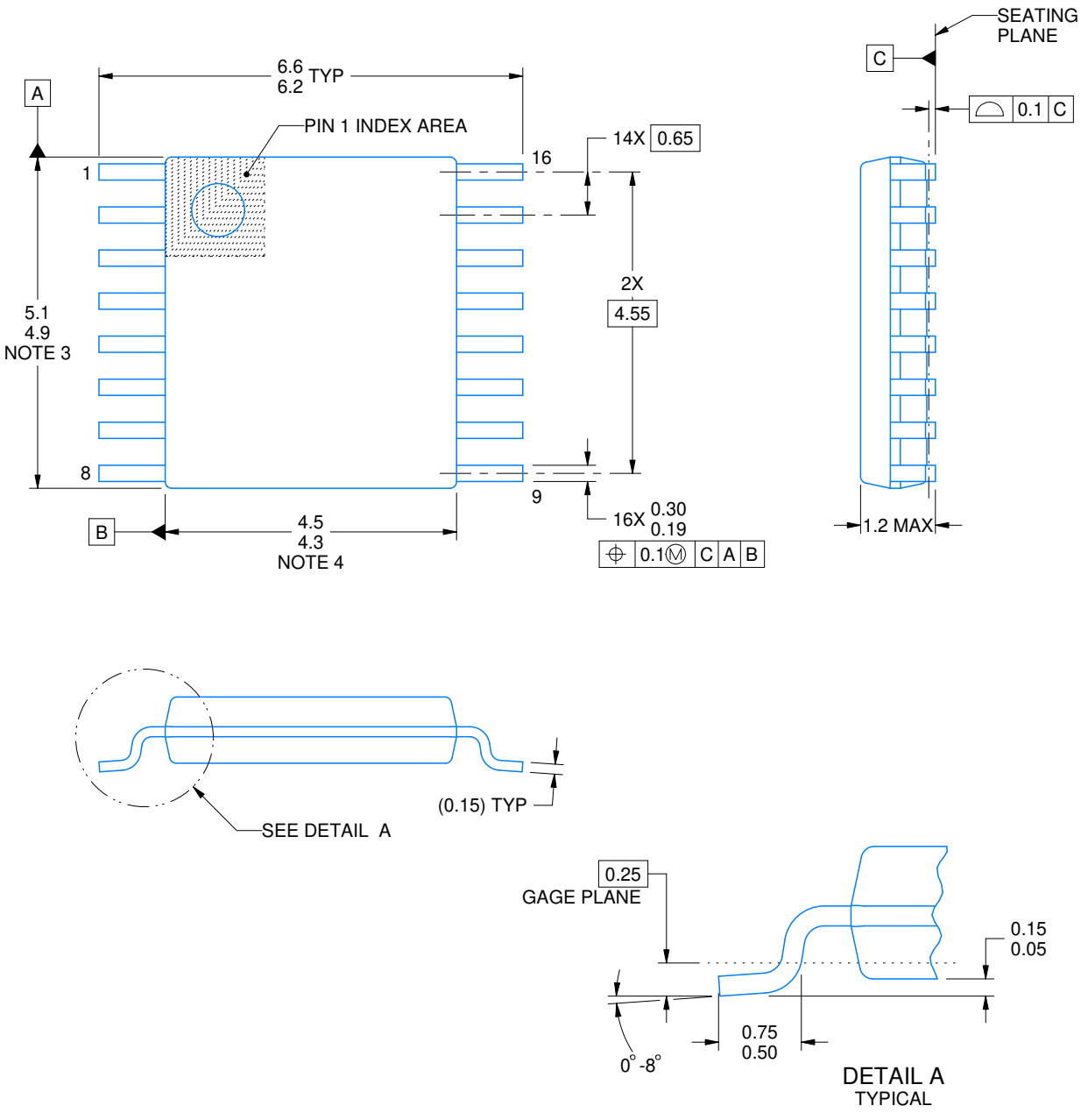
# PACKAGE OUTLINE

## PW0016A



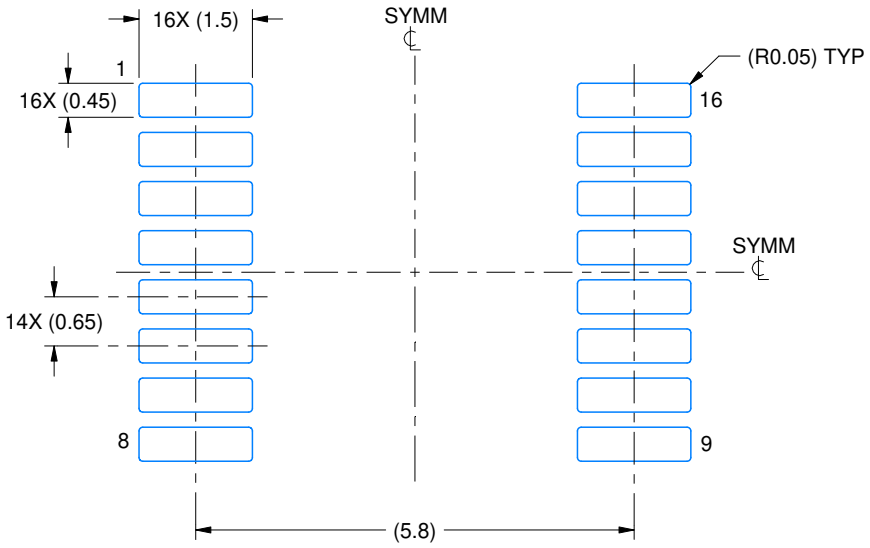
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

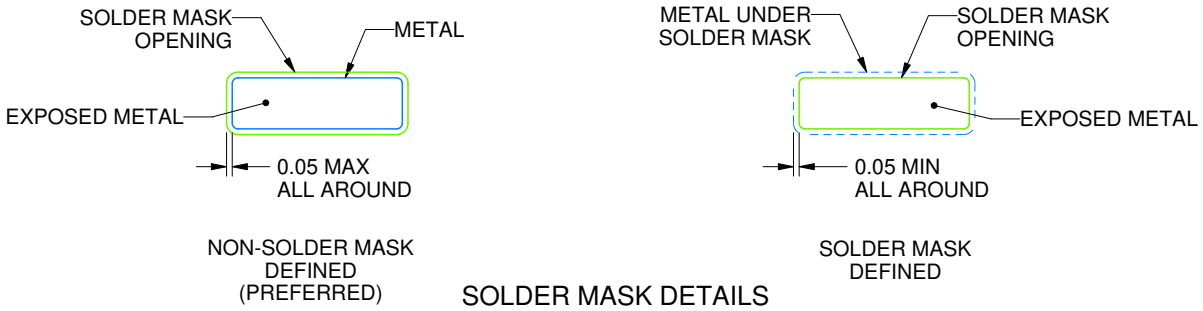



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

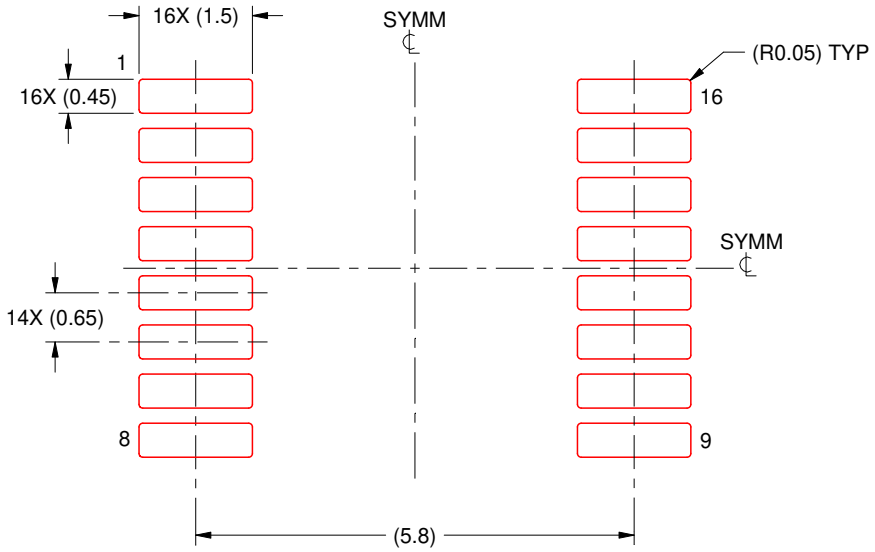



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

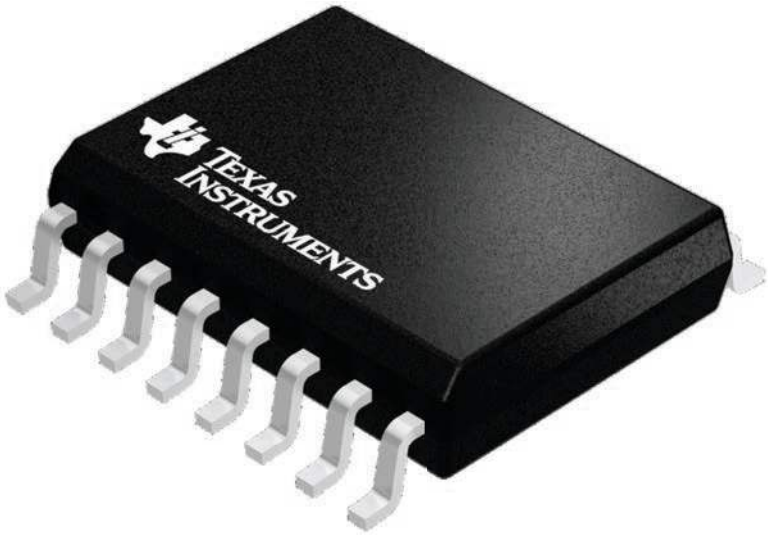
## DW 16

## SOIC - 2.65 mm max height

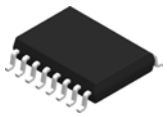
**7.5 x 10.3, 1.27 mm pitch**

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224780/A

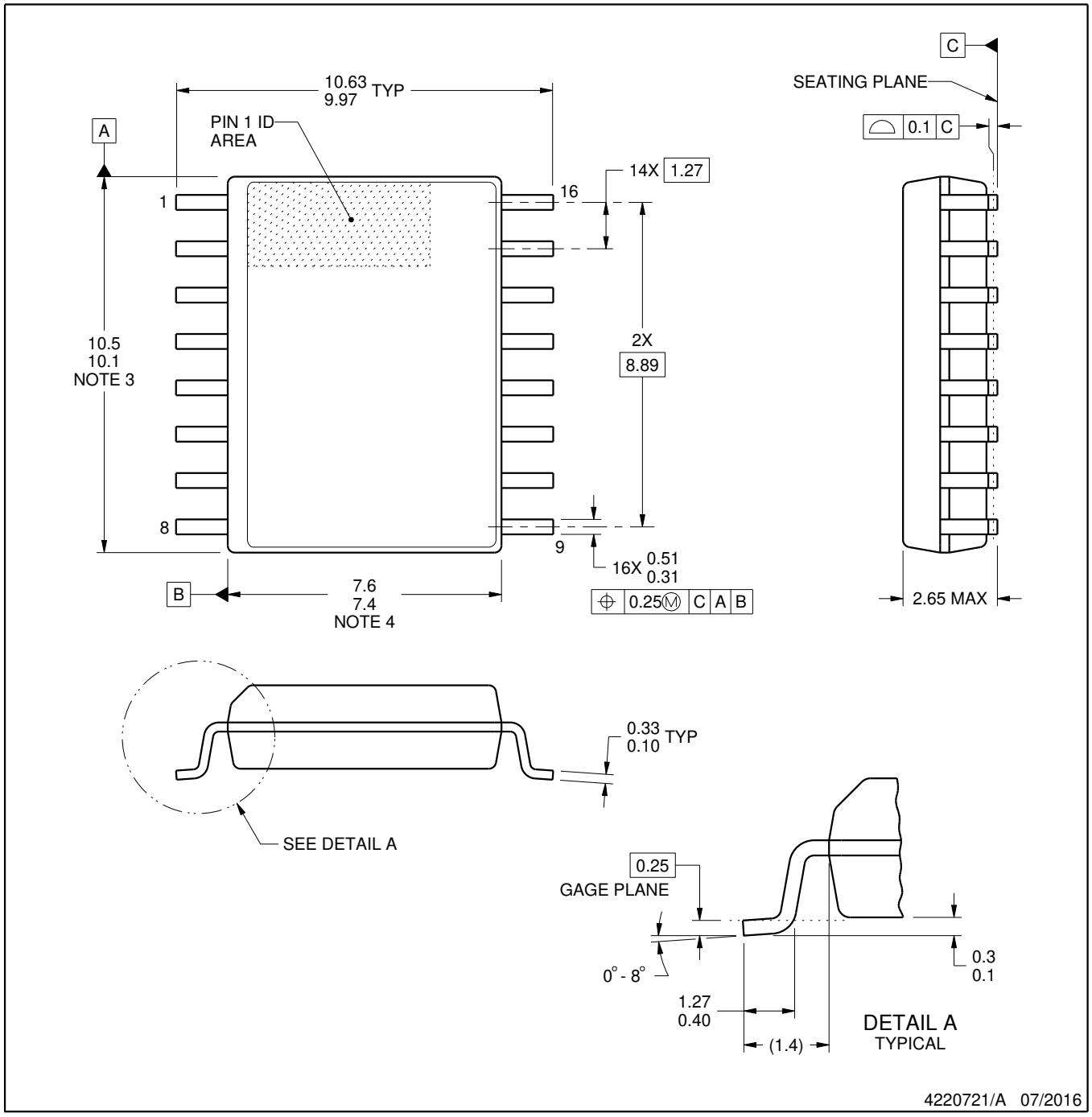


# PACKAGE OUTLINE

## DW0016A

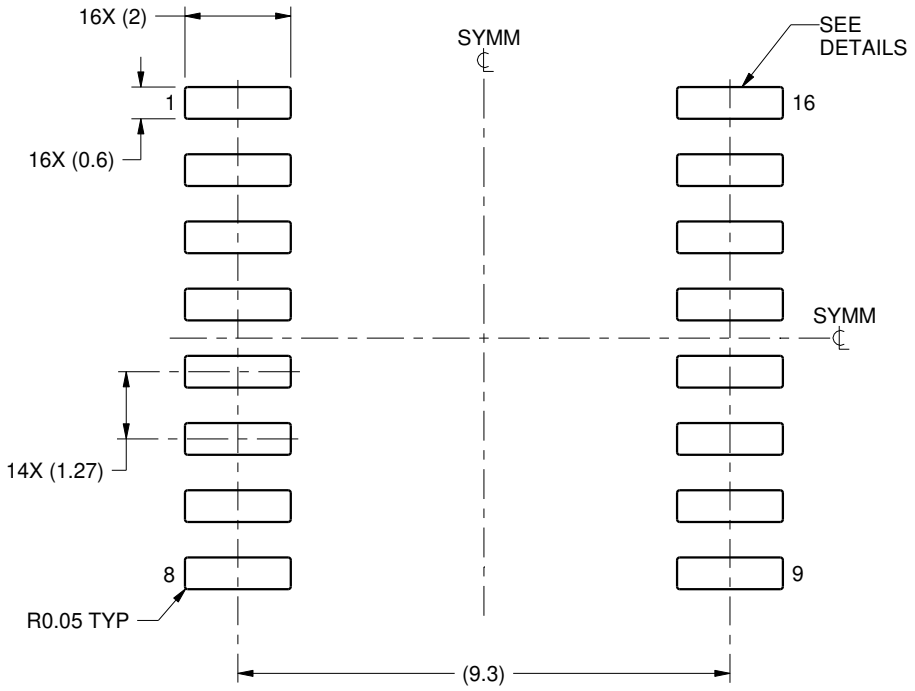
## SOIC - 2.65 mm max height

SOIC

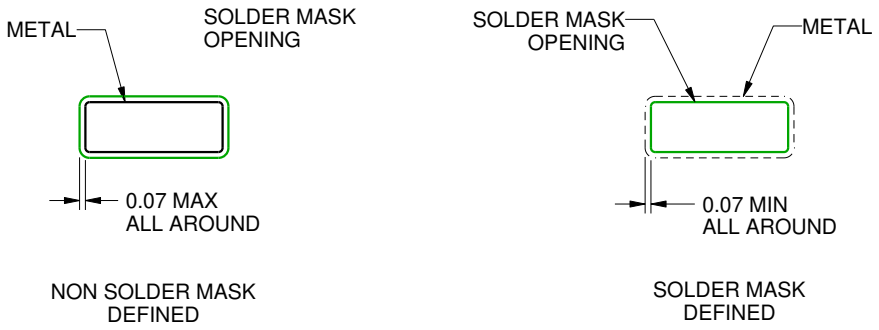



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:7X

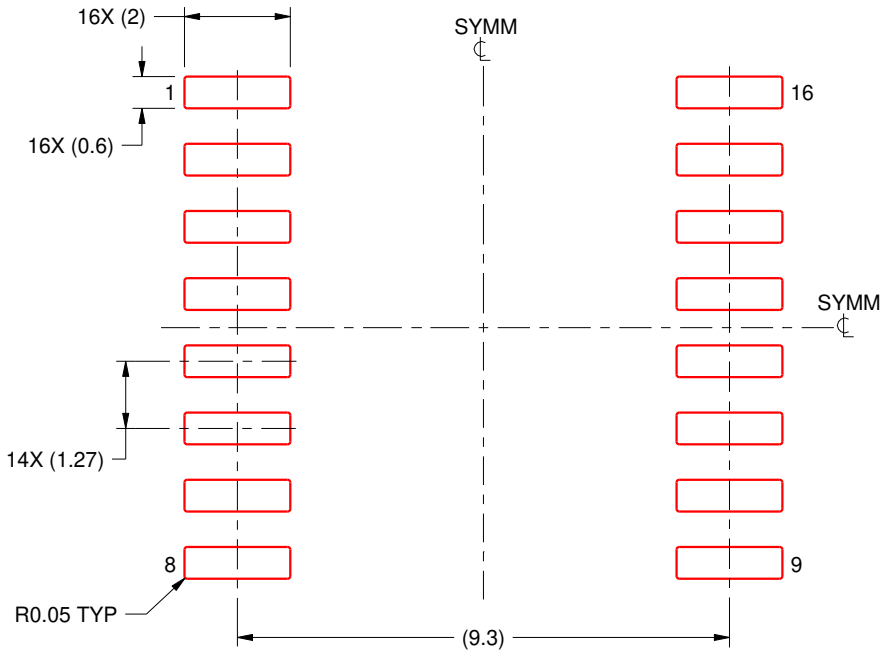



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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