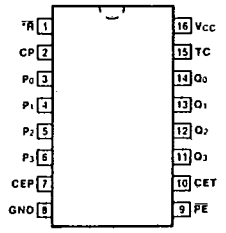
54/74161 • 54LS/74LS161
54/74163 • 54LS/74LS163

SYNCHRONOUS PRESETTABLE BINARY COUNTERS

DESCRIPTION — The '161 and '163 are high speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The '161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The '163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. For functional description and detail specifications please refer to the '160 data sheet. For S-TTL and LP-TTL versions please see the 9316 data sheet.

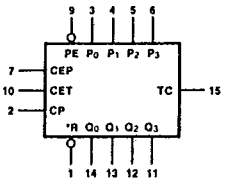
- **SYNCHRONOUS COUNTING AND LOADING**
- **HIGH SPEED SYNCHRONOUS EXPANSION**
- **LS VERSIONS FULLY EDGE TRIGGERED**

CONNECTION DIAGRAM
PINOUT A



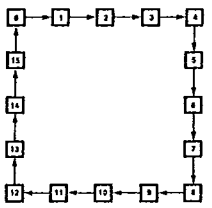
*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

LOGIC SYMBOL



*$\overline{MR}$ for '161 VCC = Pin 16
*$\overline{SR}$ for '163 Gnd = Pin 8

STATE DIAGRAM



ORDERING CODE: See Section 9

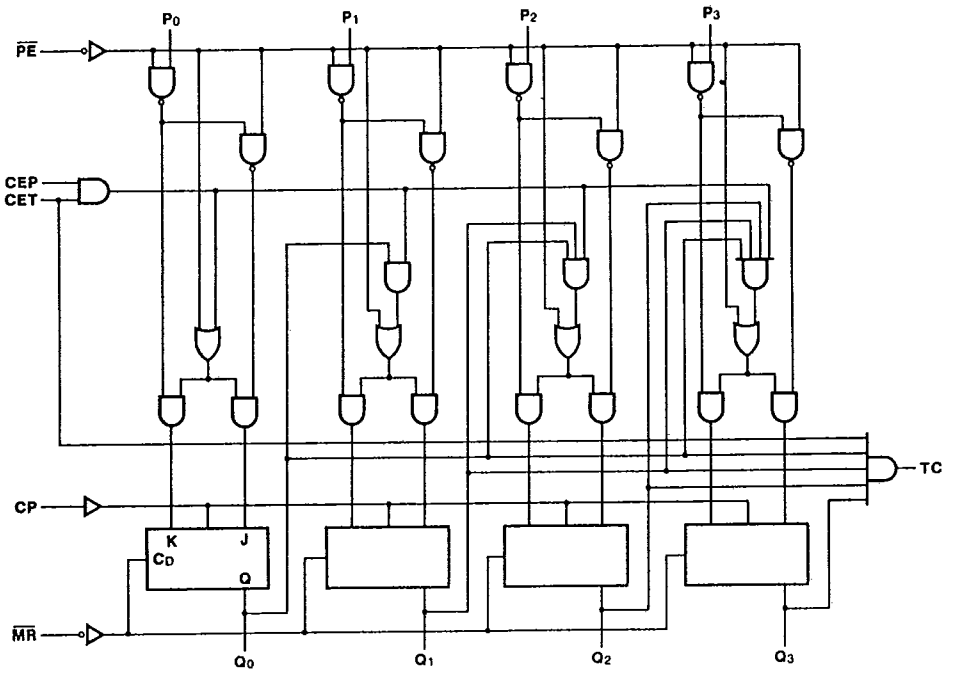
PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74161PC, 74LS161PC 74163PC, 74LS163PC		9B
Ceramic DIP (D)	A	74161DC, 74LS161DC 74163DC, 74LS163DC	54161DM, 54LS161DM 54163DM, 54LS163DM	7B
Flatpak (F)	A	74161FC, 74LS161FC 74163FC, 74LS163FC	54161FM, 54LS161FM 54163FM, 54LS163FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

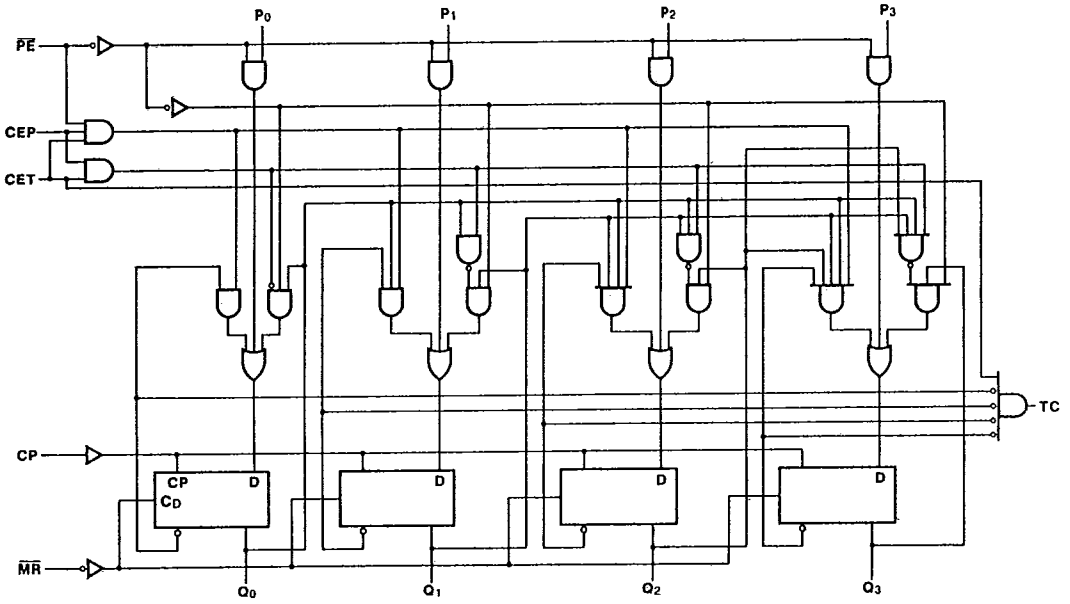
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	1.0/1.0	0.6/0.3
CET	Count Enable Trickle Input	2.0/2.0	1.0/0.5
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	0.6/0.3
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)	1.0/1.0	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	0.6/0.3
$Q_0 - Q_3$	Flip-flop Outputs	20/10	10/5.0 (2.5)
TC	Terminal Count Output	20/10	10/5.0 (2.5)

LOGIC DIAGRAMS

'161

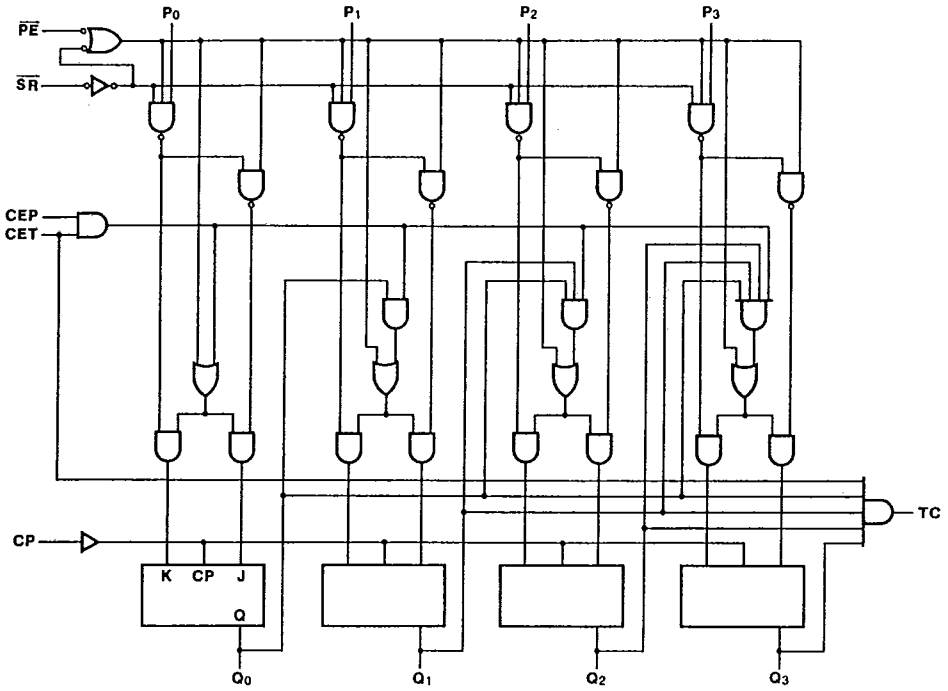


'LS161



LOGIC DIAGRAMS

'163



'LS163