

MOSFET – N-Channel, UniFET™ FRFET®

500 V, 100 A, 55 mΩ

FDL100N50F

Description

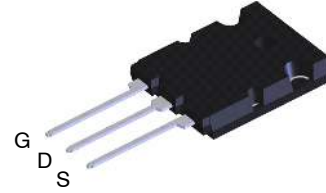
UniFET MOSFET is onsemi's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET MOSFET has been enhanced by lifetime control. Its trr is less than 100 nsec and the reverse dv/dt immunity is 15 V/ns while normal planar MOSFET's have over 200 nsec and 4.5 V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

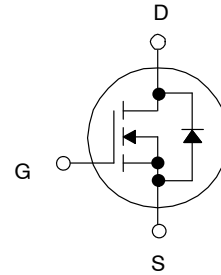
- $R_{DS(on)} = 43 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- Low Gate Charge (Typ. 238 nC)
- Low C_{rss} (Typ. 64 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

Applications

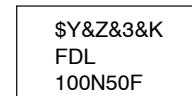
- Uninterruptible Power Supply
- AC-DC Power Supply



TO-264-3LD
CASE 340CA



MARKING DIAGRAM



FDL100N50F = Specific Device Code
 \$Y = onsemi Logo
 &Z = Assembly Location
 &3 = Date Code (Year and Week)
 &K = Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

FDL100N50F

MOSFET MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	FDL100N50F	Unit
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	100
		- Continuous ($T_C = 100^\circ\text{C}$)	60
I_{DM}	Drain Current	- Pulsed (Note 1)	400
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	5000
I_{AR}	Avalanche Current	(Note 1)	100
E_{AR}	Repetitive Avalanche Energy	(Note 1)	73.5
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	2500
		- Derate Above 25°C	20
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 1\text{ mH}$, $I_{AS} = 100\text{ A}$, $V_{DD} = 50\text{ V}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 100\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDL100N50F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.05	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	30	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\text{ V}$, $T_C = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.5	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	10	μA
		$V_{DS} = 400\text{ V}$, $T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}$, $V_{DS} = 0\text{ V}$	-	-	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 50\text{ A}$	-	0.043	0.055	Ω
gFS	Forward Transconductance	$V_{DS} = 20\text{ V}$, $I_D = 50\text{ A}$	-	95	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	12000	-	pF
C_{oss}	Output Capacitance		-	1700	-	pF
C_{riss}	Reverse Transfer Capacitance		-	64	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DD} = 400\text{ V}$, $I_D = 50\text{ A}$, $V_{GS} = 10\text{ V}$ (Note 4)	-	238	-	nC
Q_{gs}	Gate to Source Gate Charge		-	74	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	95	-	nC

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}$, $I_D = 50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 4.7\ \Omega$ (Note 4)	–	63	–	ns
t_r	Turn-On Rise Time		–	186	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	202	–	ns
t_f	Turn-Off Fall Time		–	105	–	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	100	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	400	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 100\text{ A}$	–	–	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_{SD} = 100\text{ A}$ $dI_F/dt = 100\text{ A}/\mu\text{s}$	–	250	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping [†]
FDL100N50F	FDL100N50F	TO – 264	N/A	N/A	25 Units / Tube

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

TYPICAL CHARACTERISTICS

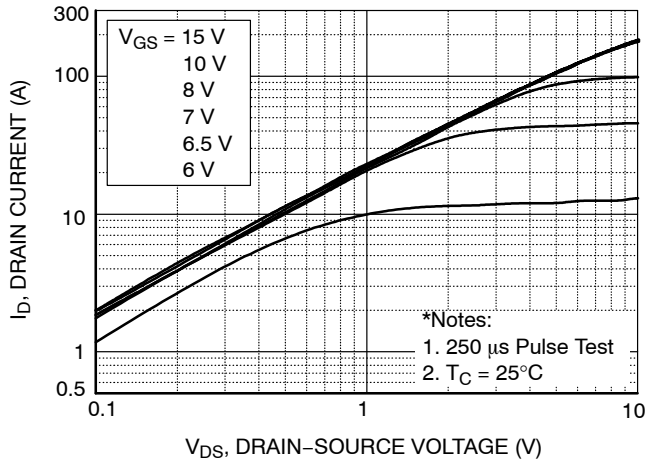


Figure 1. On-Region Characteristics

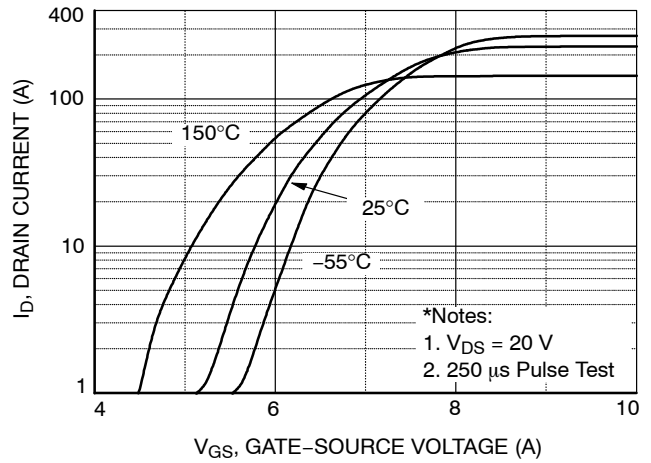


Figure 2. Transfer Characteristics

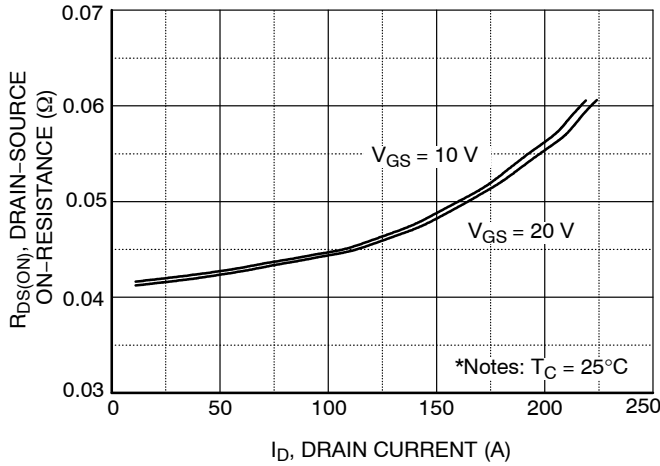


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

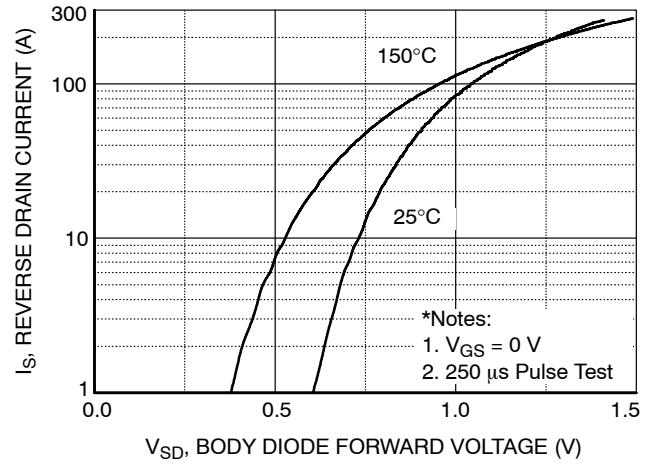


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

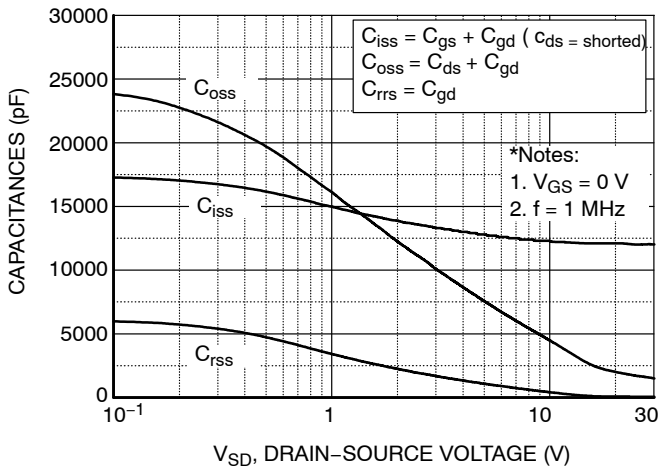


Figure 5. Capacitance Characteristics

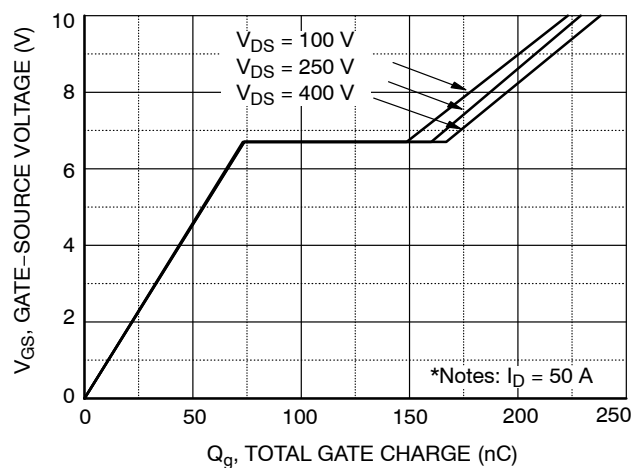


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (continued)

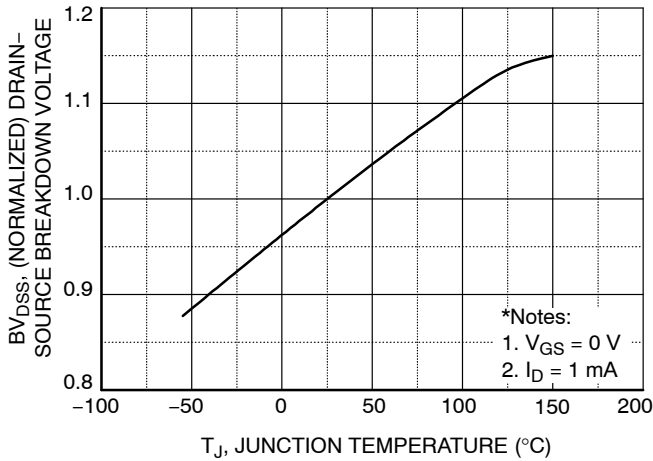


Figure 7. Breakdown Voltage Variation vs. Temperature

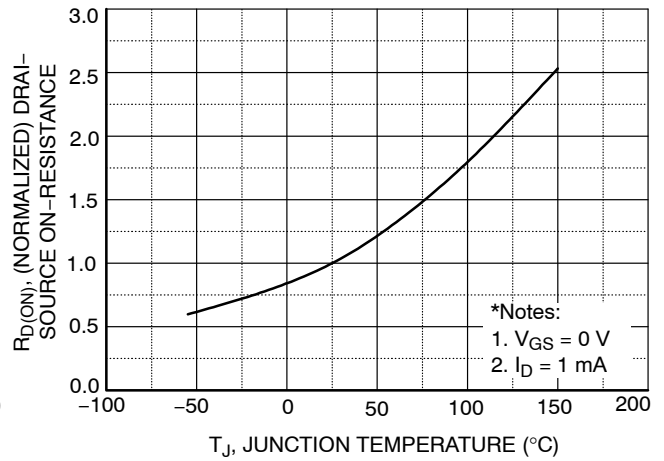


Figure 8. On-Resistance Variation vs. Temperature

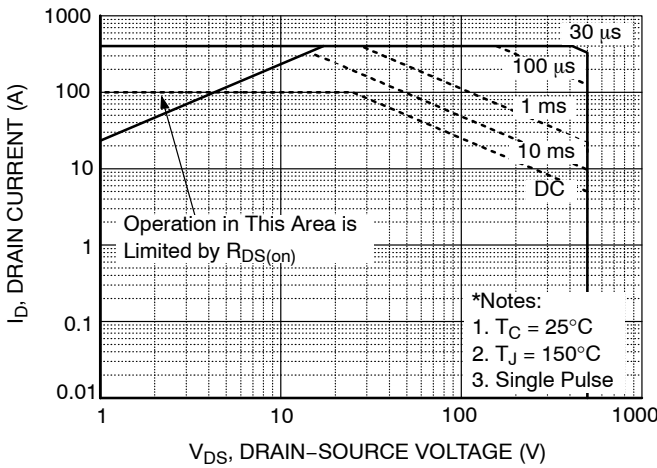


Figure 9. Maximum Safe Operating Area

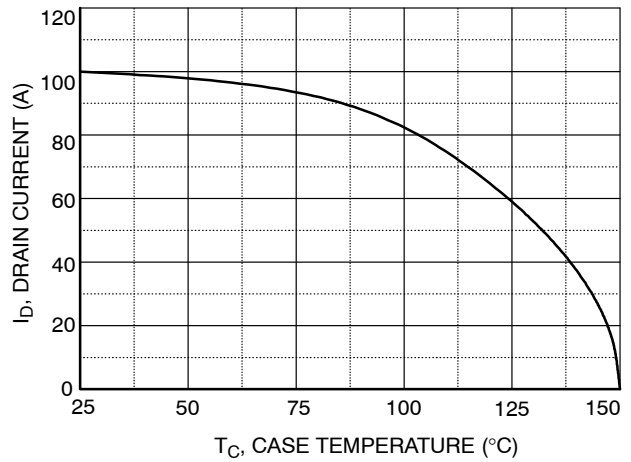


Figure 10. Maximum Drain Current vs. Case Temperature

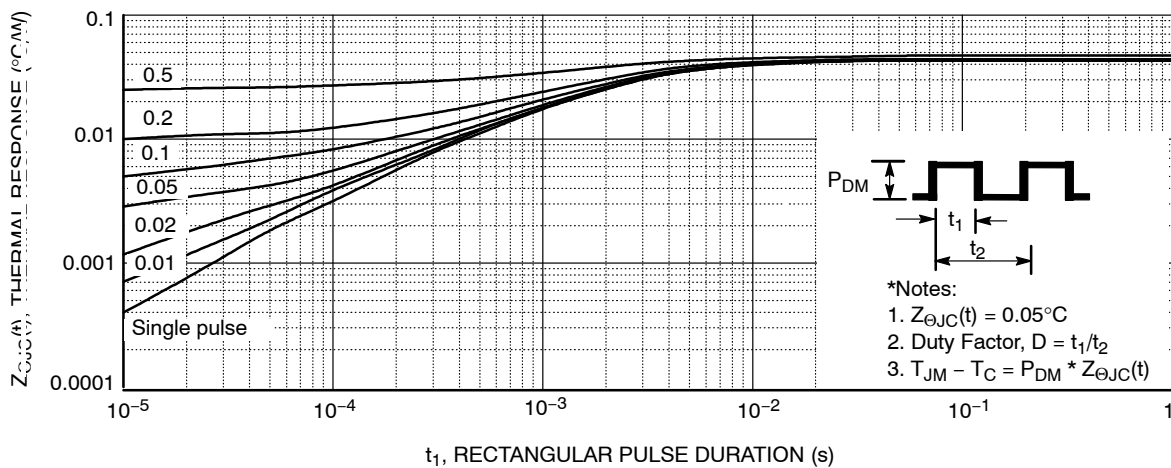


Figure 11. Transient Thermal Response Curve

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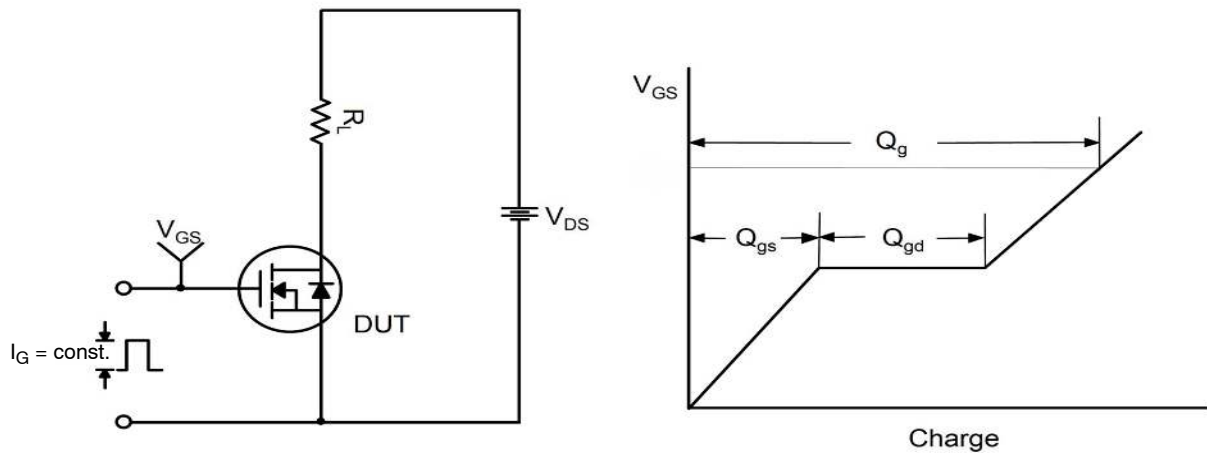


Figure 12. Gate Charge Test Circuit & Waveforms

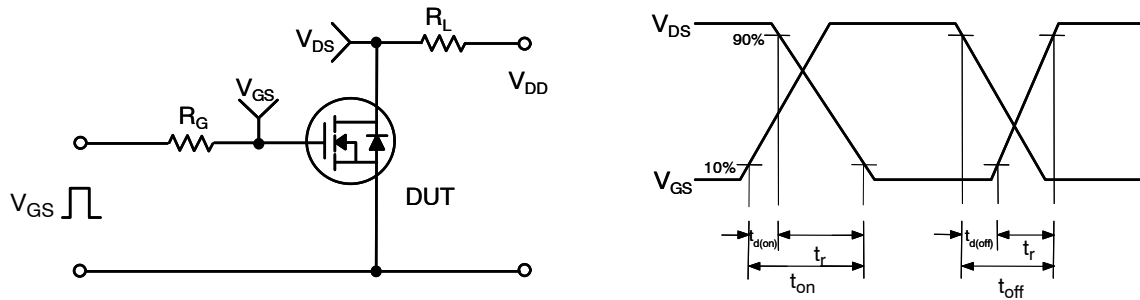


Figure 13. Resistive Switching Test Circuit & Waveforms

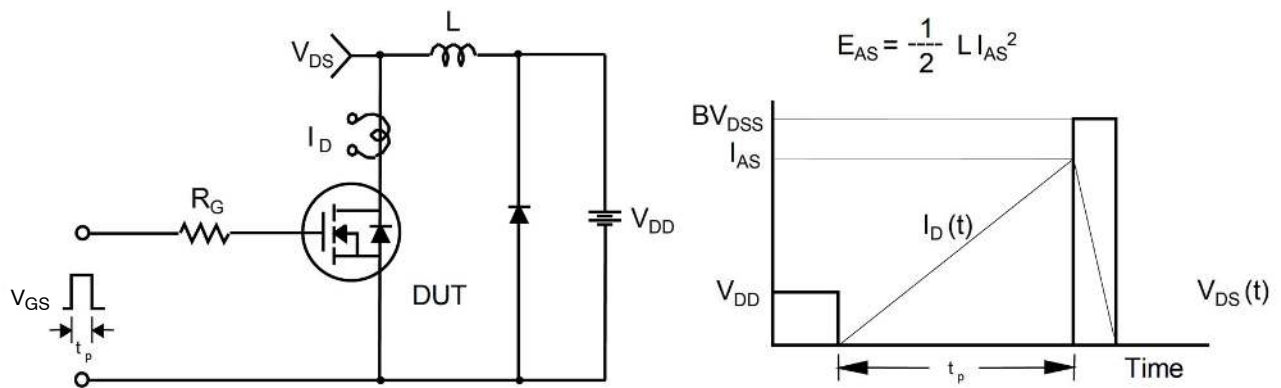


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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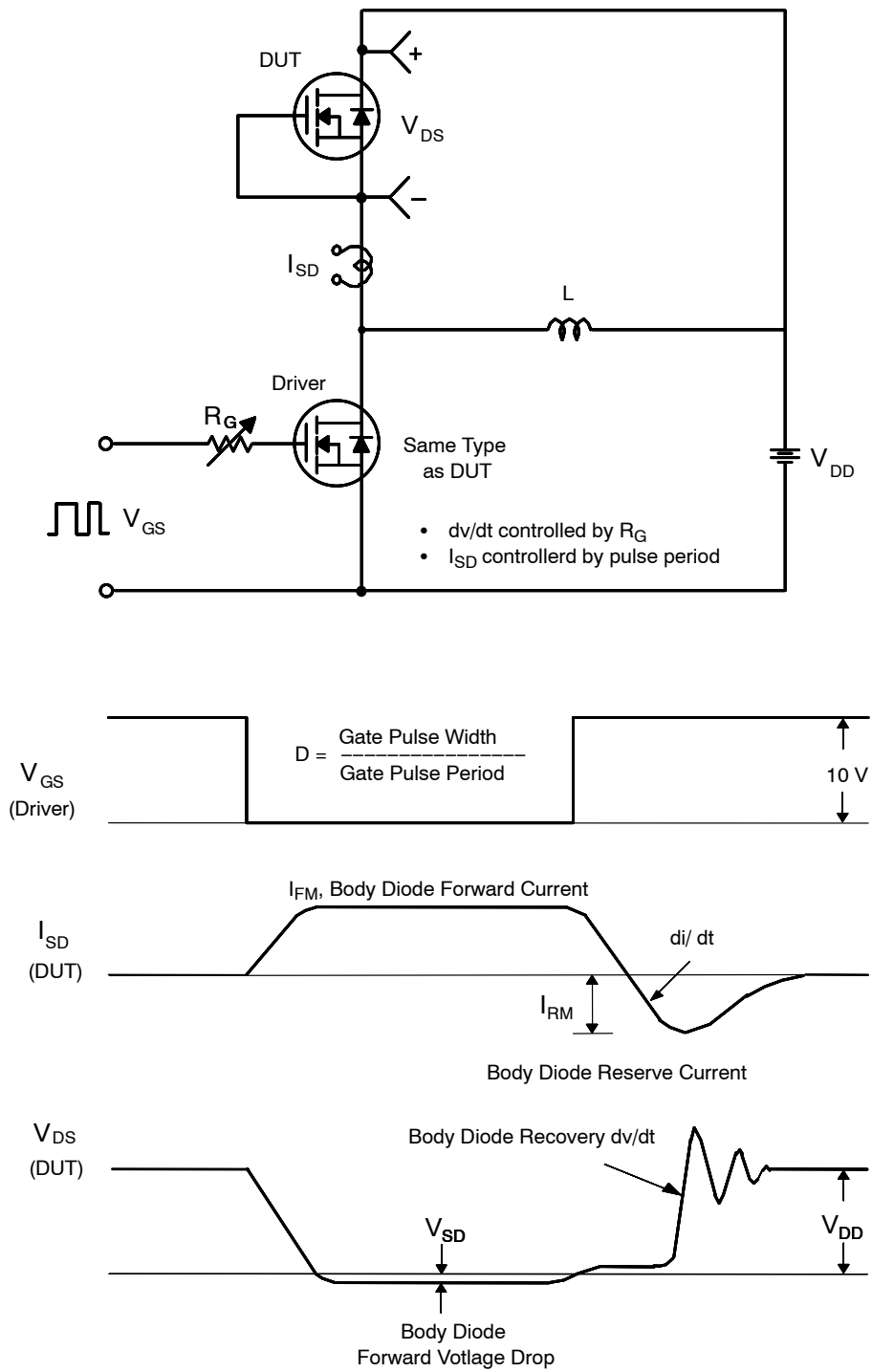


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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MECHANICAL CASE OUTLINE

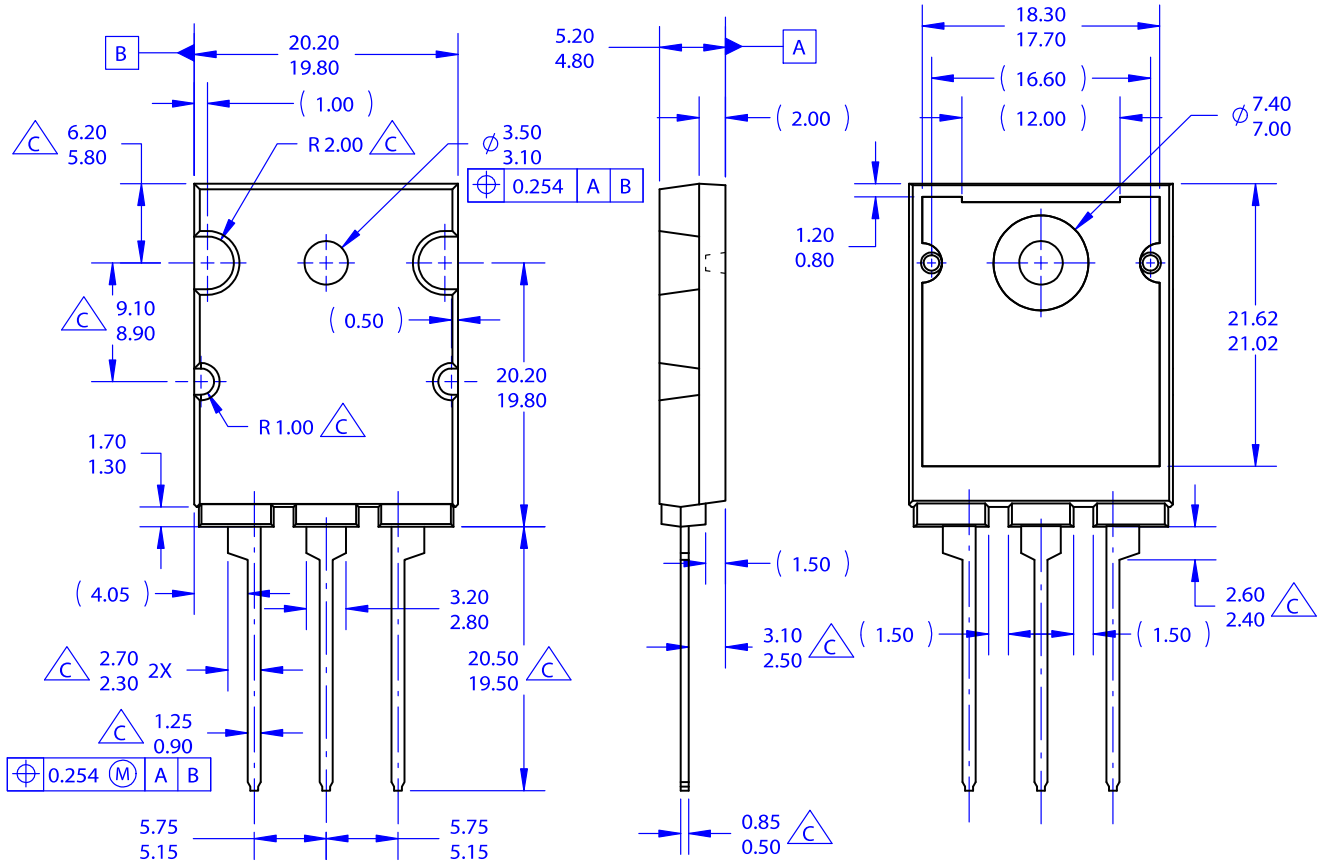
PACKAGE DIMENSIONS

ON Semiconductor®



TO-264-3LD
CASE 340CA
ISSUE O

DATE 31 OCT 2016



NOTES:

- A. PACKAGE REFERENCE: JEDEC TO264 VARIATION AA.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

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