ADS127L01 24-Bit, High-Speed, Wide-Bandwidth Analog-to-Digital Converter

1 Features

- Data Rates: Up to 512 kSPS
- AC + DC Performance:
  - Passband: Up to 230 kHz
  - SNR: Up to 115.5 dB
  - THD: Down to -129 dB
  - DC Accuracy:
  - Offset Drift: 1.5 μV/°C
  - Gain Drift: 0.2 ppm/°C
- Operating Modes:
  - High-resolution (128 kSPS at 26 mW)
  - Low-power (128 kSPS at 15 mW)
  - Very-low Power: 105 dB SNR (128 kSPS at 9 mW)
- Digital Filter Options:
  - Low-latency Filter: Sinc Frequency Response
  - Wideband 1 Filter: (0.45 to 0.55) × f_{DATA} Transition Band
  - Wideband 2 Filter: (0.40 to 0.50) × f_{DATA} Transition Band
- SPI™ or Frame-Sync Serial Interface
  - Daisy-Chain Compatible
- Analog Supply: 2.7 V to 3.6 V
- Digital Supply: 1.7 V to 3.6 V
- Operating Temperature: –40°C to +125°C

2 Applications

- Vibration and Modal Analysis
- Data Acquisition Systems
- Acoustics and Dynamic Strain Gauges
- Power Quality Analysis

3 Description

The ADS127L01 is a 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) with data rates up to 512 kSPS. This device offers a unique combination of excellent dc accuracy and outstanding ac performance. The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The integrated decimation filter suppresses modulator out-of-band noise. In addition to al low-latency filter, the ADS127L01 provides multiple Wideband filters with less than ±0.00004 dB of ripple, and an option for –116-dB stop-band attenuation at the Nyquist rate.

Traditionally, industrial delta-sigma ADCs that offer good drift performance use digital filters with large passband droop. As a result, industrial delta-sigma ADCs have limited signal bandwidth and are mostly suited for dc measurements. High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly weaker than industrial counterparts. The ADS127L01 combines these converters, providing high-precision industrial measurement with excellent dc and ac specifications over an extended industrial temperature range of –40°C to +125°C.

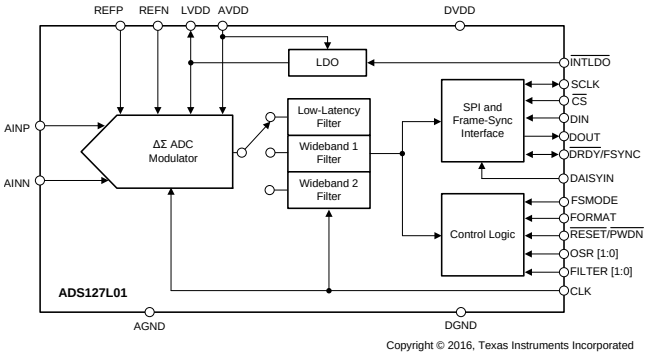
A variety of operating modes allow for optimization of speed, resolution, and power. A programmable serial interface with one of three options (SPI, frame-sync slave, or frame-sync master) provides convenient interfacing across isolation barriers to microcontrollers or digital signal processors (DSPs).

Device Information[1]

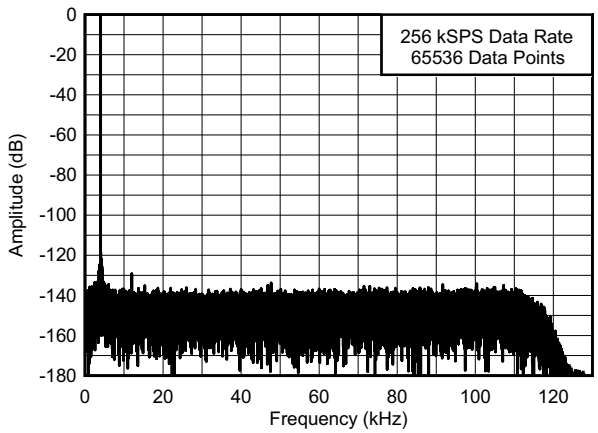
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS127L01	TQFP (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

ADS127L01 Block Diagram



ADC Frequency Spectrum



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- *Features*, Changed THD: –126 dB 9LP and VLP modes) To: THD: Down to -129 dB ... 1
- *Features*, Changed DC Accuracy To: Integral Nonlinearity: 1 ppm ... 1
- *Features*, Changed HR: 111 dB SNR To: High-resolution ... 1
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- *Pin Functions*, Changed pin 14 description of 1: Master mode ... 5
- *Pin Functions*, Changed pin 19 description "protocol" To: interface ... 5
- *Pin Functions*, Changed pin 27 description "Decouple DVDD to DGND with a 1-µF capacitor" To: Connect a 1-µF capacitor to DGND ... 5
- *Pin Functions*, Changed pin 32 description "Decouple AVDD to AGND with a 1-µF capacitor" To: Connect a 1-µF capacitor to AGND ... 5
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- *Timing Requirements: Frame-Sync Slave Mode*, Deleted text from conditions statement "and DVDD = 1.7 V to 3.6 V" ... 14
- *Typical Characteristics*, Changed conditions statement ... 16
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- Changed text frame-sync mode To: frame-sync interface mode throughout the document ... 26

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- Changed text frame-sync protocol. To: frame-sync interface mode throughout the document ... 26
- Changed section *Mode Selection* To: *Operating Modes (HR, LP, VLP)* ... 38
- Changed section *Filter Selection Pins (FILTER*) To: *Digital-Filter Path Selection Pins (FILTER[1:0])* ... 40
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- Figure 86, Changed $t_{w(STH)}$ To: $t_{w(STL)}$ ... 42
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- *Data Ready ($\overline{DRDY}$/FSYNC)*, Added text "A new conversion result is..." ... 47
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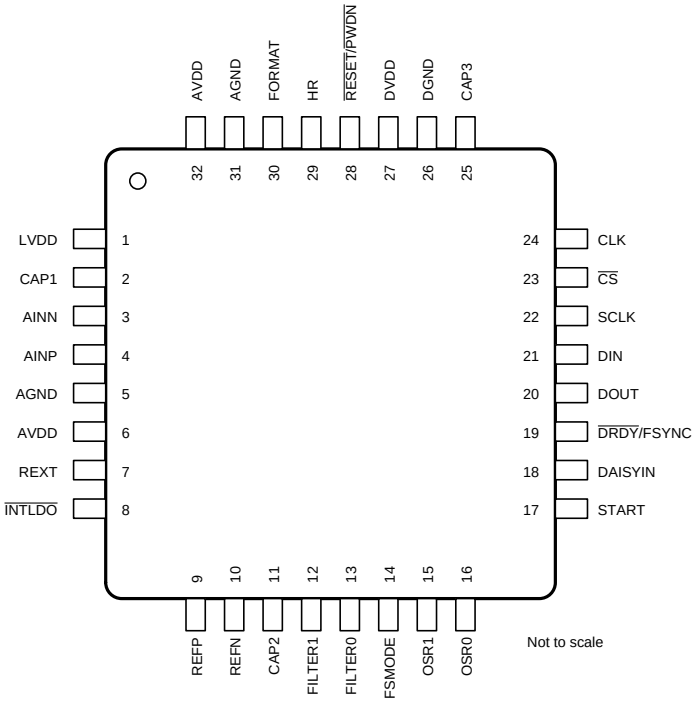
5 Pin Configuration and Functions

PBS package
32-Pin TQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION(1)
NO.	NAME		
1	LVDD	Supply	LVDD analog supply. INTLDO = 0: LVDD is an analog-supply output pin. Connect a 1-µF capacitor to AGND. INTLDO = 1: LVDD is an analog-supply input pin. Connect to a 1.8-V supply.
2	CAP1	Analog output	Modulator common-mode voltage. Connect a 1-µF capacitor to AGND
3	AINN	Analog input	Negative analog input.
4	AINP	Analog input	Positive analog input.
5	AGND	Supply	Analog ground.
6	AVDD	Supply	Analog supply. Connect a 1-µF capacitor to AGND.
7	REXT	Analog input	Analog power-scaling bias resistor pin. Recommended external resistor values: R_{EXT} = 60.4 kΩ to AGND for high-resolution (HR) and low-power (LP) modes R_{EXT} = 120 kΩ to AGND for very-low-power (VLP) mode
8	INTLDO	Digital input	LVDD voltage selection pin (pull high to AVDD or low to AGND through 10-kΩ resistor). 0: Internal analog low-dropout regulator (LDO) for LVDD voltage supply. 1: External LVDD voltage supply.
9	REFP	Analog input	Positive analog reference input. Connect a minimum 10-µF capacitor to REFN
10	REFN	Analog input	Negative analog reference input.
11	CAP2	Analog output	Reference common-mode voltage. Connect a 1-µF capacitor to AGND.

(1) See the *Unused Inputs and Outputs* section for unused pin connections.

Pin Functions (continued)

PIN		I/O	DESCRIPTION(1)
NO.	NAME		
12	FILTER1	Digital input	Digital filter select pin(2). 00: Wideband 1 filter (WB1) 01: Wideband 2 filter (WB2) 10: Low-latency filter (LL) 11: Reserved
13	FILTER0	Digital input	
14	FSMODE	Digital input	Frame-sync mode pin(2). 0: Slave mode 1: Master mode. Applies to Frame-Sync interface mode only. No effect in SPI interface mode.
15	OSR1	Digital input	Oversampling ratio (OSR) pin for the decimation filters(2). Wideband filters, FILTER[1:0] = 00 or 01: 00: 32x oversampling (OSR 32) 01: 64x oversampling (OSR 64) 10: 128x oversampling (OSR 128) 11: 256x oversampling (OSR 256) Low-latency filter, FILTER[1:0] = 10: 00: 32x oversampling (OSR 32) 01: 128x oversampling (OSR 128) 10: 512x oversampling (OSR 512) 11: 2048x oversampling (OSR 2048)
16	OSR0	Digital input	
17	START	Digital input	Synchronization signal to start or restart a conversion.
18	DAISYIN	Digital input	Daisy-chain input.
19	$\overline{\text{DRDY}}$/FSYNC	Digital input/output	SPI interface: Data ready, active low(3). Frame-sync interface: Frame-sync input signal(3)
20	DOUT	Digital output	Serial data output
21	DIN	Digital input	Serial data input. Tie directly to DGND when using the frame-sync interface.
22	SCLK	Digital input/output	Serial clock input(3).
23	$\overline{\text{CS}}$	Digital input	Chip select. Tie directly to DGND when using the frame-sync interface.
24	CLK	Digital input	Master clock input.
25	CAP3	Analog output	Internally-generated digital operating voltage. Connect a 1-µF capacitor to DGND.
26	DGND	Supply	Digital ground.
27	DVDD	Supply	Digital supply. Connect a 1-µF capacitor to DGND(3)
28	$\overline{\text{RESET}}$/$\overline{\text{PWDN}}$	Digital input	Reset or power-down pin, active low(3).
29	HR	Digital input	ADC operating mode(2). 1: High-resolution (HR) 0: Low-power (LP) or very-low-power (VLP)(4)
30	FORMAT	Digital input	Interface select pin(2). 0: SPI 1: Frame-Sync
31	AGND	Supply	Analog ground.
32	AVDD	Supply	Analog supply. Decouple AVDD to AGND with a 1-µF capacitor.

(2) Pull the hardware mode pins high to DVDD or low to DGND through 100-kΩ resistors.
(3) See the *Reset and Power-Down Pin ($\overline{\text{RESET}}$/$\overline{\text{PWDN}}$)* section for specific hardware design details if using power-down mode.
(4) Entering LP mode or VLP mode is set by R_{EXT} resistor value.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage	AVDD to AGND	–0.3	4.0	V
	DVDD to DGND	–0.3	4.0	
	LVDD to AGND	–0.3	2.0	
	AGND to DGND	–0.3	0.3	
	REFP to AGND	–0.3	AVDD + 0.3	
	REFN to AGND	–0.3	AVDD + 0.3	
	Analog input	AGND – 0.3	AVDD + 0.3	
	Digital input	DGND – 0.3	DVDD + 0.3	
Current	Input, continuous, any pin except power supply pins (2)	–10	10	mA
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Limit the input current to 10 mA or less if the analog input voltage exceeds AVDD + 0.3 V or is less than AGND – 0.3 V, or if the digital input voltage exceeds DVDD + 0.3 V or is less than DGND – 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
AVDD	Analog power supply		2.7	3.0	3.6	V
LVDD	Low voltage analog supply	$\overline{\text{INTLDO}}$ = 1	1.7	1.8	1.9	V
DVDD	Digital supply		1.7	1.8	3.6	V
ANALOG INPUTS						
V_{IN}	Differential input voltage	$V_{IN} = (V_{AINP} - V_{AINN})$	$-V_{REF}$		V_{REF}	V
V_{AINP}, V_{AINN}	Absolute input voltage	AINP or AINN to AGND	AGND		AVDD	V
V_{CM}	Common-mode input voltage	$V_{CM} = (V_{AINP} + V_{AINN}) / 2$		AVDD / 2		V
VOLTAGE REFERENCE INPUTS						
V_{REFN}	Negative reference input		AGND – 0.1	AGND	AGND + 1.0	V
V_{REFP}	Positive reference input		V_{REFN} + 0.5	2.5	AVDD	V
V_{REF}	Reference input voltage	$V_{REF} = V_{REFP} - V_{REFN}$	0.5	2.5	3.0	V
EXTERNAL CLOCK SOURCE						
f_{CLK}	Master clock rate(1)	HR mode	0.1	16.384	17.6	MHz
		LP mode	0.1	8.192	8.8	
		VLP mode	0.1	4.096	4.4	
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) To meet maximum speed conditions, f_{CLK} duty cycle must be 49% < duty cycle < 51%.

6.4 Thermal Information

THERMAL METRIC(1)		ADS127L01 PBS (TQFP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C.
All specifications are at AVDD = 3 V, LVDD = 1.8 V (external), DVDD = 1.8 V, V_{REF} = 2.5 V, $\overline{INTLDO}$ = 1, FILTER[1:0] = 01 (WB2), and f_{CLK} = 16.384 MHz for HR mode, 8.192 MHz for LP mode, or 4.096 MHz for VLP mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
	Differential input impedance	HR mode, f_{CLK} = 16.384 MHz			5		kΩ
		LP mode, f_{CLK} = 8.192 MHz			11		
		VLP mode, f_{CLK} = 4.096 MHz			23		
DC PERFORMANCE							
	Resolution	No missing codes			24		Bits
f_{DATA}	Data rate	HR mode	Wideband filters		512, 256, 128, 64		kSPS
			Low-latency filter		512, 128, 32, 8		
		LP mode	Wideband filters		256, 128, 64, 32		
			Low-latency filter		256, 64, 16, 4		
		VLP mode	Wideband filters		128, 64, 32, 16		
			Low-latency filter		128, 32, 8, 2		
INL	Integral nonlinearity(1)	HR mode	V_{CM} = AVDD / 2		2.5	10	ppm
		LP mode	V_{CM} = AVDD / 2		1	5	
		VLP mode	V_{CM} = AVDD / 2		1	5	
	Offset error				±0.1		mV
	Offset drift				1.5	3.0	µV/°C
	Gain error				0.2		%FSR
	Gain calibration accuracy				0.003%		
	Gain drift	HR mode			0.8	3	ppm/°C
		LP mode			0.4	2.5	
		VLP mode			0.2	2	
	Noise(2)	HR mode	WB2, OSR 32		10.6		μV_{RMS}
			WB2, OSR 64		7.3	10.1	
			WB2, OSR 128		5.1	7.2	
			WB2, OSR 256		3.6	5.2	
CMRR	Common-mode rejection ratio	f_{CM} = 60 Hz			95		dB
PSRR	Power-supply rejection ratio	f_{PS} = 60 Hz	AVDD		90		dB
			DVDD		85		
			LVDD		80		

(1) Best fit method.
(2) For all Wideband filter configurations, see Table 1. For all Low-latency filter configurations, see Table 2.

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 3 V, LVDD = 1.8 V (external), DVDD = 1.8 V, V_{REF} = 2.5 V, $\overline{INTLDO}$ = 1, FILTER[1:0] = 01 (WB2), and f_{CLK} = 16.384 MHz for HR mode, 8.192 MHz for LP mode, or 4.096 MHz for VLP mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SNR	Signal-to-noise ratio (2) (3)	WB2, OSR 32		104.4		dB
		WB2, OSR 64	104.9	107.8		
		WB2, OSR 128	107.9	110.9		
		WB2, OSR 256	110.6	113.9		
		WB2, OSR 32, V_{REF} = 3 V		105.8		
		WB2, OSR 64, V_{REF} = 3 V		109.3		
		WB2, OSR 128, V_{REF} = 3 V		112		
		WB2, OSR 256, V_{REF} = 3 V		115.5		
THD	Total harmonic distortion (4)	HR mode, f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS		–113		dB
		LP mode, f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS		–126		
		VLP mode, f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS		–129		
SFDR	Spurious-free dynamic range	HR mode		–115		dB
		LP mode		–130		
		VLP mode		–130		
DIGITAL FILTER RESPONSE: WIDEBAND						
	Bandwidth			See Table 1		
	Pass-band ripple			±0.000032		dB
	Transition band	FILTER[1:0] = 00 (WB1)		(0.45 to 0.55) × f_{DATA}		Hz
		FILTER[1:0] = 01 (WB2)		(0.40 to 0.50) × f_{DATA}		
	Stop-band attenuation		116			dB
	Group delay			42 / f_{DATA}		s
	Settling time	Complete settling		84 / f_{DATA}		s
DIGITAL FILTER RESPONSE: LOW-LATENCY						
	Bandwidth			See Table 2		
	Group delay			See *Low-Latency Filter* section		
	Settling time			See *Low-Latency Filter* section		
VOLTAGE REFERENCE INPUTS						
	Reference input impedance	HR mode		2.2		kΩ
		LP mode		3.2		
		VLP mode		4		
SYSTEM MONITORS						
	Input over-range detect accuracy			±100		mV
DIGITAL INPUT/OUTPUT (DVDD = 1.7 V to 3.6 V)						
V_{IH}	High-level input voltage		0.7 DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.3 DVDD	V
V_{OH}	High-level output voltage	I_{OH} = 2 mA	0.8 DVDD		DVDD	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA	DGND		0.2 DVDD	V
I_H	Input leakage, high	I_H = 3.6 V	–10		10	µA
I_L	Input leakage, low	I_L = DGND	–10		10	µA

(3) Minimum SNR is ensured by the limit of the *dc noise* specification.
(4) THD includes the first nine harmonics of the input signal.

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 3 V, LVDD = 1.8 V (external), DVDD = 1.8 V, V_{REF} = 2.5 V, $\overline{\text{INTLDO}}$ = 1, FILTER[1:0] = 01 (WB2), and f_{CLK} = 16.384 MHz for HR mode, 8.192 MHz for LP mode, or 4.096 MHz for VLP mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
	Power-down current	AVDD	$\overline{\text{INTLDO}}$ = 0		8		µA
			$\overline{\text{INTLDO}}$ = 1		2		
		DVDD			0.6		
		LVDD, $\overline{\text{INTLDO}}$ = 1			0.6		
I_{AVDD}	AVDD current	HR mode			1.3	1.6	mA
		LP mode			0.8	1.0	
		VLP mode			0.4	0.6	
I_{LVDD}	LVDD current(5) (6)	HR mode			9.3	11	mA
		LP mode			4.6	5.5	
		VLP mode			2.3	2.8	
I_{DVDD}	DVDD current(2)	HR mode	OSR 128		2.8	3.4	mA
		LP mode	OSR 128		1.5	1.8	
		VLP mode	OSR 128		0.8	1.1	
P_D	Power dissipation	HR mode, OSR 128, AVDD = 3.0 V, DVDD = 1.8 V	$\overline{\text{INTLDO}}$ = 1, LVDD = 1.8 V,		25.7	30.8	mW
			$\overline{\text{INTLDO}}$ = 0		36.8	44.2	
		LP mode, OSR 128, AVDD = 3.0 V, DVDD = 1.8 V	$\overline{\text{INTLDO}}$ = 1, LVDD = 1.8 V,		13.4	16.1	
			$\overline{\text{INTLDO}}$ = 0		18.9	22.7	
		VLP mode, OSR 128, AVDD = 3.0 V, DVDD = 1.8 V	$\overline{\text{INTLDO}}$ = 1, LVDD = 1.8 V,		6.8	8.2	
			$\overline{\text{INTLDO}}$ = 0		9.5	11.4	

(5) LVDD current sourced from AVDD when the internal LDO is used ($\overline{\text{INTLDO}}$ = 0).
(6) LVDD current scales with f_{CLK}; see Figure 47.

6.6 Timing Requirements: Serial Interface

over operating ambient temperature range (unless otherwise noted)

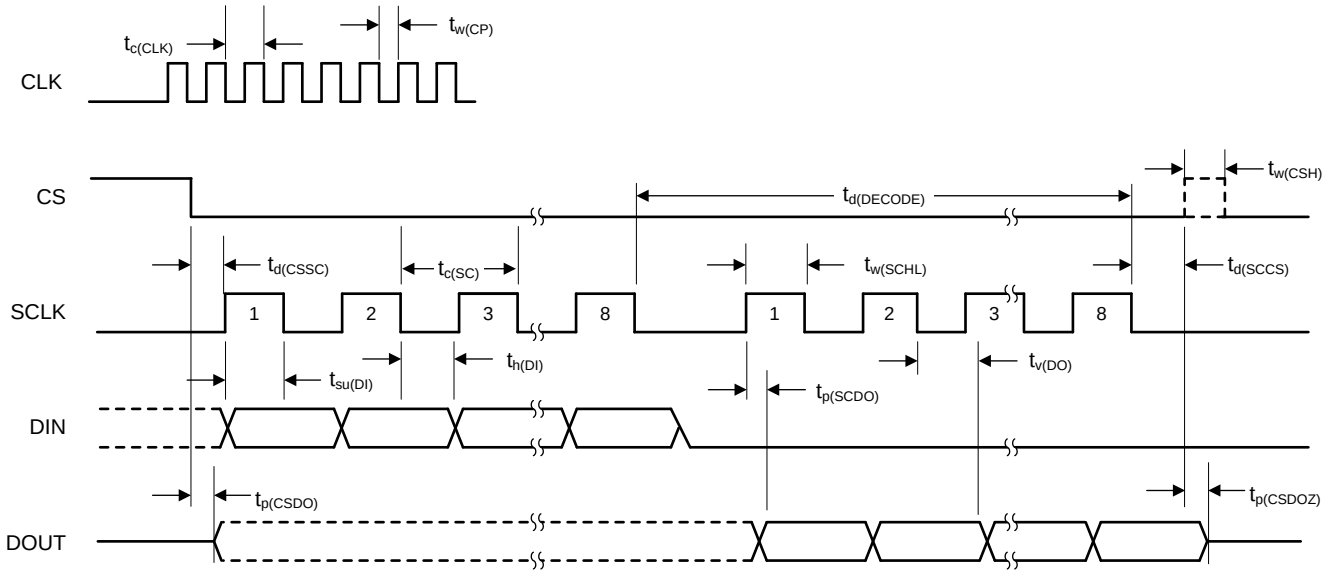
			2.8 V < DVDD ≤ 3.6 V			1.7 V ≤ DVDD ≤ 2.8 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CLK)}$	Master clock period	HR mode	57		10,000	57		10,000	ns
		LP mode	114		10,000	114		10,000	
		VLP mode	227		10,000	227		10,000	
$t_{w(CP)}$	Pulse duration, Master clock high or low	HR mode	28		5,000	28		5,000	ns
		LP mode	56		5,000	56		5,000	
		VLP mode	112		5,000	112		5,000	
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1)		8			12			ns
$t_{c(SC)}$	SCLK period		40		6250	50		6250	ns
$t_{w(SCHL)}$	Pulse duration, SCLK high or low		20			25			ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge		6			9			ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge		8			9			ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high		6			6			t_{CLK}
$t_{d(SCCS)}$	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge		2			2			t_{CLK}
$t_{d(DECODE)}$	Delay time, command decode time		4			4			t_{CLK}
	SPI timeout(2)	TOUT_DEL = 0			2^{16}			2^{16}	t_{CLK}
		TOUT_DEL = 1			2^{14}			2^{14}	t_{CLK}
$t_{su(DCI)}$	Setup time, DAISYIN valid before SCLK falling edge		5			8			ns
$t_{h(DCI)}$	Hold time, DAISYIN valid after SCLK falling edge		20			25			ns

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) See the *SPI Timeout* section for more information.

6.7 Switching Characteristics: Serial Interface Mode

over operating ambient temperature range (unless otherwise noted)

		2.8 V < DVDD ≤ 3.6 V			1.7 V ≤ DVDD ≤ 2.8 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven			12			18	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT			15			21	ns
$t_{v(DO)}$	Valid time, SCLK falling edge to DOUT invalid	18	t_{SCLK} / 2		20	t_{SCLK} / 2		ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance			20			20	ns



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. SPI Interface Timing

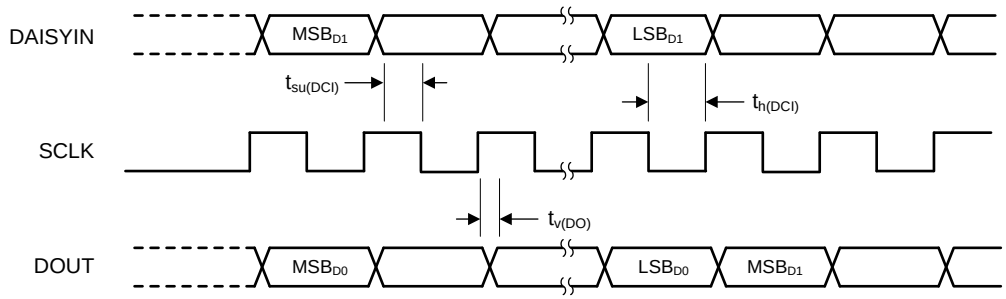


Figure 2. SPI Daisy-Chain Interface Timing

6.8 Timing Requirements: Frame-Sync Master Mode

over operating ambient temperature range and DVDD = 1.7 V to 3.6 V (unless otherwise noted)

			1.7 V ≤ DVDD ≤ 3.6 V			UNIT
			MIN	TYP	MAX	
$t_{c(CLK)}$	Master clock period	HR mode	57		10,000	ns
		LP mode	114		10,000	
		VLP mode	227		10,000	
$t_{w(CP)}$	Pulse duration, Master clock high or low	HR mode	28		5,000	ns
		LP mode	56		5,000	
		VLP mode	112		5,000	

6.9 Switching Characteristics: Frame-Sync Master Mode

over operating free-air temperature range (unless otherwise noted)

		2.8 V < DVDD ≤ 3.6 V			1.7 V ≤ DVDD ≤ 2.8 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{d(CSC)}$	Delay time, CLK rising edge to SCLK falling edge		15			15		ns
$t_{c(FRAME)}$	Frame period		$1 / f_{DATA}$			$1 / f_{DATA}$		s
$t_{w(FP)}$	Pulse duration, FSYNC high or low		$1 / (2f_{DATA})$			$1 / (2f_{DATA})$		s
$t_{d(FSSC)}$	Delay time, FSYNC rising edge to SCLK falling edge			6			8	ns
$t_{c(SC)}$	SCLK period		$1 / (32f_{DATA})$			$1 / (32f_{DATA})$		s
$t_{w(SCHL)}$	Pulse duration, SCLK high or low		$1 / (64f_{DATA})$			$1 / (64f_{DATA})$		s
$t_{v(DO)}$	Valid time, SCLK rising edge to DOUT invalid	25			25			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK falling edge to DOUT driven			15			17	ns
$t_{p(FSDO)}$	Propagation delay time, FSYNC rising edge to DOUT MSB valid			12			15	ns

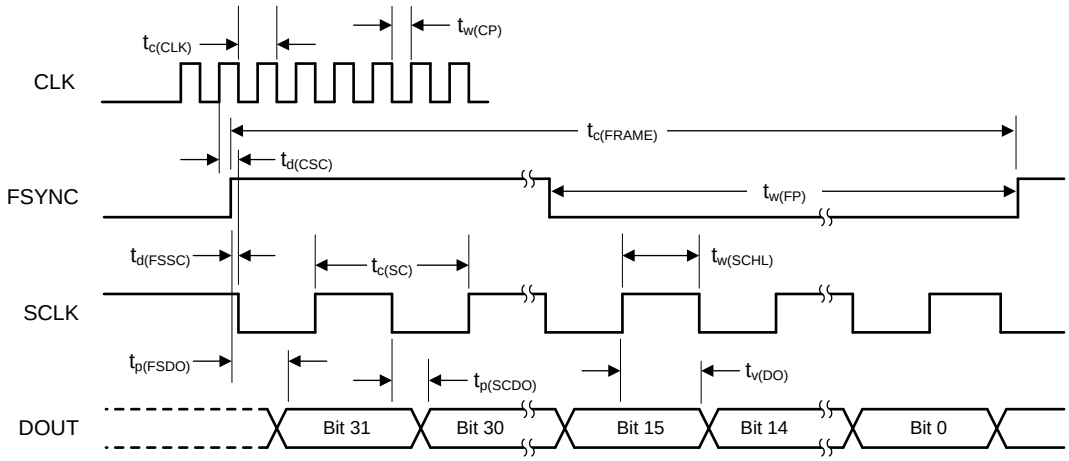


Figure 3. Frame-Sync Interface Timing Master Mode

6.10 Timing Requirements: Frame-Sync Slave Mode

over operating ambient temperature range (unless otherwise noted)

			2.8 V < DVDD ≤ 3.6 V			1.7 V ≤ DVDD ≤ 2.8 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(CLK)}$	Master clock period	HR mode	57		10,000	57		10,000	ns
		LP mode	114		10,000	114		10,000	
		VLP mode	227		10,000	227		10,000	
$t_{w(CP)}$	Pulse duration, Master clock high or low	HR mode	28		5,000	28		5,000	ns
		LP mode	56		5,000	56		5,000	
		VLP mode	112		5,000	112		5,000	
$t_{d(CSC)}$	Delay time, CLK rising edge to SCLK falling edge		2			2			ns
$t_{c(FRAME)}$	Frame period		1 / f_{DATA}			1 / f_{DATA}			s
$t_{w(FP)}$	Pulse durration, FSYNC high or low		2			2			t_{SCLK}
$t_{d(FSSC)}$	Delay time, FSYNC rising edge to SCLK falling edge				6			6	ns
$t_{d(SCFS)}$	Delay time, SCLK falling edge to FSYNC rising edge				2			2	ns
$t_{c(SC)}$	SCLK period		40			56			ns
$t_{w(SCHL)}$	Pulse duration, SCLK high or low		20			28			ns
DAISY-CHAIN TIMING									
$t_{su(DCI)}$	Setup time, DAISYIN valid before SCLK rising edge		8			8			ns
$t_{h(DCI)}$	Hold time, DAISYIN valid after SCLK rising edge		25			31			ns

6.11 Switching Characteristics: Frame-Sync Slave Mode

over operating ambient temperature range (unless otherwise noted)

		2.8 V < DVDD ≤ 3.6 V			1.7 V ≤ DVDD ≤ 2.8 V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{v(DO)}$	Valid time, SCLK rising edge to DOUT invalid	17			25			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK falling edge to valid new DOUT			22			22	ns
$t_{p(FSDO)}$	Propagation delay time, FSYNC rising edge to DOUT MSB valid		15	22		25	32	ns

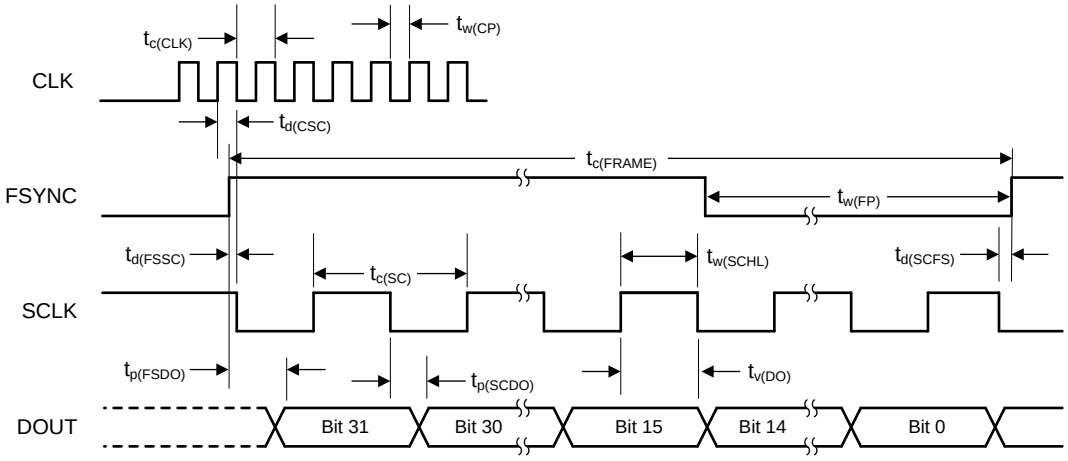


Figure 4. Frame-Sync Interface Timing Slave Mode

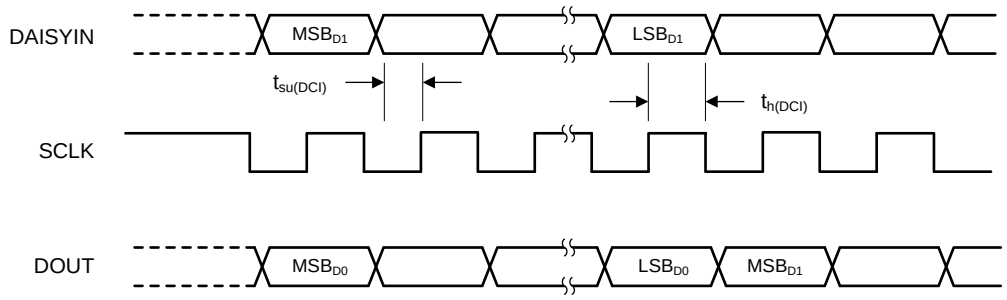
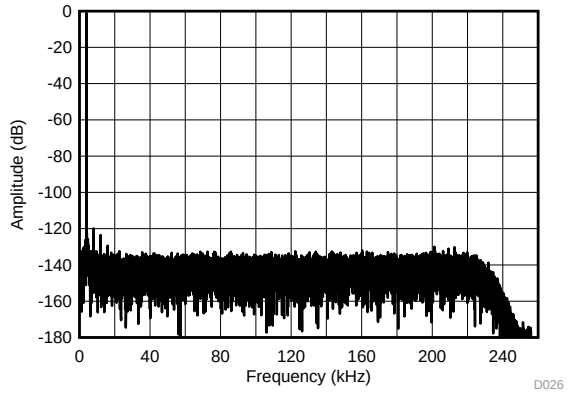


Figure 5. Frame-Sync Interface Slave Daisy-Chain Timing

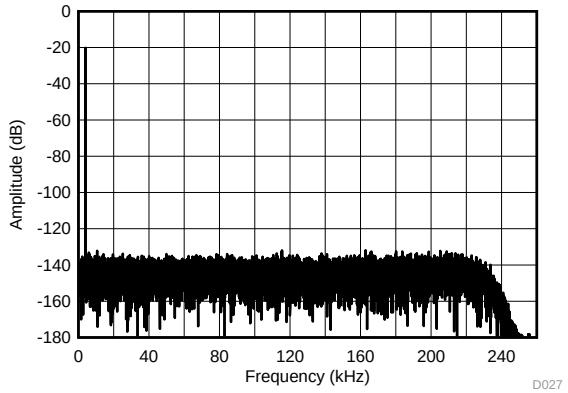
6.12 Typical Characteristics

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)



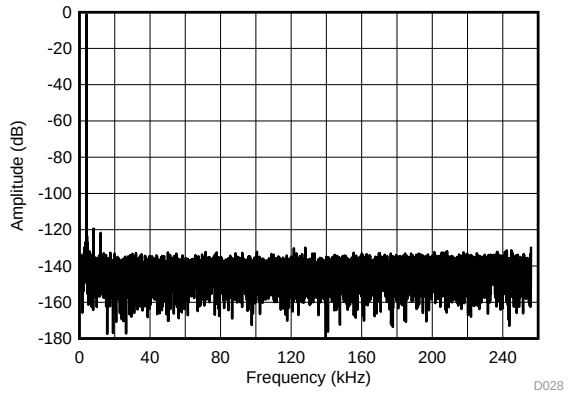
f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS, HR mode, WB2, 512 kSPS, 32768 samples

Figure 6. Output Spectrum



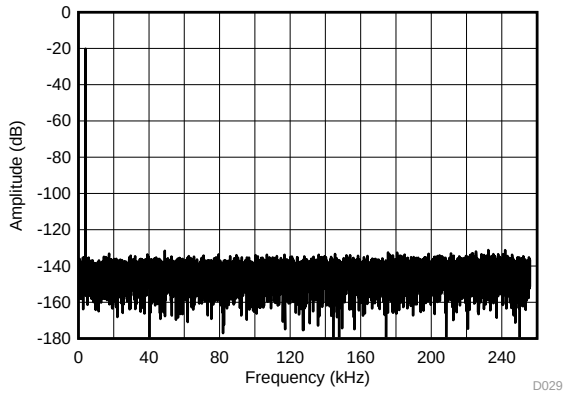
f_{IN} = 4 kHz, V_{IN} = –20 dBFS, HR mode, WB2, 512 kSPS, 32768 samples

Figure 7. Output Spectrum



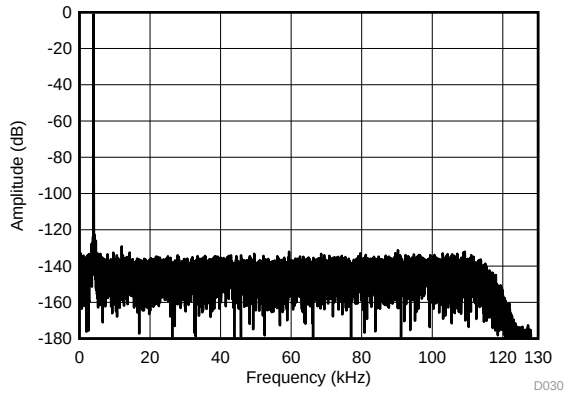
f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS, HR mode, WB1, 512 kSPS, 32768 samples

Figure 8. Output Spectrum



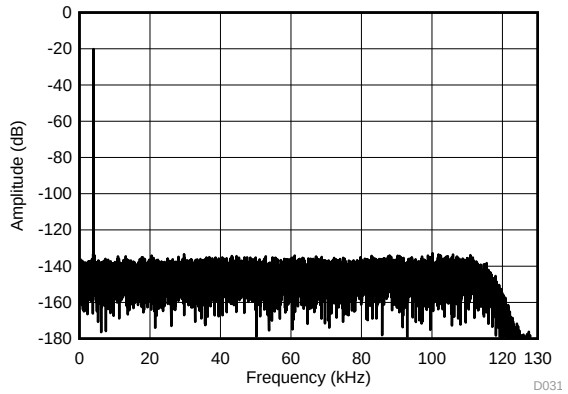
f_{IN} = 4 kHz, V_{IN} = –20 dBFS, HR mode, WB1, 512 kSPS, 32768 samples

Figure 9. Output Spectrum



f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS, LP mode, WB2, 256 kSPS, 32768 samples

Figure 10. Output Spectrum

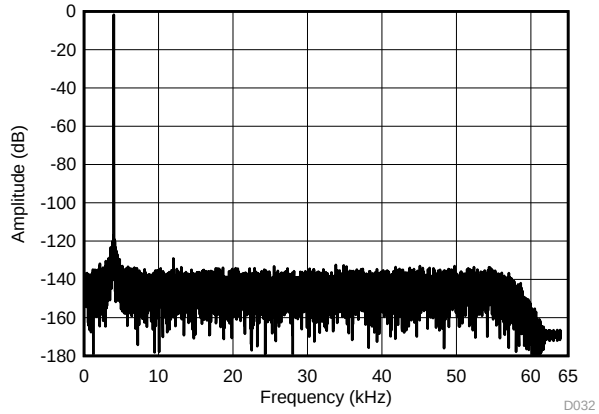


f_{IN} = 4 kHz, V_{IN} = –20 dBFS, LP mode, WB2, 256 kSPS, 32768 samples

Figure 11. Output Spectrum

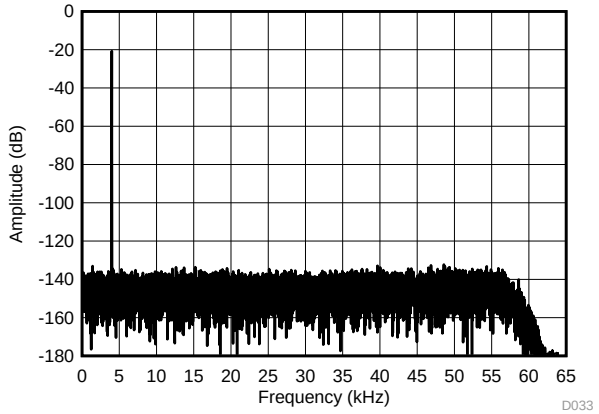
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)



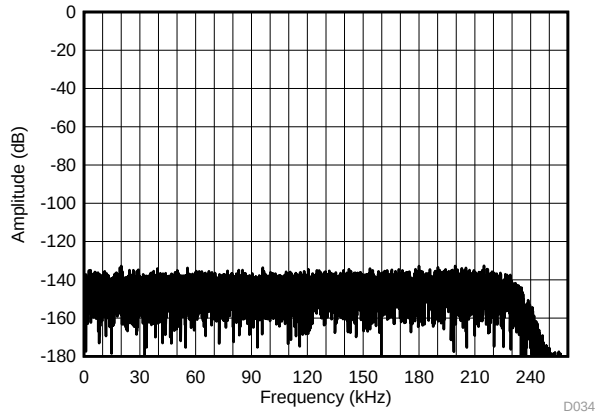
f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS, VLP mode, WB2, 128 kSPS, 32768 samples

Figure 12. Output Spectrum



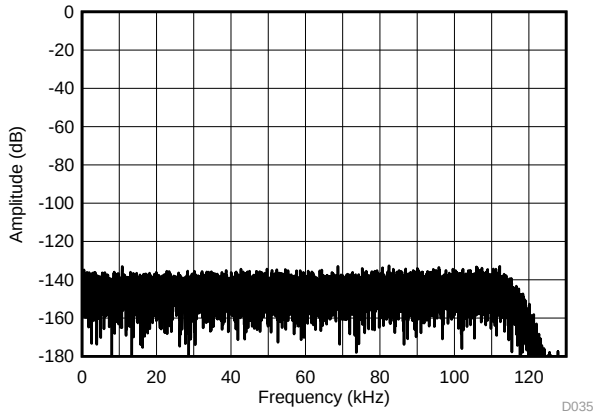
f_{IN} = 4 kHz, V_{IN} = –20 dBFS, VLP mode, WB2, 128 kSPS, 32768 samples

Figure 13. Output Spectrum



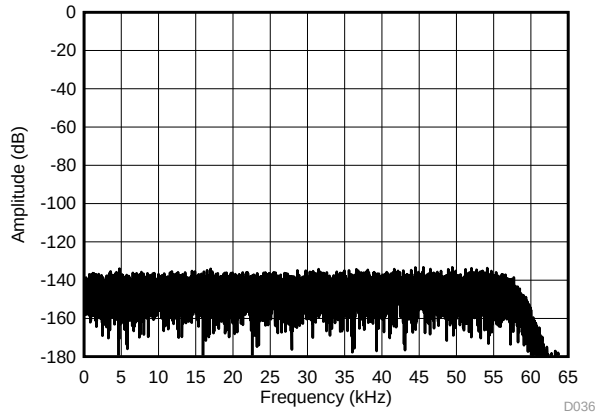
Inputs shorted, HR mode, WB2, 512 kSPS, 32768 samples

Figure 14. Output Spectrum



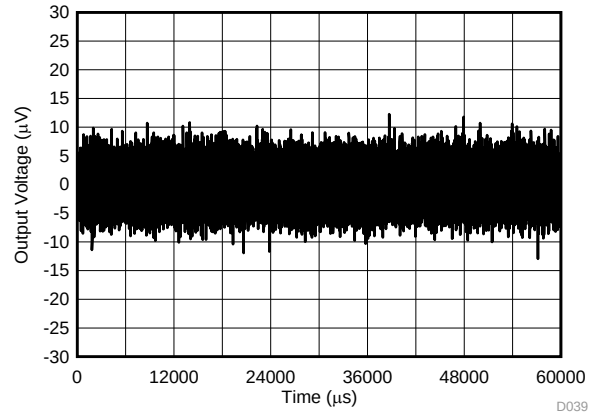
Inputs shorted, LP mode, WB2, 256 kSPS, 32768 samples

Figure 15. Output Spectrum



Inputs shorted, VLP mode, WB2, 128 kSPS, 32768 samples

Figure 16. Output Spectrum

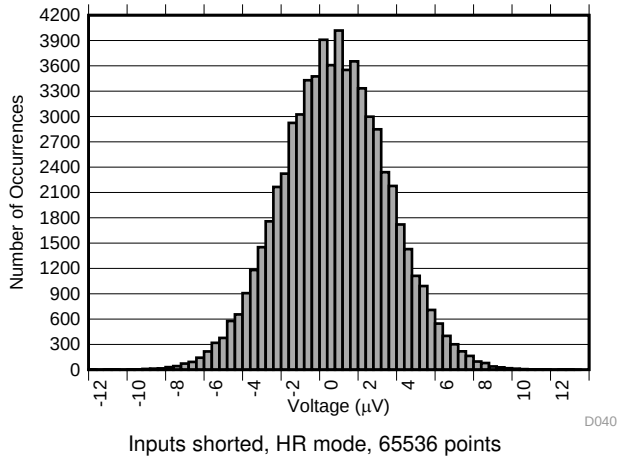


HR mode, 0.5 seconds data collection

Figure 17. ADC Conversion Noise

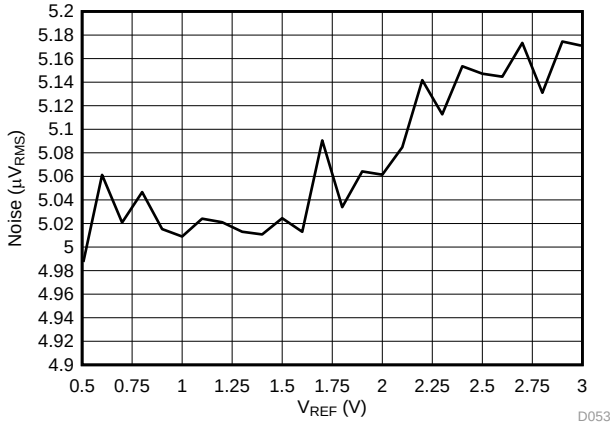
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)



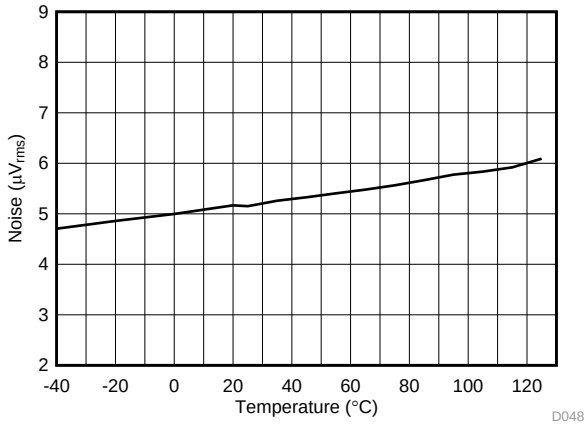
Inputs shorted, HR mode, 65536 points

Figure 18. Noise Histogram



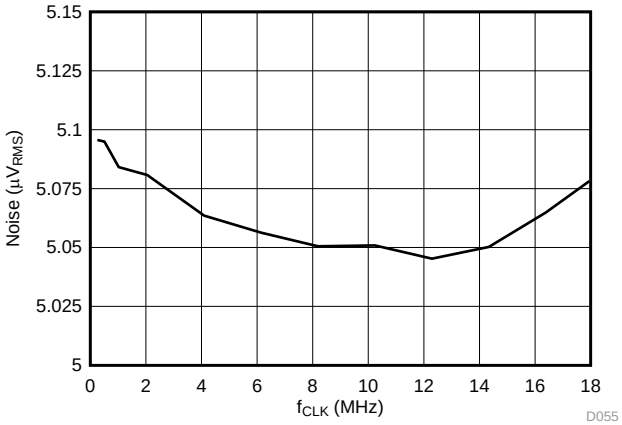
Inputs shorted, HR mode

Figure 19. Noise vs V_{REF}



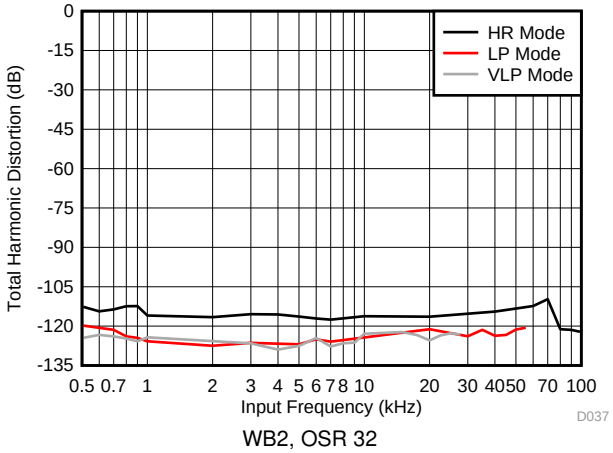
Inputs shorted

Figure 20. Noise vs Temperature



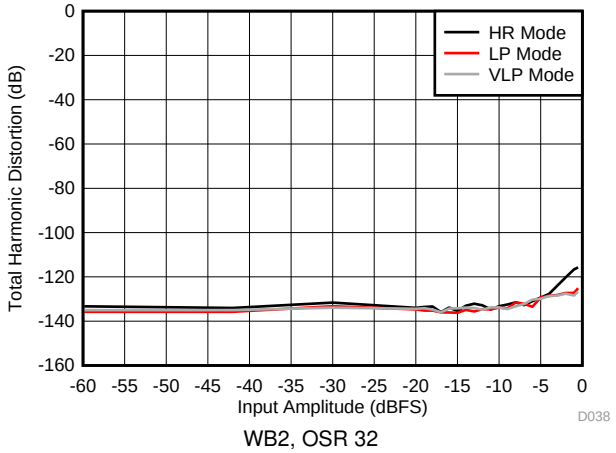
Inputs shorted, HR mode

Figure 21. Noise vs f_{CLK}



WB2, OSR 32

Figure 22. Total Harmonic Distortion vs f_{IN}

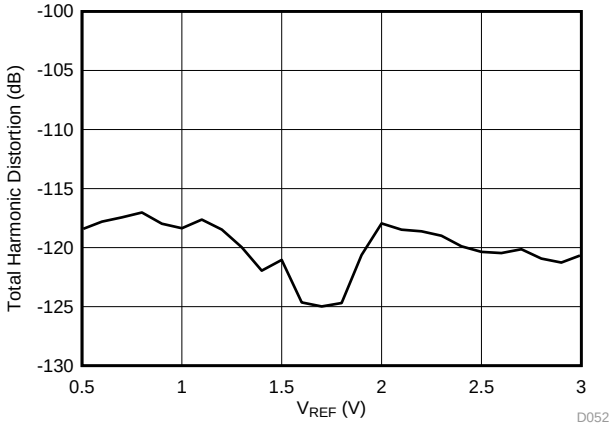


WB2, OSR 32

Figure 23. Total Harmonic Distortion vs V_{IN}

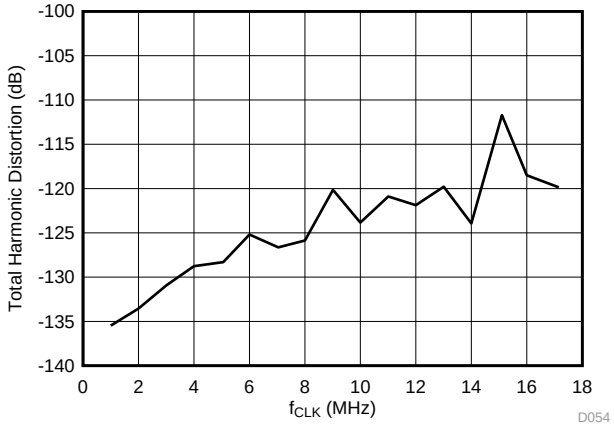
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)



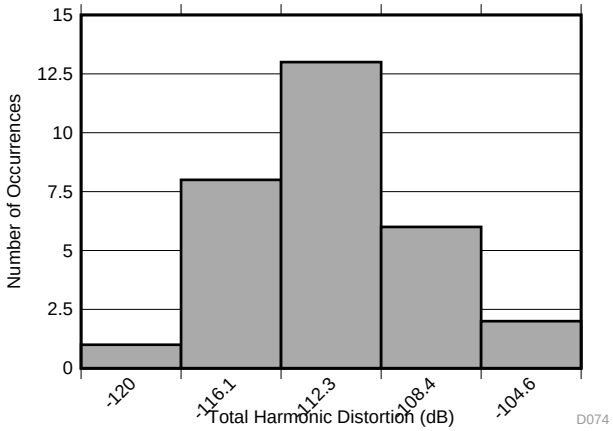
HR mode, f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS

Figure 24. Total Harmonic Distortion vs V_{REF}



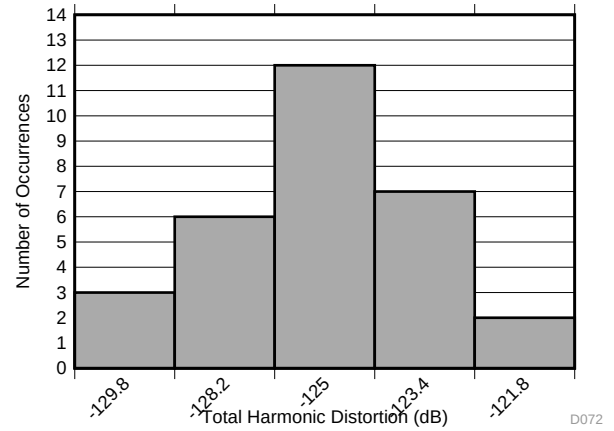
f_{IN} = 4 kHz, HR mode

Figure 25. Total Harmonic Distortion vs f_{CLK}



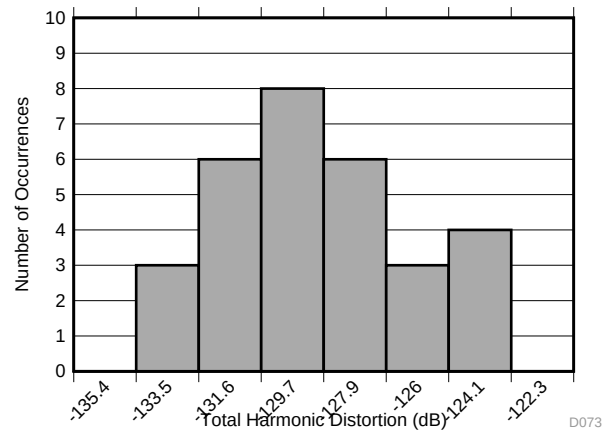
HR mode, f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS

Figure 26. Total Harmonic Distortion Histogram



LP mode, f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS

Figure 27. Total Harmonic Distortion Histogram



VLP mode, f_{IN} = 4 kHz, V_{IN} = –0.5 dBFS

Figure 28. Total Harmonic Distortion Histogram

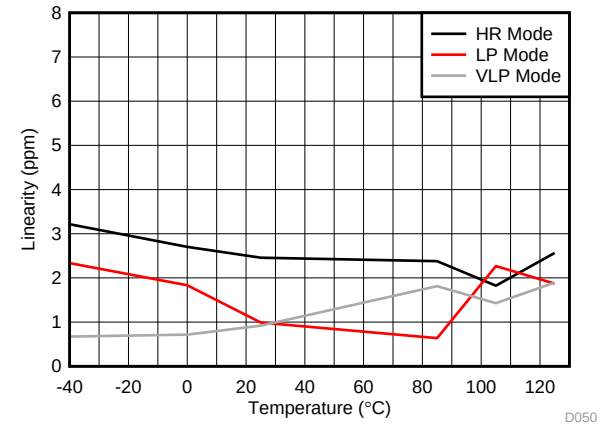


Figure 29. INL vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)

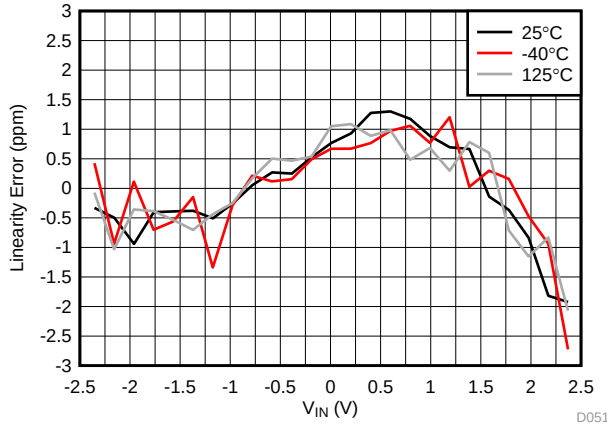


Figure 30. INL vs V_{IN}

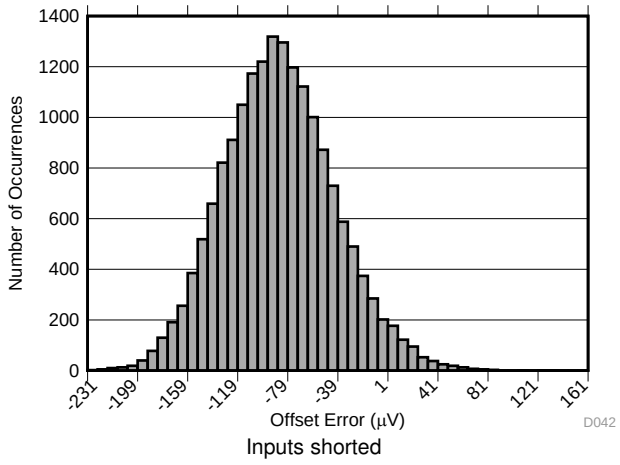


Figure 31. Offset Error Histogram

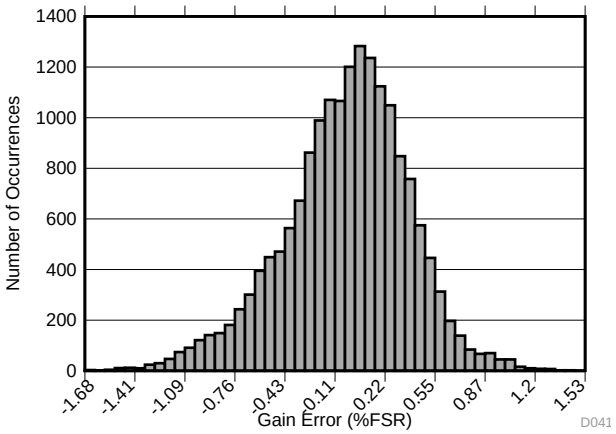


Figure 32. Gain Error Histogram

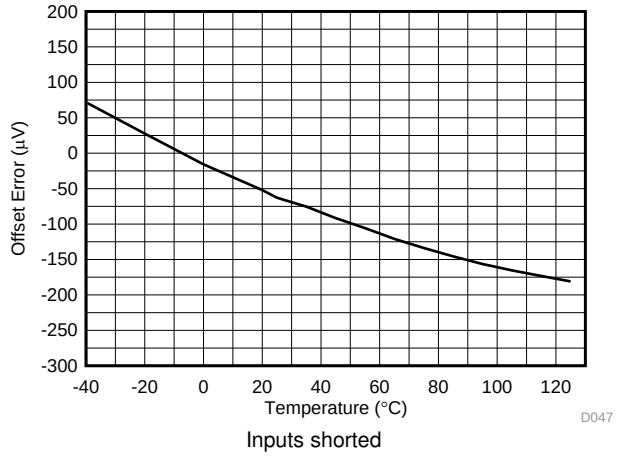


Figure 33. Offset Error vs Temperature

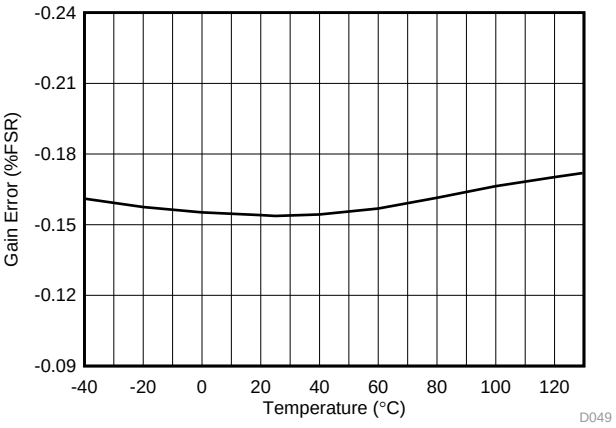


Figure 34. Gain Error vs Temperature

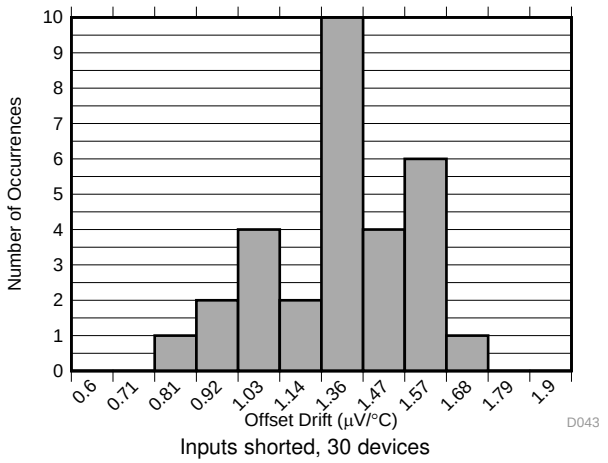


Figure 35. Offset Drift Histogram

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)

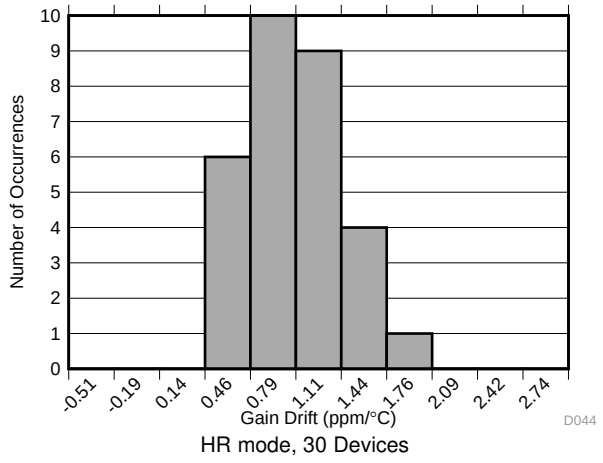


Figure 36. Gain Drift Histogram

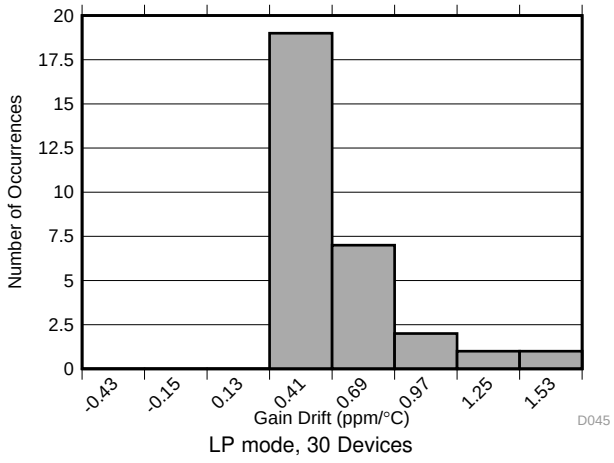


Figure 37. Gain Drift Histogram

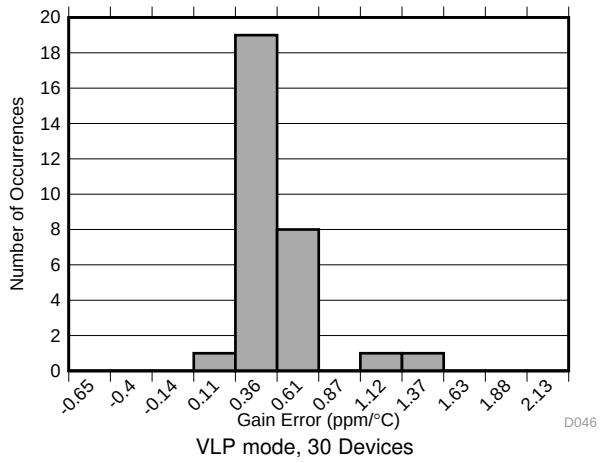


Figure 38. Gain Drift Histogram

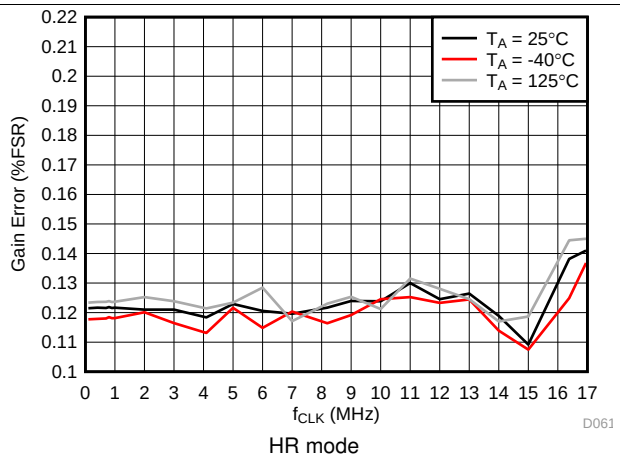


Figure 39. Gain Error vs f_{CLK}

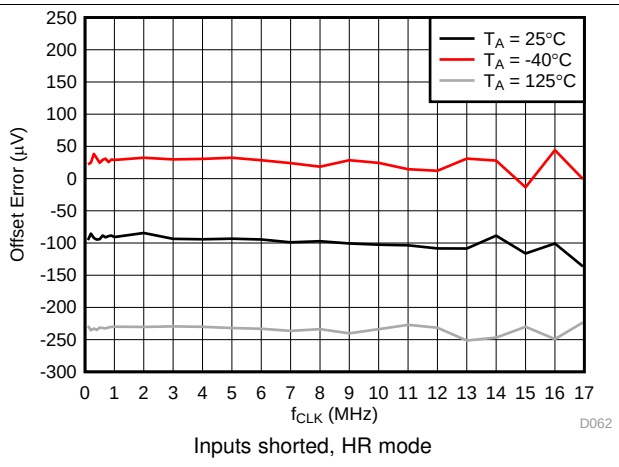


Figure 40. Offset Voltage vs f_{CLK}

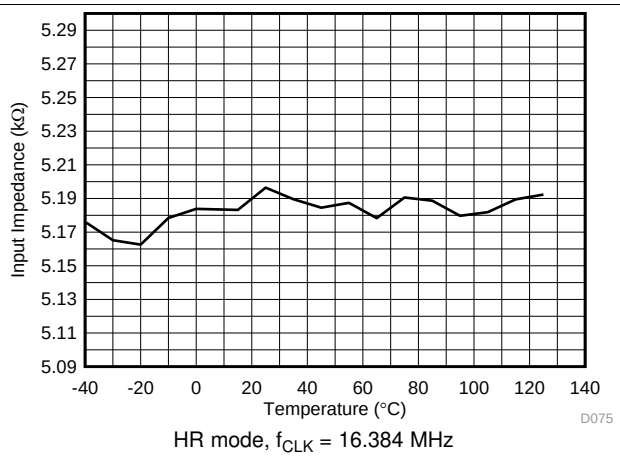
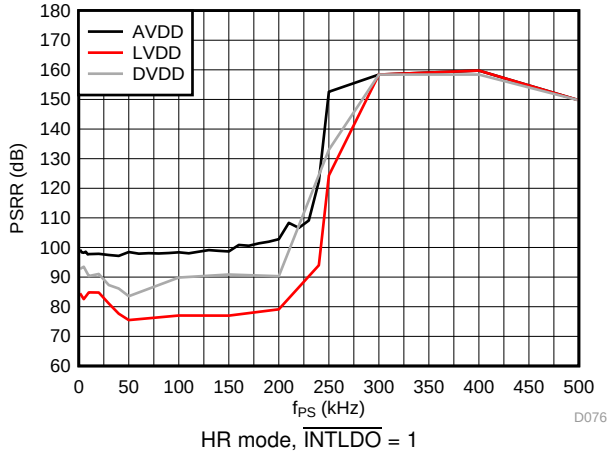


Figure 41. Differential Input Impedance vs Temperature

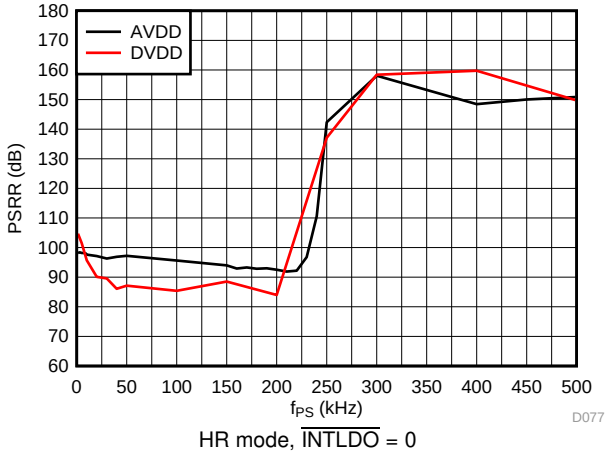
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)



HR mode, $\overline{INTLDO}$ = 1

Figure 42. PSRR vs Power-Supply Frequency



HR mode, $\overline{INTLDO}$ = 0

Figure 43. PSRR vs Power-Supply Frequency

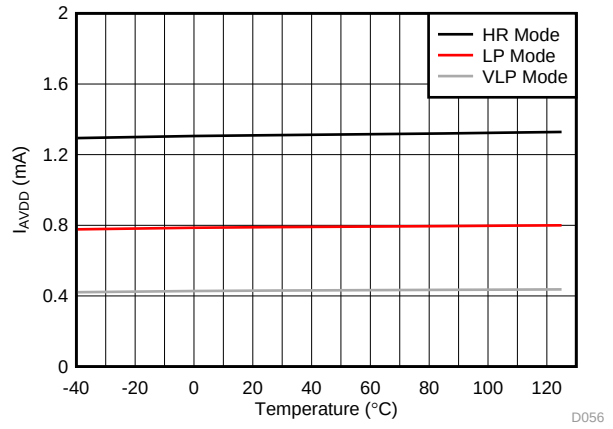


Figure 44. I_{AVDD} vs Temperature

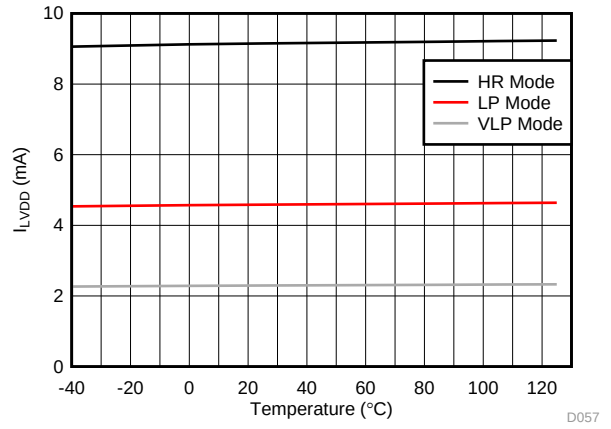


Figure 45. I_{LVDD} vs Temperature

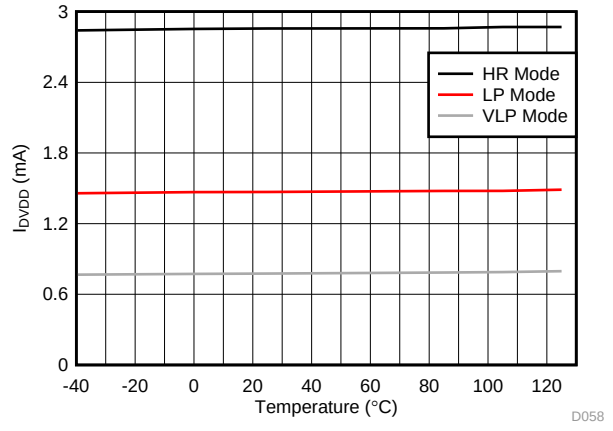


Figure 46. I_{DVDD} vs Temperature

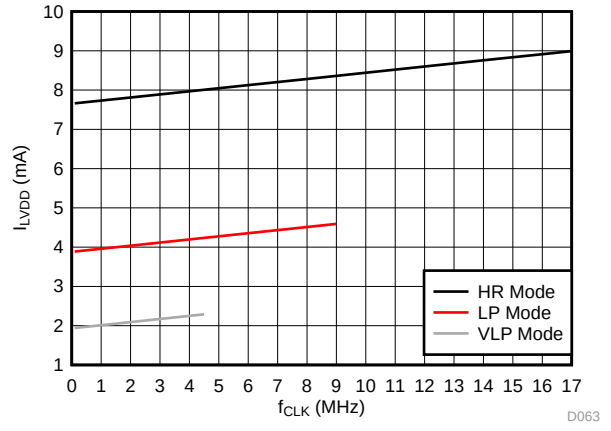
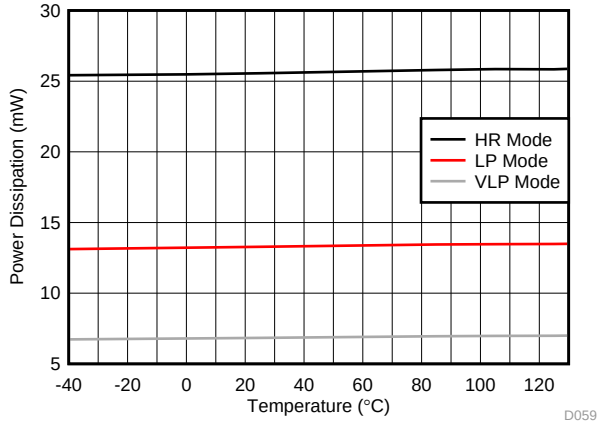


Figure 47. I_{LVDD} vs f_{CLK}

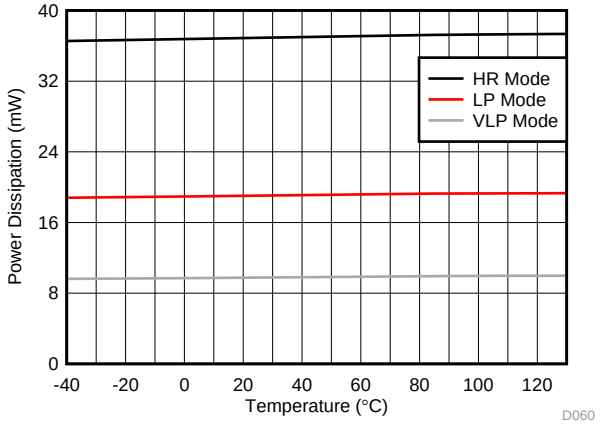
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)



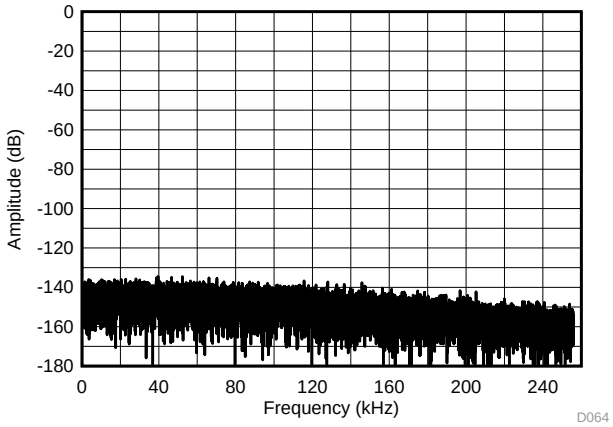
$\overline{INTLDO}$ = 1, LVDD = 1.8 V

Figure 48. Power Dissipation vs Temperature



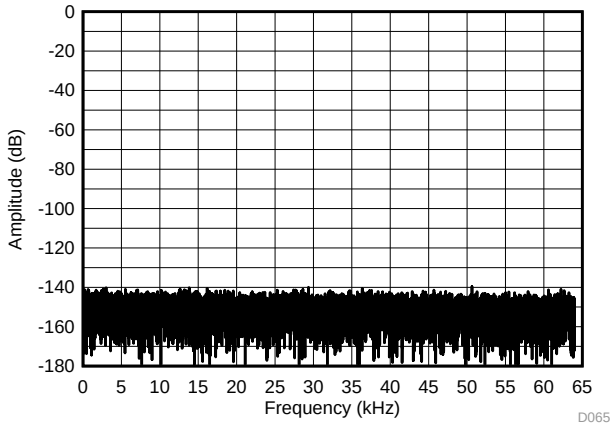
$\overline{INTLDO}$ = 0

Figure 49. Power Dissipation vs Temperature



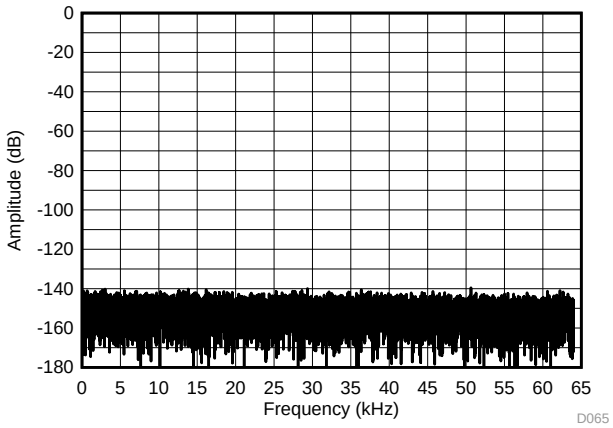
Inputs shorted, HR mode, LL, 512 kSPS, 32768 samples

Figure 50. Output Spectrum



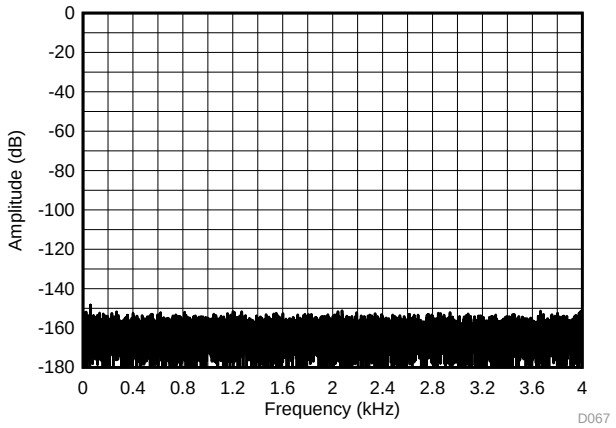
Inputs shorted, HR mode, LL, 128 kSPS, 32768 samples

Figure 51. Output Spectrum



Inputs shorted, HR mode, LL, 32 kSPS, 32768 samples

Figure 52. Output Spectrum

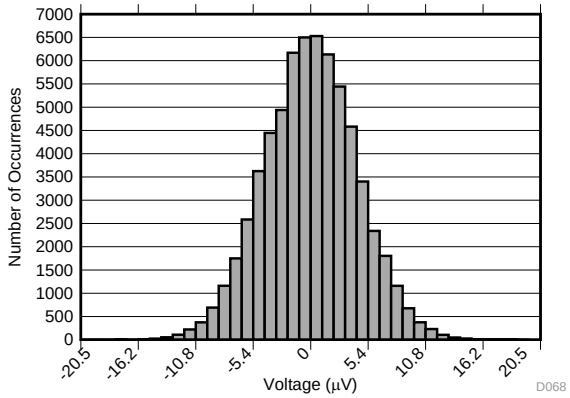


Inputs shorted, HR mode, LL, 8 kSPS, 32768 samples

Figure 53. Output Spectrum

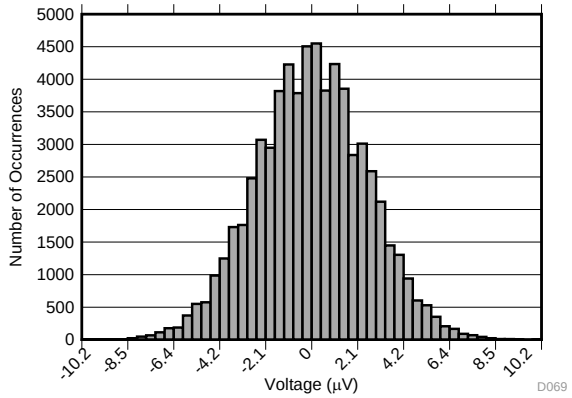
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, and external V_{REF} = 2.5 V (unless otherwise noted)



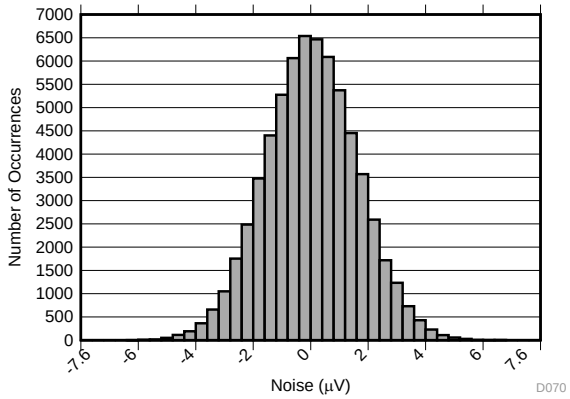
Inputs shorted, HR mode, LL, 512 kSPS, 32768 samples

Figure 54. Noise Histogram



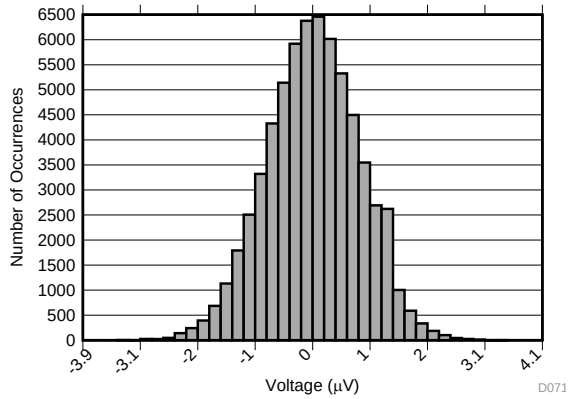
Inputs shorted, HR mode, LL, 128 kSPS, 32768 samples

Figure 55. Noise Histogram



Inputs shorted, HR mode, LL, 32 kSPS, 32768 samples

Figure 56. Noise Histogram



Inputs shorted, HR mode, LL, 8 kSPS, 32768 samples

Figure 57. Noise Histogram

7 Parameter Measurement information

7.1 Noise Performance

Adjust the oversampling ratio (OSR) to control the data rate and change the digital filter in order to optimize the noise performance of the ADS127L01. Hardware control pins offer four oversampling options and three selectable digital filter options to configure the ADC for a specific bandwidth of interest. When averaging is increased by reducing the data rate (increasing the OSR), the in-band noise drops as more samples from the modulator are averaged to yield one conversion result. Table 1 and Table 2 summarize the device noise performance across the various oversampling and digital filter options. Wideband 1 filter has a filter transition band of (0.45 to 0.55) f_{DATA}, and Wideband 2 filter has a filter transition band of (0.40 to 0.50) f_{DATA}. Data are representative of typical noise performance at T_A = 25°C with an external 2.5-V reference. Data shown are the result of one standard deviation of the readings with the inputs shorted together and biased to midsupply. A minimum of 1,000 consecutive readings are used to calculate the V_{RMS_noise} voltage noise for each measurement. Equation 1 is used to convert the noise in V_{RMS_noise} to SNR, and Equation 2 is used to convert the noise in V_{RMS_noise} to ENOB. The peak-to-peak noise for the Low-latency filter is defined as V_{PP_noise}.

$$SNR = 20 \times \log (V_{REF} \times 0.7071 / V_{RMS\_noise}) \quad (1)$$

$$ENOB = \ln (2 \times V_{REF} / V_{RMS\_noise}) / \ln (2) \quad (2)$$

Noise Performance (continued)

Table 1. Wideband Filters Performance Summary at AVDD = 3.0 V, DVDD = 1.8 V, and 2.5-V Reference

MODE	DATA RATE (SPS)	OSR	TRANSITION BAND	PASS BAND (kHz)	SNR (dB)	V_{RMS_noise} (μV_{RMS})	ENOB	I_{DVDD} (mA)
High-resolution (HR)	512,000	32	Wideband 1 filter	230.4	103.7	11.61	18.72	7.50
			Wideband 2 filter	204.8	104.1	10.64	18.84	
	256,000	64	Wideband 1 filter	115.2	107.3	7.61	19.33	4.35
			Wideband 2 filter	102.4	107.7	7.25	19.40	
	128,000	128	Wideband 1 filter	57.6	110.4	5.35	19.83	2.80
			Wideband 2 filter	51.2	110.9	5.06	19.91	
	64,000	256	Wideband 1 filter	28.8	113.4	3.79	20.33	2.00
			Wideband 2 filter	25.6	113.9	3.58	20.41	
Low-power (LP)	256,000	32	Wideband 1 filter	115.2	103.9	11.27	18.76	3.80
			Wideband 2 filter	102.4	104.7	10.31	18.89	
	128,000	64	Wideband 1 filter	57.6	107.6	7.38	19.37	2.25
			Wideband 2 filter	51.2	108.1	6.96	19.45	
	64,000	128	Wideband 1 filter	28.8	110.7	5.18	19.88	1.50
			Wideband 2 filter	25.6	111.1	4.95	19.95	
	32,000	256	Wideband 1 filter	14.4	113.7	3.67	20.38	1.10
			Wideband 2 filter	12.8	114.1	3.47	20.46	
Very-low-power (VLP)	128,000	32	Wideband 1 filter	57.6	104.1	11.01	18.79	1.95
			Wideband 2 filter	51.2	104.9	10.11	18.92	
	64,000	64	Wideband 1 filter	28.8	107.8	7.20	19.41	1.20
			Wideband 2 filter	25.6	108.3	6.80	19.49	
	32,000	128	Wideband 1 filter	14.4	110.9	5.07	19.91	0.80
			Wideband 2 filter	12.8	111.3	4.81	19.99	
	16,000	256	Wideband 1 filter	7.2	113.9	3.59	20.41	0.60
			Wideband 2 filter	6.9	114.3	3.41	20.48	

Table 2. Low-Latency Filter Performance Summary at AVDD = 3.0 V, DVDD = 1.8 V, and 2.5-V Reference

MODE	DATA RATE (SPS)	OSR	-3-dB BANDWIDTH (kHz)	SNR (dB)	V_{RMS_noise} (μV_{RMS})	ENOB	V_{PP_noise} (μV_{PP})	I_{DVDD} (mA)
High-resolution (HR)	512,000	32	101.8	107.6	7.40	19.37	64.67	1.60
	128,000	128	50.6	110.8	5.12	19.90	44.11	1.39
	32,000	512	13.7	116.2	2.74	20.80	24.14	1.33
	8,000	2048	3.5	122.0	1.41	21.76	11.32	1.32
Low-power (LP)	256,000	32	50.9	107.8	7.22	19.40	61.99	0.85
	64,000	128	25.3	111.0	4.97	19.94	46.79	0.75
	16,000	512	6.9	116.5	2.65	20.85	22.05	0.73
	4,000	2048	1.7	122.2	1.37	21.80	10.73	0.72
Very-low-power (VLP)	128,000	32	25.5	108.1	6.97	19.45	65.57	0.50
	32,000	128	12.7	111.3	4.80	19.99	39.64	0.44
	8,000	512	3.4	116.7	2.57	20.89	20.27	0.41
	2,000	2048	0.9	122.4	1.34	21.83	10.73	0.40

8 Detailed Description

8.1 Overview

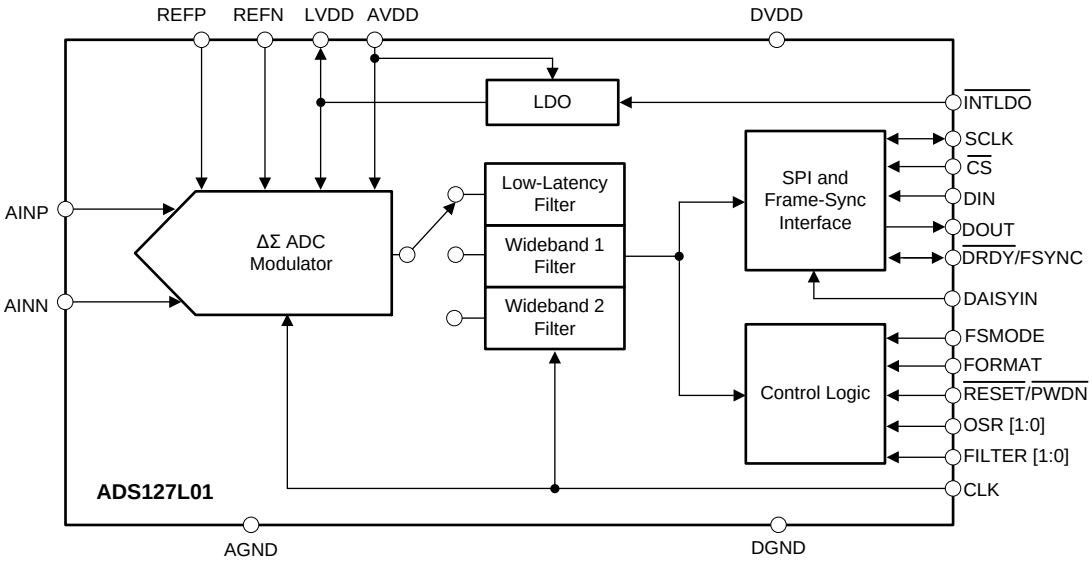
The ADS127L01 is a 24-bit delta-sigma (ΔΣ) ADC that offers a combination of excellent dc accuracy and ac performance. The flexible digital-filter options make it suitable for both dc and ac applications. The device is hardware programmable, making it easy to configure for a variety of applications without the need to program any registers.

The *Functional Block Diagram* shows the main internal features of the ADS127L01. The converter is comprised of a third-order, chopper-stabilized, delta-sigma modulator, that measures the differential input signal, $V_{IN} = (V_{AINP} - V_{AINN})$, against the differential reference, $V_{REF} = (V_{REFP} - V_{REFN})$. The converter core consists of a differential, switched-capacitor, delta-sigma modulator followed by a selectable digital filter. The digital-filter low-latency path uses a cascaded combination of a fifth-order sinc and a first-order sinc filter, ideal for applications requiring fast response time or systems using a multiplexed input. Two wide-bandwidth paths (Wideband 1 and Wideband 2) are also available, providing outstanding frequency response with very low pass-band ripple, a steep-transition band, and high stop-band attenuation. The ADS127L01 provides two selectable options for transition-band frequency. The Wideband-filter paths are suited for applications that require high-resolution measurements of high-frequency, ac-signal content. To allow tradeoffs among speed, resolution, and power, three operating modes are supported: high-resolution (HR), low-power (LP), and very-low-power (VLP).

In HR mode, SNR = 104.4 dB (V_{REF} = 2.5 V) at a maximum data rate of 512 kSPS. At this data rate, the power dissipation is only 35 mW, and scales with master clock frequency. In LP mode, the maximum data rate is 256 kSPS, while consuming only 19 mW of power. In VLP mode, the maximum data rate is 128 kSPS, while consuming only 9 mW of power.

Configure the ADS127L01 by setting the appropriate hardware I/O pins. Registers are available for gain and offset calibrations. Three interface communication modes are available, providing flexibility for convenient interfacing to microcontrollers, DSPs, or FPGAs. SPI, frame-sync slave, or frame-sync master communication modes are hardware selectable on the device. The ADS127L01 has a daisy-chain output available, and can synchronize externally to another device or system using the START signal. The daisy-chain configuration allows the device to be used conveniently in systems that require multiple channels.

8.2 Functional Block Diagram



8.3 Feature Description

This section discusses the details of the ADS127L01 internal functional elements. Throughout this document, f_{CLK} denotes the frequency of the signal at the CLK pin, t_{CLK} denotes the period of the signal at the CLK pin, f_{DATA} denotes the output data rate, and t_{DATA} denotes the time period of the output data.

8.3.1 Analog Inputs (AINP, AINN)

The ADS127L01 measures the differential input signal $V_{IN} = (V_{AINP} – V_{AINN})$ against the differential reference $V_{REF} = (V_{REFP} – V_{REFN})$. The most positive measurable differential input is $+V_{REF}$ and the most negative measurable differential input is $–V_{REF}$.

For optimum performance, drive the ADS127L01 inputs differentially, centered around a common-mode voltage of AVDD / 2. Alternatively, if the signal is of pseudo-differential nature, the negative input can be held at a constant voltage other than 0 V (typically AVDD / 2), and the voltage on the positive input can change. Figure 58 and Figure 59 show examples of both fully-differential and pseudo-differential signals, respectively.

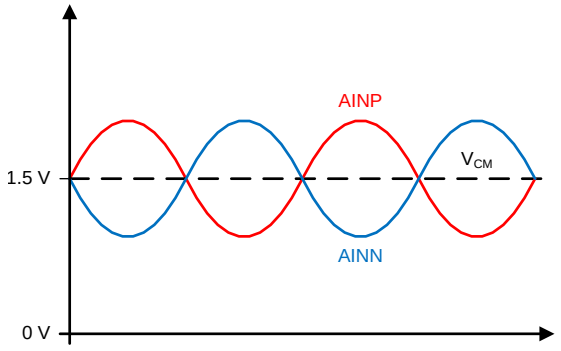


Figure 58. Fully-Differential Input Signal

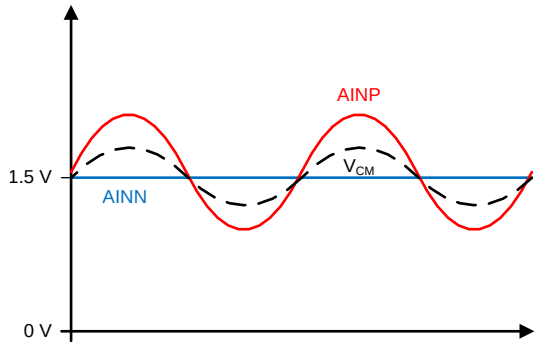


Figure 59. Pseudo-Differential Input Signal

Electrostatic discharge (ESD) diodes to AVDD and AGND protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by Equation 3:

$$AGND – 0.3\ V < V_{AINx} < AVDD + 0.3\ V \quad (3)$$

The analog input pins, AINP and AINN, at the front end of the converter are connected directly to the switched-capacitor sampling network to measure the input voltage. Figure 60 shows a conceptual diagram of the modulator circuit charging and discharging the sampling capacitor through switches, although the actual implementation is slightly different. The sampling time (t_{CLK} / 2) is equivalent to half the master clock period, and is the inverse of the modulator sampling frequency.

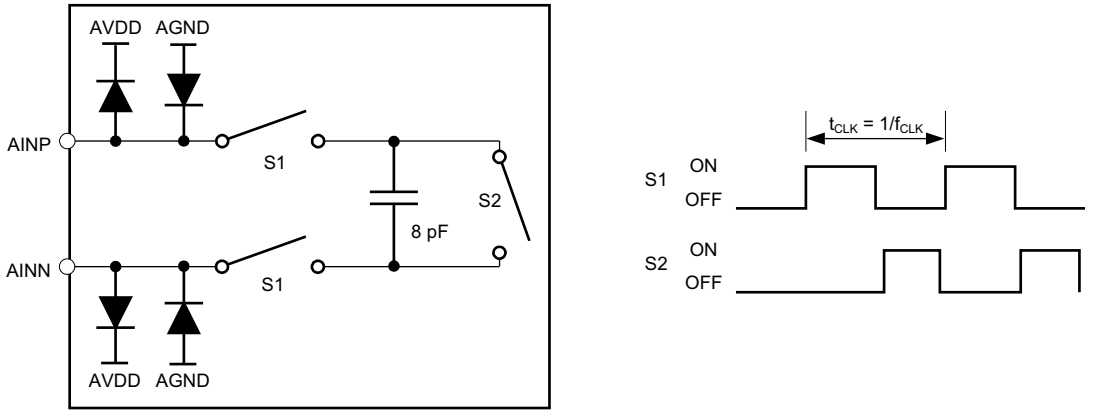


Figure 60. Equivalent Analog Input Circuitry

Feature Description (continued)

The average load presented by the switched-capacitor input can be modeled with an effective differential impedance, as shown in Figure 61. The effective impedance is a function of the modulator clock, and is equal to the master clock, f_{CLK}. The ADS127L01 samples the input at very high speeds, and does not include an integrated buffer; a suitable driver must be used. See the Application and Implementation section for recommended driver circuit designs.

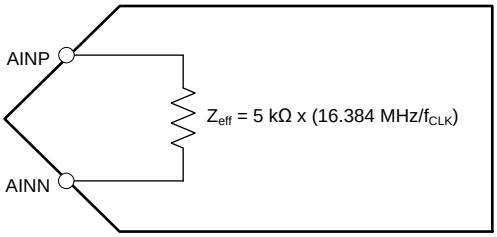


Figure 61. Effective Input Impedance

The ADC sampling network is connected to a delta-sigma modulator used to convert the analog input voltage into a data bit stream. The modulator is third-order, with a multibit quantizer that runs at the modulator clock frequency, f_{MOD}, equal to the master clock frequency, f_{CLK}.

8.3.2 Digital Filter

The ADS127L01 offers three selectable digital filters to perform both filtering and decimation of the digital data stream coming from the modulator. The oversampling ratio (OSR) and digital-filter selection sets the overall frequency response for the data converter. The available filter options for the ADS127L01 are:

- Low-latency sinc filter (LL)
- Wideband finite impulse response (FIR) filter with a transition band of (0.45 to 0.55) × f_{DATA} (WB1)
- Wideband finite impulse response (FIR) filter with a transition band of (0.40 to 0.50) × f_{DATA} (WB2)

Use the hardware FILTER[1:0] pins shown in Table 11. Each filter has four OSR options (the ratio of the modulator sampling to the output data rate, or f_{MOD} / f_{DATA}), shown in Table 12, that are selectable through hardware OSR[1:0] pins. The low-latency sinc filter is a cascaded sinc5 and sinc1 filter, and provides OSR options to achieve data rates ranging from 8 kSPS to 512 kSPS when operating from a 16.384-MHz master clock. The two Wideband filters use a multistage FIR topology to provide linear phase response with very low pass-band ripple and high stop-band attenuation. Wideband filters 1 and 2 provide four OSRs to achieve data rates ranging from 64 kSPS to 512 kSPS when operating from a 16.384-MHz master clock.

Select the filter and data rate when START is low, or take the START or $\overline{\text{RESET}}/\overline{\text{PWDN}}$ pin low and back high after a filter-path or data-rate change. If software commands are used to control conversions, use the STOP and START commands after a change to the filter path selection or the data rate. If a conversion is in process during a filter-path or data-rate change, the output data are not valid and must be discarded.

8.3.2.1 Low-Latency Filter

The low-latency sinc filter consists of two stages: a fixed-decimation, sinc5 filter, followed by a variable-decimation, sinc1 filter. The first-stage, sinc5 digital filter decimates by a fixed value of 32. When using OSR 32, the first-stage digital filter bypasses the second filter stage, and has a sinc5 frequency response profile. The second digital-filter stage provides an additional decimation of 4, 16, or 64 to create overall decimation options of 128, 512, and 2048. Together, the two stages create four selectable, Low-latency, filter data rates when operated from a 16.384-MHz clock: 512 kSPS, 128 kSPS, 32 kSPS, and 4 kSPS.

8.3.2.1.1 Low-Latency Filter Frequency Response

The low-pass filtering effect of the sinc filter sets the overall frequency response of the ADC when in low-latency filter mode. The frequency response of OSR 32 is from only the sinc5 filter stage. The frequency response of OSR 128, 512, or 2048 is the product of the sinc5 first-stage and sinc1 second-stage frequency responses. The overall filter response is given in Equation 4:

Feature Description (continued)

$$\left|H_{(f)}\right| = \left|H_{sinc^5}(f)\right| \times \left|H_{sinc^1}(f)\right| = \left|\frac{\sin\left[\frac{32\pi f}{f_{CLK}}\right]}{32 \times \sin\left[\frac{\pi f}{f_{CLK}}\right]}\right|^5 \times \left|\frac{\sin\left[\frac{32N\pi f}{f_{CLK}}\right]}{N \times \sin\left[\frac{32\pi f}{f_{CLK}}\right]}\right| \quad (4)$$

where

- f = signal frequency
- f_{CLK} = ADC master clock frequency = ADC modulator clock frequency
- N = Second-stage oversampling = 1 (OSR 32), 4 (OSR 128), 16 (OSR 512), or 64 (OSR 2048)

The inherent nature of the sinc filter response begins to attenuate frequencies as the signal moves away from dc. The pass band droop for inband ac signals makes the low-latency filter less ideal for ac signals.

As shown in Figure 62 and Figure 63, when OSR is set to 32, the digital filter frequency response follows a sinc5 transfer function with nulls occurring at f_{DATA} and at multiples thereof. At the null frequencies, the filter has zero gain. Convert the x-axis from the data rate, f_{DATA}, to terms of the master clock, f_{CLK}, by using Equation 5:

$$f_{DATA} = f_{CLK} / OSR \quad (5)$$

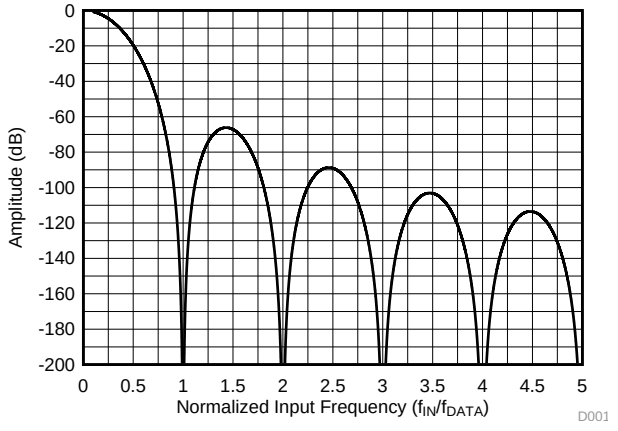


Figure 62. Low-Latency Filter Frequency Response (OSR 32)

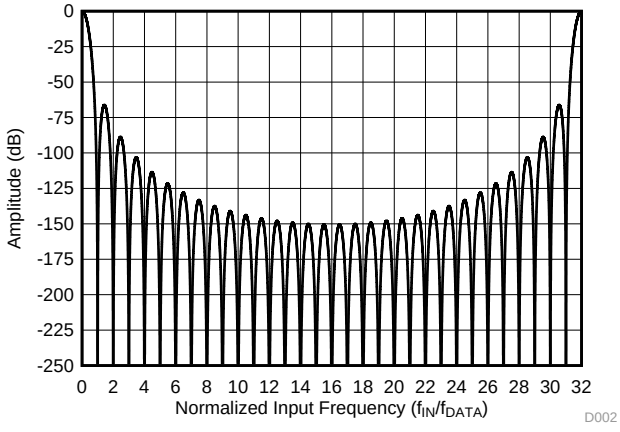


Figure 63. Low-Latency Filter Frequency Response (OSR 32) to f_{CLK}

Adjust the digital-filter response by changing the OSR or the master clock, f_{CLK}. Noise tradeoffs are made with signal bandwidth and filter latency.

Selecting an OSR other than 32 superimposes new nulls from the second-stage sinc1 filter over the nulls produced by the sinc5 stage. The end result is a combined frequency response from a sinc5 function at OSR 32 with nulls created from the sinc1 second stage at f_{DATA} and multiple thereof.

Figure 64 and Figure 65 illustrate the normalized frequency response of the Low-latency filter across all four OSR settings. OSR 32 follows a sinc5 frequency response, as highlighted in Figure 62. OSR 128, OSR 512, and OSR 2048 show a combined sinc5 and sinc1 response.

Figure 66, Figure 67, and Figure 68 illustrate the frequency response of OSR 128, OSR 512, and OSR 2048, respectively.

The Low-latency filter uses a multiple-stage, linear-phase, digital filter. Linear-phase filters exhibit constant delay time versus input frequency (also known as constant group delay). This feature of linear phase filters means that the time delay from any instant of the input signal to the corresponding same instant of the output data is constant and independent of the input-signal frequency. This behavior results in essentially zero phase error when measuring multitone signals.

Feature Description (continued)

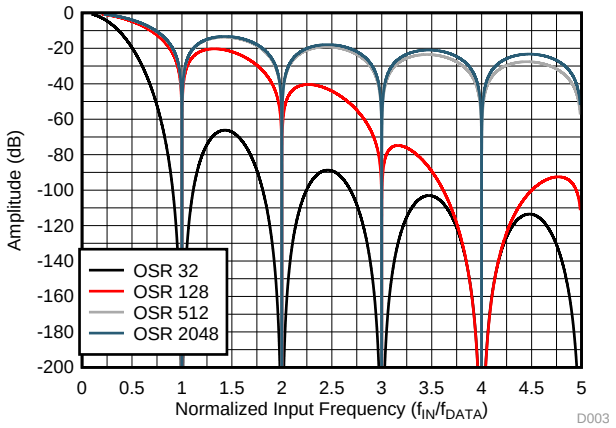


Figure 64. Low-Latency Filter Frequency Response

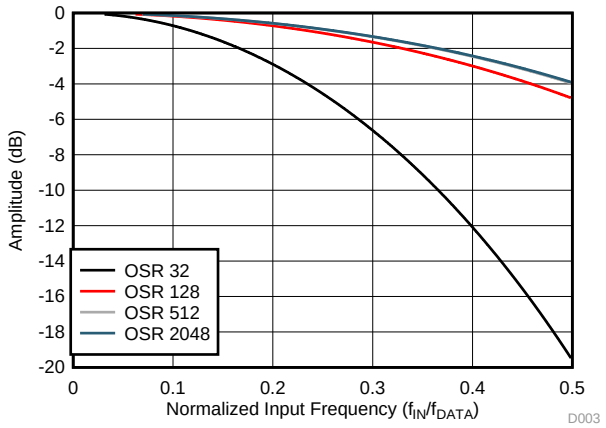


Figure 65. Low-Latency Filter Frequency Response to 0.5 × f_{IN} / f_{DATA}

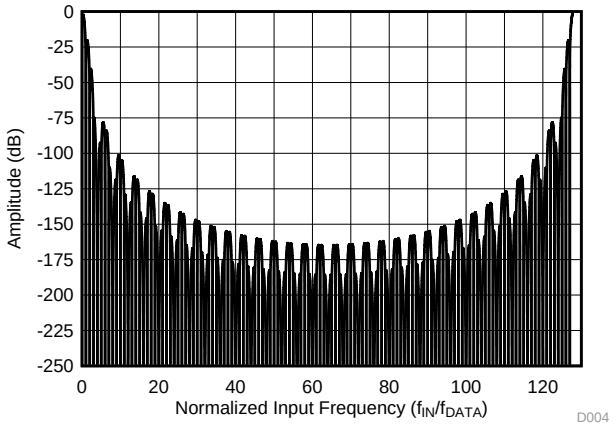


Figure 66. Low-Latency Filter Frequency Response (OSR 128) to f_{CLK}

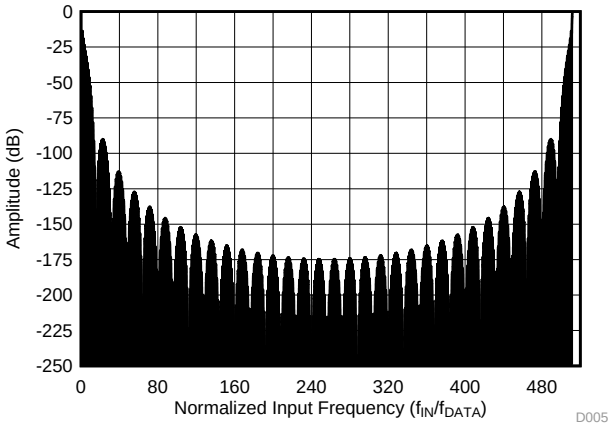


Figure 67. Low-Latency Filter Frequency Response (OSR 512) to f_{CLK}

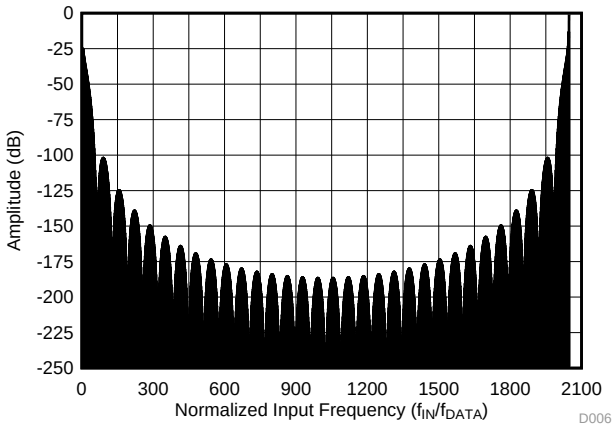


Figure 68. Low-Latency Filter Frequency Response (OSR 2048) to f_{CLK}

Feature Description (continued)

8.3.2.1.2 Low-Latency Filter Settling Time

The Low-latency filter takes several conversion cycles to provide fully-settled data following a START pin low-to-high transition or a START command. The OSR setting determines the exact number of conversion cycles for first new available data, as shown in Table 3. In SPI mode, the $\overline{\text{DRDY}}$ signal remains high until settled data are available. After settled data are available, a high-to-low transition on $\overline{\text{DRDY}}$ takes place. In frame-sync mode, DOUT shifts zeroes until settled data are available. Figure 69 shows the relationship between START to the first settled available data for SPI and frame-sync interface mode. See the *Start Pin (START)* section for exact timing for the START pin to first available data.

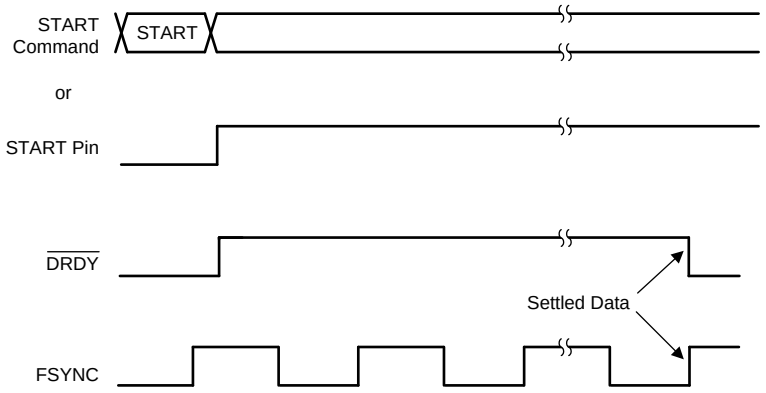


Figure 69. START to First Available Data

When applying an asynchronous step input to a converting ADS127L01, the output shift register does not gate data during digital-filter settling. The step-input-setting timing diagram shown in Figure 70 illustrates the converter step response with an asynchronous step input. The time that the analog input must be stable varies depending on the OSR. Table 3 summarizes the settling time of the Low-latency filter when a step input is applied to the input.

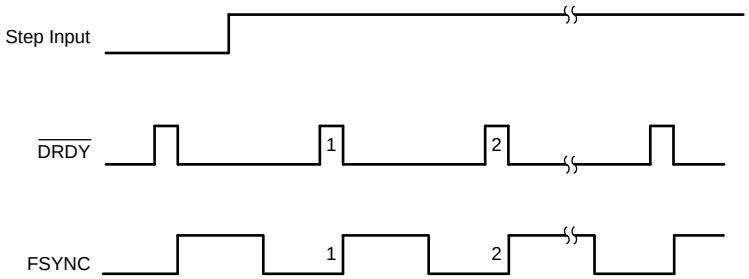


Figure 70. Asynchronous Step-Input Settling Time

Table 3. Low-Latency Filter Settling Time (Conversion Latency)

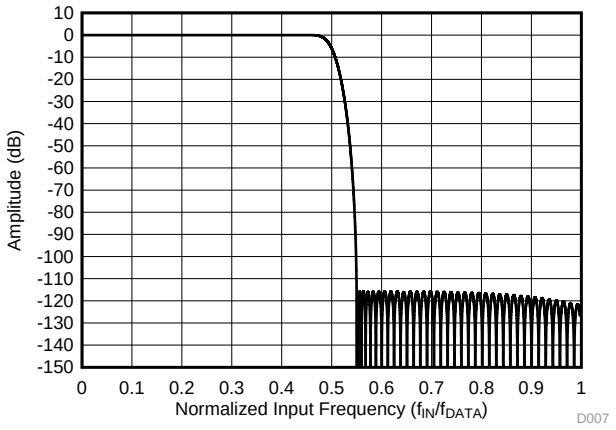
OSR	SETTLING TIME FROM START (t_{CLK} Periods)	INPUT SETTLING ($\overline{\text{DRDY}}$ or FSYNC Pulses)
32	160	5
128	288	3
512	672	2
2048	2208	2

8.3.2.2 Wideband Filter

The two Wideband filters use a multistage FIR topology to provide linear phase response with minimal pass-band ripple and high stop-band attenuation. The filters are well suited for measuring high-frequency ac signals while still maintaining excellent dc accuracy. Both Wideband filter options offer the same four OSR options; 32, 64, 128, and 256. The difference is in the transition band. When these four OSRs are paired with a 16.384-MHz clock, four selectable Wideband filter data rates are created: 512 kSPS, 256 kSPS, 128 kSPS, and 64 kSPS.

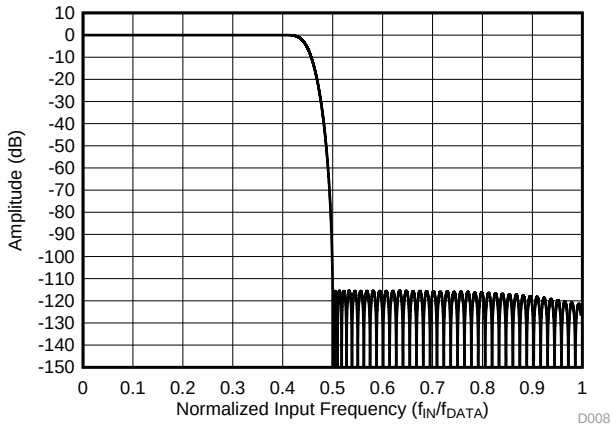
8.3.2.2.1 Wideband Filters Frequency Response

Figure 71 shows the frequency response of the Wideband 1 filter with a transition band of (0.45 to 0.55) × f_{DATA} normalized to the output data rate, f_{DATA}. Figure 72 shows the frequency response of the Wideband 2 filter with a transition band of (0.40 to 0.50) × f_{DATA} normalized to the output data rate, f_{DATA}. These plots are valid for all of the data rates available on the ADS127L01. Substitute the selected data rate, f_{DATA} (calculated using Equation 5), to express the x-axis in absolute frequency. Figure 73 overlaps the transition band of the Wideband 1 and Wideband 2 filters, showing the difference in frequency response. The Wideband 2 filter frequency response is designed to attenuate out-of-band signals more than –116 dB by the Nyquist frequency (0.5 × f_{DATA}) to reduce the effects of aliasing near the transition band.



FILTER[1:0] = 00

Figure 71. Wideband 1 Filter Frequency Response



FILTER[1:0] = 01

Figure 72. Wideband 2 Filter Frequency Response

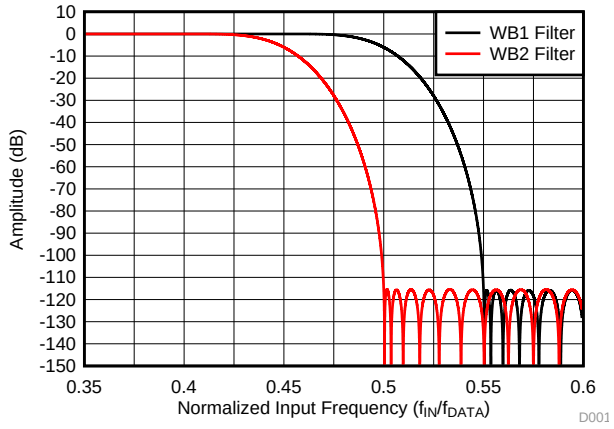
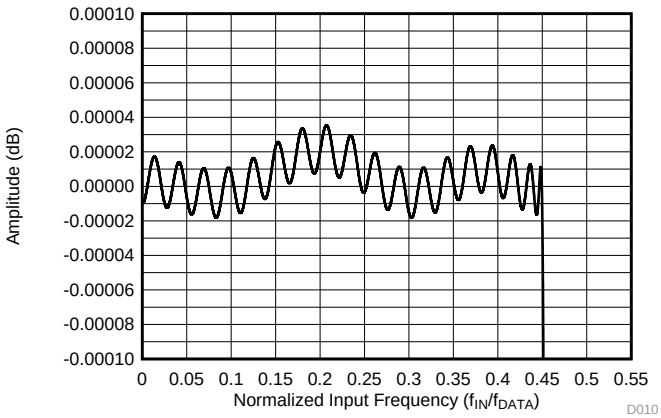


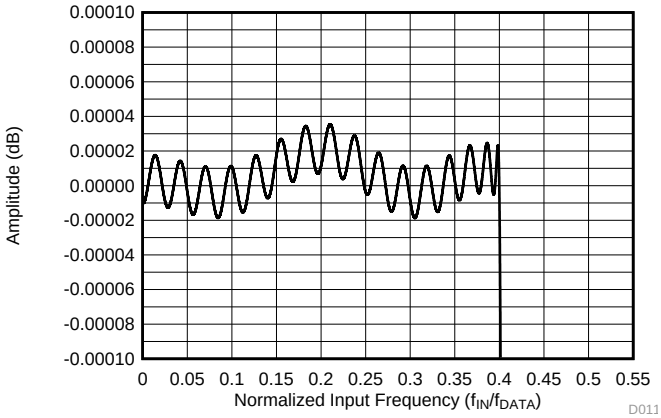
Figure 73. Wideband Filters Transition Band

The pass-band ripple for the two digital filters are shown in Figure 74 and Figure 75.



FILTER[1:0] = 00

Figure 74. Pass Band Ripple for Wideband 1 Filter



FILTER[1:0] = 01

Figure 75. Pass Band Ripple for Wideband 2 Filter

The overall frequency response repeats at the modulator sampling rate, which is the same as the input clock frequency, f_{CLK}. Figure 76 shows the response with the fastest data rate selected (512 kSPS when f_{CLK} = 16.384 MHz).

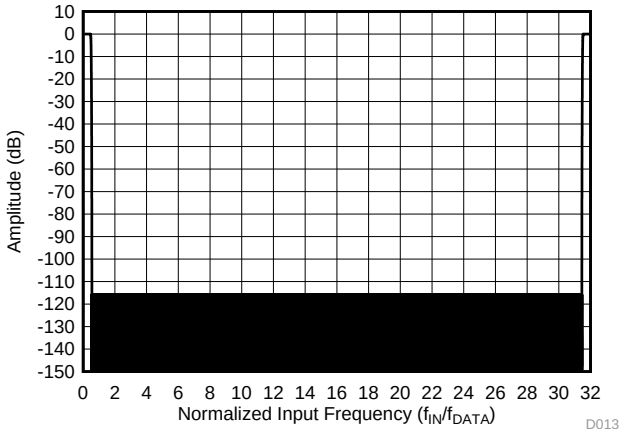


Figure 76. Extended Frequency Response of Wideband 1 Filter (OSR 32)

The Wideband filters use a multiple-stage, linear-phase, digital-filter architecture. Linear-phase filters exhibit constant delay time versus input frequency (also known as constant group delay). This feature of linear phase filters means that the time delay from any instant of the input signal to the corresponding same instant of the output data is constant and independent of the input-signal frequency. This behavior results in essentially zero phase error when measuring multitone signals.

8.3.2.2.2 Wideband Filters Settling Time

The Wideband filters fully settle before outputting data after the START pin low-to-high transition or a START command is issued. The settling time of the Wideband filters is 84 conversion cycles; the $\overline{\text{DRDY}}$ signal idles high and does not assert until new settled data are available in SPI interface mode. In frame-sync interface mode, the output shift register outputs zeroes in place of the conversion data for 84 conversion cycles until the first settled data are available. A step input on the analog input requires multiple conversions to settle if START is not pulsed, or if the START command is not issued. Figure 77 shows the settling response with the x-axis normalized to conversions or $\overline{\text{DRDY}}$/FSYNC cycles.

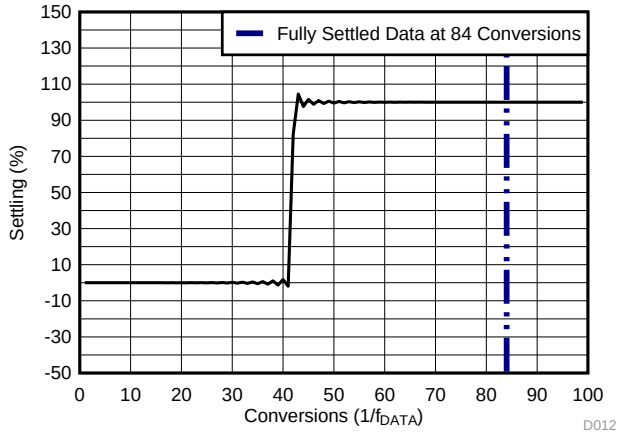


Figure 77. Step Response For Wideband Filters

Figure 78 and Figure 79 plot the undershoot and overshoot from the Wideband digital filter during an input step function.

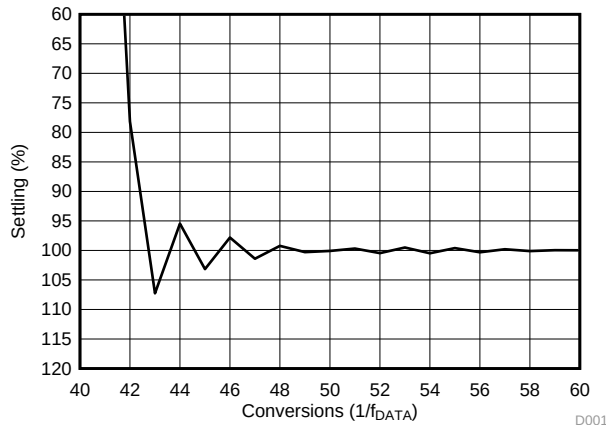


Figure 78. Wideband Filters Step-Response Undershoot

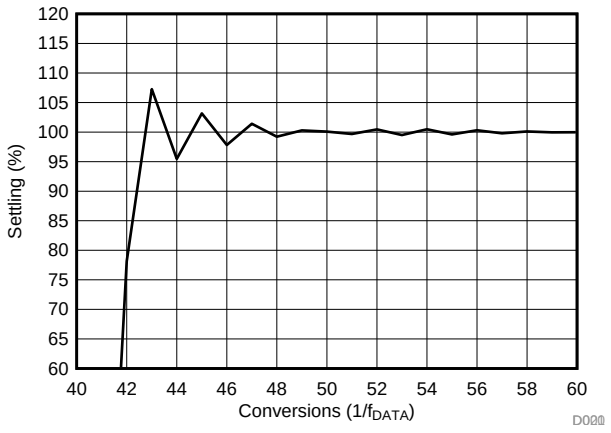


Figure 79. Wideband Filters Step-Response Overshoot

8.3.3 Voltage Reference Inputs (REFP, REFN)

The ADC requires the connection of an external reference voltage for operation. The voltage reference for the device is the differential voltage between REFP and REFN: $V_{REF} = (V_{REFP} – V_{REFN})$. The reference inputs are not buffered and use a sampling structure similar to that of the analog inputs, with the equivalent circuitry on the reference inputs shown in Figure 80. The load across REFP and REFN is presented by the switched-capacitor in parallel with a 6.4-kΩ resistor, and is modeled with an effective impedance (Z_{eff}) proportional to the master clock, f_{CLK}, as shown in Figure 81.

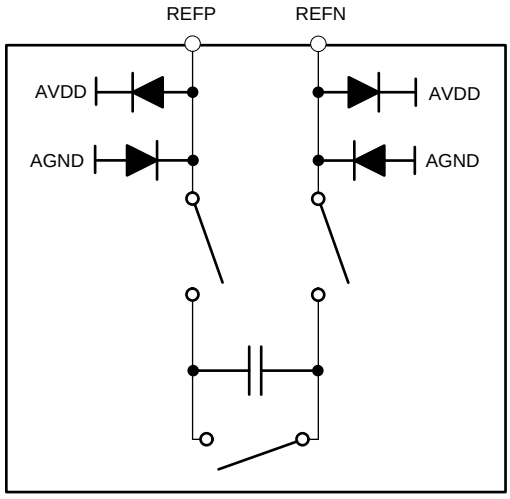


Figure 80. Equivalent Reference Input Circuitry

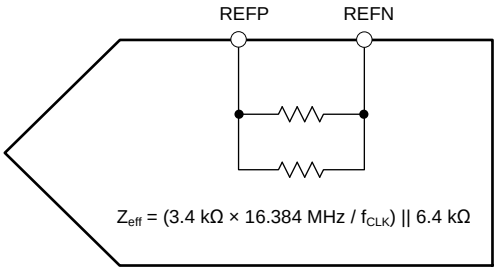


Figure 81. Effective Reference Impedance

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 0.3 V, and do not exceed AVDD by 0.3 V. Use external Schottky clamp diodes or series resistors to limit the input current to safe values if the reference input may exceed the absolute maximum ratings (see the *Absolute Maximum Ratings* table).

A high-quality reference voltage with the appropriate drive strength is required for achieving the best performance from the ADS127L01. Noise and drift on the reference degrade overall system performance. Use a minimum parallel combination of 10-µF and 0.1-µF ceramic bypass capacitors directly across the reference inputs, REFP and REFN. Place these capacitors as close as possible to the device on the layout. See the *Application Information* section for example reference circuits.

8.3.4 Clock Input (CLK)

The ADS127L01 requires an external clock for operation. This clock signal is used for the sampling network of the modulator without any prescalers or dividers, and for the timing for the digital filter. Drive the ADC with an external clock by applying the clock input to the CLK pin. At the maximum data rate, the clock input is 16.384 MHz for HR mode, 8.192 MHz for LP mode, and 4.096 MHz for VLP mode.

A high-quality, low-jitter clock is essential for optimum performance measuring the high-frequency input signals. Any uncertainty during sampling of the input from clock jitter limits the maximum achievable SNR. For example, uses an external clock with better than 10 ps_{rms} jitter for a 200-kHz f_{IN}. For a lower f_{IN}, the target jitter requirement can be relaxed by –20 dB per decade. At f_{IN} = 20 kHz, use a clock with better than 100-ps_{rms} jitter.

The selection of the external clock frequency (f_{CLK}) does not affect the resolution of the ADS127L01. The output data rates scale with f_{CLK} frequency down to a minimum clock frequency of f_{CLK} = 100 kHz. Use a slower f_{CLK} to reduce the ADC power consumption and relax the requirements of an external ADC drive circuit on the analog input and reference input.

Crystal clock oscillators are the recommended clock source. Make sure to avoid excess ringing on the clock input. A series resistor placed at the external clock buffer output often helps to reduce overshoot.

8.3.5 Out-of-Range-Detect System Monitor

An out-of-range-detect system-monitor bit (INP) is available in the status word (see the *Status Word* section). The out-of-range detect bit flags (INP = 1) when the input exceeds the positive or negative full-scale range, set by V_{REF}, with each conversion result. The input is monitored using an analog comparator. The flag is issued when the full-scale range is exceeded without waiting for the conversions to propagate through the digital filter. The INP bit is used for narrow out-of-range input glitches that may or may not be removed by the ADC digital filter.

8.3.6 System Calibration

The ADC incorporates optional offset- and gain-calibration registers to system-calibrate the ADC and signal chain when in SPI interface mode. Enable the offset calibration register by setting FSC bit (bit 5 in the *Configuration register*) to 1, and enable the gain calibration register by setting OFC bit (bit 4 in the *Configuration register*) to 1. The programmable offset calibration value is 24 bits wide, and the gain calibration value is 16 bits wide. Use calibration to correct internal ADC errors or overall system errors. Calibration is only supported through direct user calibration, requiring the user to calculate and write the correction values to the calibration registers. Perform a system offset calibration before full-scale calibration. After power-up, but before calibrating, wait for the power supplies and reference voltage to fully settle.

As shown in Figure 82, the value of the offset calibration register is subtracted from the filter output, and then multiplied by the full-scale register value. The data are then clipped to a 24-bit value to provide the final output.

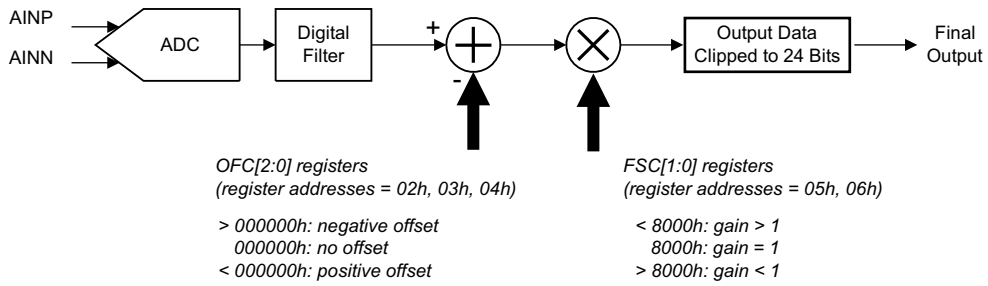


Figure 82. ADC Calibration Block Diagram

Equation 6 shows the internal calibration on the data result.

$$\text{ADC Final Output Data} = (\text{Filter Output} - \text{OFC}[23:0]) \times \text{FSC}[15:0] / 8000\text{h} \quad (6)$$

The ADC offset calibration word is 24 bits, consisting of three 8-bit registers (OFC2, OFC, 1 OFC0), as shown in Table 4. The offset value is twos complement format with a maximum positive value equal to 7FFFFFh (for negative offset), and a maximum negative value equal to 800000h (for positive offset). A register value equal to 000000h has no offset correction. For offset calibration, short the ADC inputs or system inputs, and average the conversions; averaging reduces noise for a more accurate calibration. Write the average value to the offset calibration registers. The ADC subtracts the value from the conversion result.

Table 4. Offset Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
OFC0	LSB	02h	OFC_B7	OFC_B6	OFC_B5	OFC_B4	OFC_B3	OFC_B2	OFC_B1	OFC_B0 (LSB)
OFC1	MID	03h	OFC_B15	OFC_B14	OFC_B13	OFC_B12	OFC_B11	OFC_B10	OFC_B9	OFC_B8
OFC2	MSB	04h	OFC_B23 (MSB)	OFC_B22	OFC_B21	OFC_B20	OFC_B19	OFC_B18	OFC_B17	OFC_B16

The ADC gain calibration word is 16 bits consisting of two 8-bit registers (FSC1, FSC0), as shown in Table 5. The full-scale calibration value is twos compliment, with a unity-gain correction factor at a register value equal to 8000h. Table 6 shows register values for selected gain factors.

Table 5. Gain Calibration Registers

REGISTER	BYTE ORDER	ADDRESS	BIT ORDER							
FSC0	LSB	05h	FSC_B7	FSC_B6	FSC_B5	FSC_B4	FSC_B3	FSC_B2	FSC_B1	FSC_B0 (LSB)
FSC1	MSB	06h	FSC_B15 (MSB)	FSC_B14	FSC_B13	FSC_B12	FSC_B11	FSC_B10	FSC_B9	FSC_B8

Table 6. Gain Calibration Register Values

FSCAL[2:0] REGISTER VALUE	GAIN FACTOR
7FFFh	2.00
8000h	1.00
0000h	0.00

For gain calibration, apply a dc calibration voltage that is less than positive full-scale voltage in order to avoid clipped codes (V_{IN} < +FSR), and average the conversions to reduce noise for a more accurate calibration. Gain calibration is computed as shown in Equation 7, after offset error is removed.

$$\text{Full-Scale Calibration} = \text{Expected Code Value} / \text{Actual Code Value} \quad (7)$$

If the actual code is higher than the expected value, then the calculated calibration value is less than 8000h, and the ADC gain is subsequently reduced. Write the calibration value to the gain calibration registers.

8.4 Device Functional Modes

8.4.1 Operating Modes (HR, LP, VLP)

The ADS127L01 offers three operational modes: high-resolution (HR), low-power (LP), and very-low-power (VLP). These modes optimize power consumption by restricting the maximum master-clock frequency (f_{CLK}) controlling the data rate. The status of the HR pin determines if the device is in HR mode or LP mode. Enter VLP mode by setting the ADS127L01 in LP mode, and increasing the value of the external R_{EXT} power scaling resistor from 60.4 kΩ to 120 kΩ. The tolerance on the R_{EXT} power-scaling resistor must be 1% or better. The analog current consumed by AVDD and LVDD decreases when in LP mode, and decreases further in VLP mode, with a tighter restriction on maximum master-clock frequency. Table 7 details the HR pin and REXT settings for each operating mode in the ADS127L01.

Table 7. Operating Mode Selection

OPERATING MODE	OPERATING MODE SELECTION PIN (HR)	R_{EXT} VALUE	MAXIMUM f_{CLK}
High-Resolution (HR)	1	60.4 kΩ	17.6 MHz
Low-Power (LP)	0	60.4 kΩ	8.8 MHz
Very-Low-Power (VLP)	0	120 kΩ	4.4 MHz

8.4.2 Hardware Mode Pins

The ADS127L01 uses two-state hardware mode pins for ADC configuration. The operating mode, interface selection, digital filter selection, and oversampling ratio (OSR) are all controlled through hardware pins. These pins are constantly monitored, and set by either pulling them high to DVDD, or low to DGND. Use pull-up or pull-down 100-kΩ resistors, or directly tie the pins to microcontroller or DSP I/O lines to set the state of the pins. When a change is sensed on the hardware mode pins after power-up, the ADC automatically issues a reset. To ensure synchronization, issue a software reset command, or pulse the $\overline{\text{RESET}}$/PWDN pin following the mode change delay, $t_{d(MD)}$.

When using the SPI interface mode, $\overline{\text{DRDY}}$ is held high after a mode change occurs until settled data are ready; see Figure 83 and Table 8.

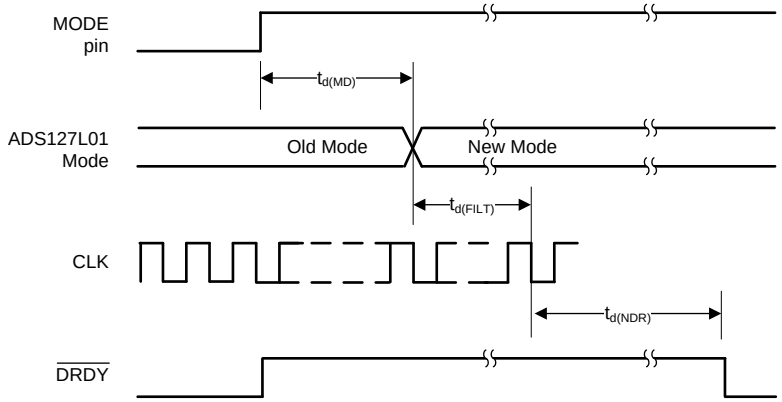


Figure 83. Mode Change Timing (SPI Interface)

Table 8. SPI Interface New Data After Mode Change

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{d(MD)}$	Delay time, MODE pin rising edge to mode change				3	t_{CLK}
$t_{d(FILT)}$	Delay time, mode change to first modulator sample		3.5		4.5	t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

In Frame-sync intreface mode, the DOUT pins are held low after a mode change occurs until settled data are ready; see Figure 84 and Table 9. Data can be read from the device to detect when DOUT changes, indicating that data are valid.

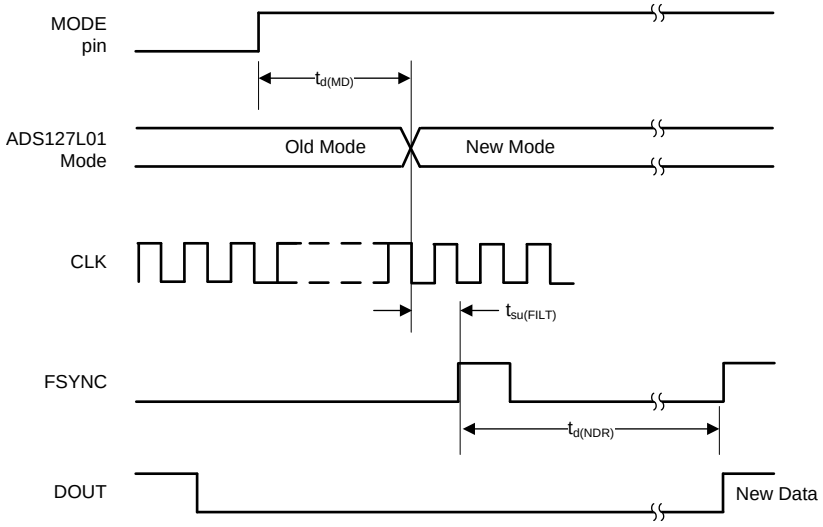


Figure 84. Mode Change Timing (Frame-Sync Interface)

Table 9. Frame-Sync Interface New Data After Mode Change

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{d(MD)}$	Delay time, MODE pin rising edge to mode change				3	t_{CLK}
$t_{su(FILT)}$	Setup time, mode change to FSYNC rising edge	Frame-sync slave	5			t_{CLK}
		Frame-sync master	1			t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

8.4.2.1 Interface Selection Pins (FORMAT, FSMODE)

Data are read from the ADS127L01 using one of two selectable interface modes, SPI or frame-sync. Use the FORMAT input pin to select among the two interface options.

If the frame-sync interface is selected, the ADS127L01 offers either a master or slave option, selectable using the FSMODE pin. Table 10 lists the available options.

Table 10. Interface Mode Options

FORMAT	FSMODE	INTERFACE MODE
0	0	SPI
0	1	SPI
1	0	Frame-sync slave mode
1	1	Frame-sync master mode

8.4.2.2 Digital-Filter Path Selection Pins (FILTER[1:0])

Three digital filter options are available in the ADS127L01: two Wideband filter options, and a Low-latency filter. See the *Digital Filter* section for detailed information on the digital filters and the frequency responses. The FILTER[1:0] hardware mode pins set the filter path selection for the modulator data, as shown in Table 11. Select the filter when START is low, or take the START or $\overline{\text{RESET}}/\overline{\text{PWDN}}$ pin low and back high after a filter path change. If software commands are used to control conversions, use the STOP and START commands after a change to the filter path selection. If a conversion is in process during a filter path change, the output data are not valid and must be discarded.

Table 11. Digital-Filter Path Selection

FILTER1	FILTER0	SELECTED FILTER PATH	FILTER TRANSITION BAND
0	0	Wideband 1 filter	$0.45 \times f_{DATA}$ to $0.55 \times f_{DATA}$
0	1	Wideband 2 filter	$0.40 \times f_{DATA}$ to $0.50 \times f_{DATA}$
1	0	Low-latency filter	SINC5 / SINC
1	1	Reserved: do not use	

8.4.2.3 Oversampling Ratio Selection Pins (OSR[1:0])

The ADS127L01 has two hardware oversampling ratio (OSR) pins used to configure the converter data rate. The rate at which the modulator bit stream data is decimated differs depending on whether the Wideband or the Low-latency digital filter is used (set using the Digital-Filter Path Selection Pins (FILTER[1:0])). The OSR options and corresponding maximum data rate at f_{CLK} = 16.384 MHz are shown in Table 12 for both the Wideband and the Low-latency filters. Change the OSR when START is low, or take the START or $\overline{\text{RESET}}/\overline{\text{PWDN}}$ pin low and back high after changing the OSR. If software commands are used to control conversions, use the STOP and START commands after changing the OSR.

Table 12. OSR Selection

FILTER	OSR1	OSR0	OSR	DATA RATE (kSPS) AT f_{CLK} = 16.384 MHz
Wideband filters	0	0	32	512
	0	1	64	256
	1	0	128	128
	1	1	256	64
Low-latency filter	0	0	32	512
	0	1	128	128
	1	0	512	32
	1	1	2048	8

8.4.3 Start Pin (START)

The START pin controls the start and stop of ADC conversions used for converter synchronization. Take the START pin low to stop conversions and reset the digital filter. Pull START high to start or restart the conversions.

Synchronization allows the conversion to be aligned with an external event, such as the changing of an external multiplexer on the analog inputs. The START pin is also used to synchronize multiple devices to within the same CLK cycle.

Figure 85 and Figure 86 illustrate the timing requirement for the START pin with respect to CLK in SPI and frame-sync interface modes. After synchronization, indication of valid data depends on whether SPI or frame-sync interface mode is used.

In the SPI interface mode, $\overline{\text{DRDY}}$ goes high as soon as START is taken low, as shown in Figure 85. After START is returned high, $\overline{\text{DRDY}}$ stays high while the digital filter completes reset and settles. After valid data are ready for retrieval, $\overline{\text{DRDY}}$ goes low.

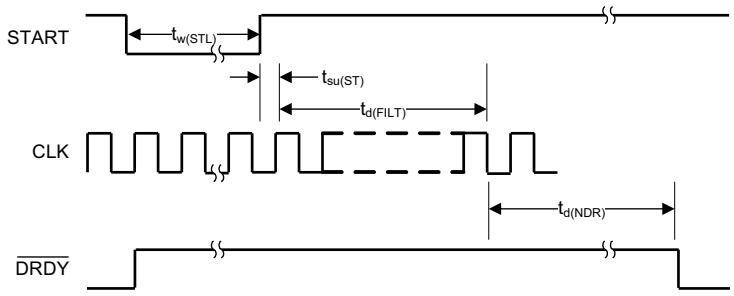


Figure 85. Synchronization Timing (SPI Interface)

Table 13. SPI Interface Start

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{w(STL)}$	Pulse duration, START low		4			t_{CLK}
$t_{su(ST)}$	Setup time, START rising edge to CLK rising edge		10			ns
$t_{d(FILT)}$	Delay time, START rising edge to first modulator sample		4		5	t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

In frame-sync interface, DOUT goes low as soon as START is taken low, as shown in Figure 86. After START is returned high, the following FSYNC rising edge releases the digital filter from reset to begin conversions. DOUT stays low while the digital filter is settling. Data are ready for retrieval on DOUT after the digital filter settles. For proper synchronization, FSYNC, SCLK, and CLK must be established before taking START high, and must then remain running. If either CLK, FSYNC or SCLK are interrupted or reset, reassert the START pin.

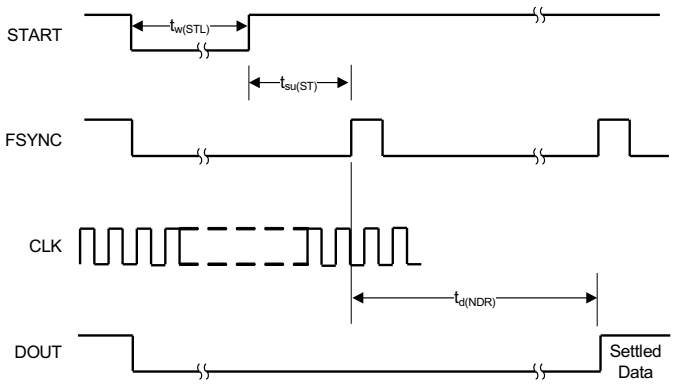


Figure 86. Synchronization Timing (Frame-Sync Interface)

Table 14. Frame-Sync Interface Start

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{w(STL)}$	Pulse duration, START low		4			t_{CLK}
$t_{su(ST)}$	Setup time, START rising edge to FSYNC rising edge	Frame-sync slave	6			t_{CLK}
		Frame-sync master	5			t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

In addition to the START pin, START and STOP commands are also available to control the start and stop of conversions, but only when using the SPI interface. Using the commands requires that the hardware START pin is tied low the entire time. The START command is also used to synchronize multiple ADS127L01s sharing the same SPI interface. See the *SPI Commands* section for information on using the START and STOP commands to control ADC conversions.

8.4.4 Reset and Power-Down Pin (RESET/PWDN)

The RESET/PWDN pin has two functions, depending on the amount of time the pin is held in a low state. If RESET/PWDN is low for < 2^{15} – 1 CLK periods, the ADS127L01 resets both the digital filter and register contents to default settings. The low-to-high transition of the RESET/PWDN pin brings the ADS127L01 out of reset by completing the digital filter reset, as shown in Figure 87 and Figure 88.

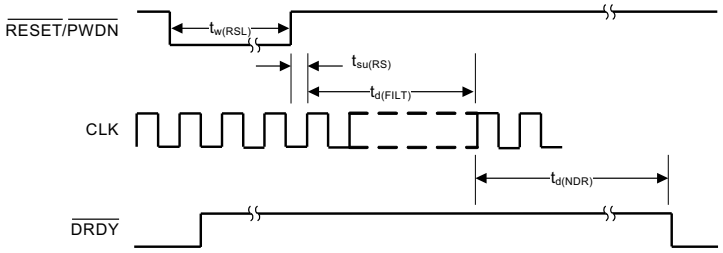


Figure 87. Reset Timing (SPI Interface)

Table 15. SPI Interface Reset Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{w(RSL)}$	Pulse duration RESET/PWDN low		4		2^{15} – 1	t_{CLK}
$t_{su(RS)}$	Setup time, RESET/PWDN rising edge to CLK rising edge		10			ns
$t_{d(FILT)}$	Delay time, RESET/PWDN rising edge to first modulator sample		37			t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

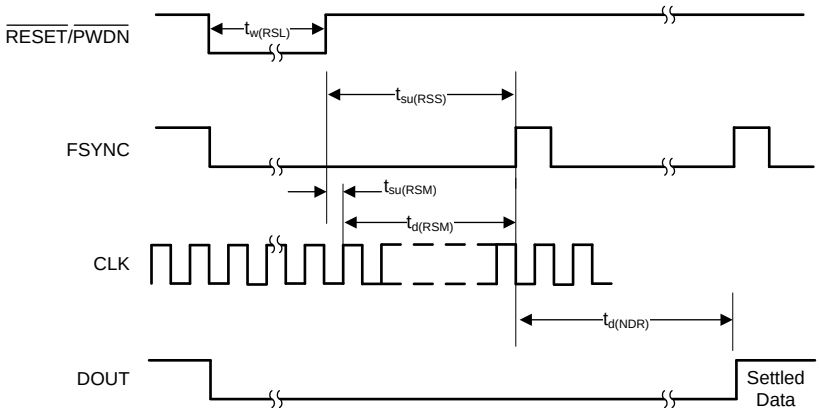


Figure 88. Reset Timing (Frame-Sync Interface)

Table 16. Frame-Sync Interface Reset Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{w(RSL)}$	Pulse duration RESET/PWDN low		4		2^{15} – 1	t_{CLK}
$t_{su(RSS)}$	Frame-Sync Slave Mode: Setup time, RESET/PWDN rising edge to first FSYNC		7			t_{CLK}
$t_{su(RSM)}$	Frame-Sync Master Mode: Setup time, RESET/PWDN rising edge to CLK rising edge		10			ns
$t_{d(RSM)}$	Frame-Sync Master Mode: Delay time, CLK rising edge to FSYNC rising edge		4			t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

If $\overline{\text{RESET}}/\overline{\text{PWDN}}$ is low for > 2^{15} – 1 CLK periods, the ADS127L01 enters power-down mode where both the analog and digital circuitry is completely deactivated. The digital inputs are internally disabled so there is no concern in driving the pins.

Use individual 1-MΩ pull-down resistors placed on CAP3 to DGND, SCLK to DGND, and $\overline{\text{DRDY}}$/FSYNC to DGND if power-down mode is planned to be used. These resistors help discharge voltage when the device is placed in power-down mode. Shut down the CLK and SCLK in power-down mode to avoid additional power consumption.

Return the $\overline{\text{RESET}}/\overline{\text{PWDN}}$ pin high to exit power-down mode. As shown in Figure 89 and Figure 90, a minimum of 2^{15} + 37 master clock periods must elapse before the device exits power-down mode and begins sampling when using SPI interface mode. $\overline{\text{DRDY}}$ stays high after exiting power-down mode while the digital filter settles.

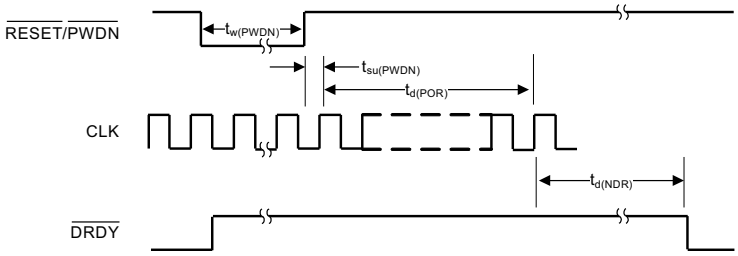


Figure 89. Power-Down Timing (SPI Interface)

Table 17. SPI Interface Power-Down Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{w(PWDN)}$	Pulse duartion$\overline{\text{RESET}}/\overline{\text{PWDN}}$ low		2^{15}			t_{CLK}
$t_{su(PWDN)}$	Setup time, $\overline{\text{RESET}}/\overline{\text{PWDN}}$ rising edge to CLK rising edge		10			ns
$t_{d(POR)}$	Delay time, power-on-reset complete following $\overline{\text{RESET}}/\overline{\text{PWDN}}$ rising edge		2^{15} + 37			t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

A minimum of 2^{15} + 7 master clock periods must elapse before the device exits power-down mode to begin sampling, when in Frame-Sync interface mode, as shown in Figure 90 and Table 18. When using Frame-Sync interface mode, DOUT will read back low while the digital filter settles.

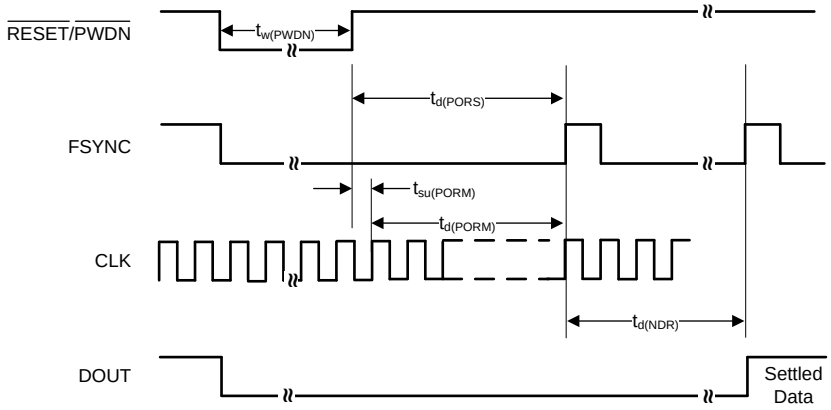


Figure 90. Power-Down Timing (Frame-Sync Interface)

Table 18. Frame-Sync Interface Power-Down Timing

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
$t_{w(PWDN)}$	Pulse duration $\overline{RESET}/\overline{PWDN}$ low		2^{15}			t_{CLK}
$t_{d(PORS)}$	Frame-Sync Slave Mode, Delay time, $\overline{RESET}/\overline{PWDN}$ rising edge to FSYNC rising edge		2^{15} + 7			t_{CLK}
$t_{su(PORM)}$	Frame-Sync Slave Mode, Setup time, $\overline{RESET}/\overline{PWDN}$ rising edge to CLK rising edge		10			ns
$t_{d(PORM)}$	Frame-Sync Slave Mode, Delay time, CLK rising edge to FSYNC rising edge		2^{15} + 7			t_{CLK}
$t_{d(NDR)}$	Delay time for new data to be ready	Wideband filters		84		t_{DATA}
		Low-latency filter		See Table 3		t_{DATA}

8.5 Programming

Data are retrieved from the ADS127L01 using a serial interface. To provide easy connection to either microcontrollers or DSPs, three communication modes are available: SPI, frame-sync master, and frame-sync slave. The FORMAT and FSMODE hardware mode pins select the interface. The same communication pins are used for all three interfaces: SCLK, $\overline{\text{DRDY}}$/FSYNC, DIN, DAISYIN, and DOUT; however, functionality depends on the interface selected.

When FORMAT = 0, SPI interface is selected, and the $\overline{\text{DRDY}}$/FSYNC pin becomes a data ready ($\overline{\text{DRDY}}$) output. In SPI interface mode, commands and internal registers are available for further device configuration. Tie the FSMODE pin to DGND when using SPI communication mode.

When FORMAT = 1, frame-sync interface mode is selected, and the $\overline{\text{DRDY}}$/FSYNC pin becomes an FSYNC input or output. Frame-sync offers two different modes controlled by the FSMODE pin.

When FSMODE = 0, the interface uses frame-sync slave mode, requiring that the SCLK and FSYNC signals are driven by the processor to the ADS127L01.

When FSMODE = 1, the interface is set to frame-sync master mode, and the SCLK and FSYNC signals are generated from the ADC derived from the master clock.

8.5.1 Serial Peripheral Interface (SPI) Programming

The SPI-compatible serial interface of the device is used to read conversion data, read and write the device configuration registers, and control device operation. Only SPI mode 1 (CPOL = 0, CPHA = 1) is supported. The interface consists of five control lines ($\overline{\text{CS}}$, SCLK, DIN, DOUT, and $\overline{\text{DRDY}}$/FSYNC), but the interface is operational with only four control lines. If the serial bus is not shared with any other device, $\overline{\text{CS}}$ can be tied low permanently so that only signals SCLK, DIN, DOUT and $\overline{\text{DRDY}}$/FSYNC are required to communicate with the device.

8.5.1.1 Chip Select ($\overline{\text{CS}}$)

Chip select ($\overline{\text{CS}}$) is an active-low input that selects the device for SPI communication. $\overline{\text{CS}}$ must remain low for the entire duration of the serial communication to complete a command or data readback. When $\overline{\text{CS}}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT enters a high-impedance state. If the serial bus is not shared with another peripheral, $\overline{\text{CS}}$ can be tied low.

8.5.1.2 Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input, and is used to clock data into and out of the device on DIN and DOUT, respectively. SCLKs can be sent to the ADC continuously or in byte increments. Even though the input has hysteresis, keep the SCLK signal as clean as possible to prevent glitches from accidentally shifting data. When the serial interface is idle, hold SCLK low.

Programming (continued)

8.5.1.3 Data Ready ($\overline{DRDY}$/FSYNC)

In SPI interface mode, $\overline{DRDY}$/FSYNC is an active-low, new-data-ready indicator for when a new conversion result is ready for retrieval. When $\overline{DRDY}$/FSYNC transitions low, new conversion data are ready. The $\overline{DRDY}$/FSYNC signal transitions from low to high with the first SCLK falling edge, as shown in Figure 91. When no data are read during continuous conversion mode, $\overline{DRDY}$/FSYNC remains low but pulses high for a duration of 2 · t_{CLK} before the next $\overline{DRDY}$/FSYNC falling edge. The $\overline{DRDY}$/FSYNC pin is always actively driven, even when $\overline{CS}$ is high.

A new conversion result is loaded into the output shift register before $\overline{DRDY}$ transitions from high to low. The LSB of the previous data word must be read at least 4 · t_{CLK} before the next $\overline{DRDY}$ falling edge. This delay is known as *keep-out time* (t_{KO}). Keep SCLK low during t_{KO} until the next conversion result is ready for retrieval, as shown in Figure 91.

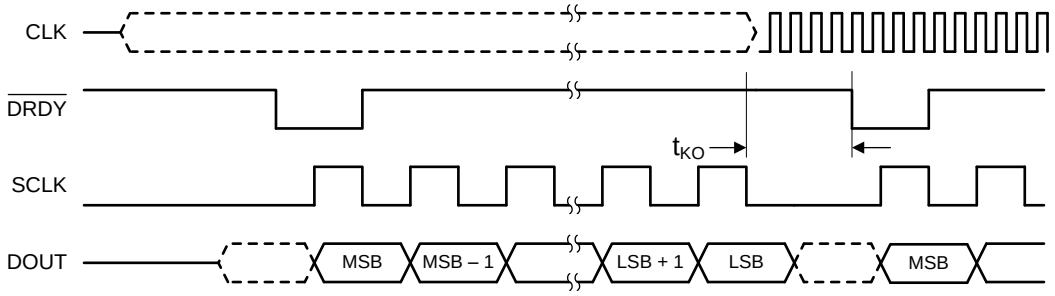


Figure 91. SPI Keep-Out Time (t_{KO})

8.5.1.4 Data Input (DIN)

The data input pin (DIN) is used with SCLK to send data (commands and register data) to the device. The device latches data on DIN on the SCLK falling edge. The device never drives the DIN pin.

8.5.1.5 Data Output (DOUT)

DOUT is used with SCLK to read conversion and register data from the device. Data on DOUT are shifted out on the SCLK rising edge, to be read from the host on the SCLK falling edge. DOUT goes to a high-impedance state when $\overline{CS}$ is high.

8.5.1.6 Daisy-Chain Input (DAISYIN)

DAISYIN is an optional pin used with SCLK to shift data in from a secondary ADS127L01 device when in a daisy-chain configuration. Data are shifted out from DOUT of a secondary device into the DAISYIN pin of the first device. The individual data bits are latched into DAISYIN on the SCLK falling edge. See the *Multiple Device Configuration* section for more information on using daisy-chain mode. If not used, tie the DAISYIN pin to DGND.

8.5.1.7 SPI Timeout

The ADS127L01 offers an SPI timeout feature that is used to recover communication when a serial interface transmission is interrupted. This feature is especially useful in applications where $\overline{CS}$ is permanently tied low and is not used to frame a communication sequence.

The timeout feature is disabled by default, but can be enabled in the CONFIG register. The time for the timeout to issue is also configurable using the CONFIG register. When enabled, and whenever a complete command is not sent within 2^{14} · t_{CLK} or 2^{16} · t_{CLK} (configurable by the TOUT_DEL bit in the CONFIG register), the serial interface resets and the next SCLK pulse starts a new communication cycle. For the RREG and WREG commands, a complete command includes the command byte plus the register bytes that are read or written.

Programming (continued)

8.5.1.8 SPI Commands

The ADS127L01 provides flexible configuration, including commands and configurable registers, only when using the SPI interface. The commands, summarized in Table 19, are stand-alone and configure the operation of the ADS127L01. Each command is a single byte, except for the register read and write operations that require two or more bytes. $\overline{CS}$ must remain low for the entire command operation (especially for multibyte commands). Take $\overline{CS}$ high during a opcode command to abort the command.

Table 19. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
System Commands			
RESET	Reset the device	0000 011x	
START	Start or restart (synchronize) conversions	0000 100x	
STOP	Stop conversion	0000 101x	
Data Read Commands			
RDATA	Read data by command	0001 0010	
Register Commands			
RREG	Read (*nnnn* + 1) registers starting at address *rrrr*	0010 *rrrr*	0000 *nnnn*
WREG	Write (*nnnn* + 1) registers starting at address *rrrr*	0100 *rrrr*	0000 *nnnn*

8.5.1.8.1 RESET (0000 011x)

The RESET command halts conversions and resets the ADC to power-on-reset values. During this time, the digital filter resets, requiring an additional power-up time for conversions to begin. The RESET command is decoded by the ADS127L01 on the seventh falling edge of SCLK. For more information, refer to the *Reset and Power-Down Pin (RESET/PWDN)* section.

8.5.1.8.2 START (0000 100x)

The START command starts conversions and resynchronize the device. When conversions are stopped, either at power-up or following a STOP command, issue a START command to begin ADC conversions. Issuing a START command restarts the conversions by resetting the digital filters. During the reset period, $\overline{DRDY}$/FSYNC does not toggle. The START command is decoded by the ADS127L01 on the seventh falling edge of SCLK. The START pin must be held low if the START and STOP commands are used. For more information, refer to the *Start Pin (START)* section.

8.5.1.8.3 STOP (0000 101x)

The STOP command places the ADC in an idle state where the modulator stops converting. The STOP command is decoded by the ADS127L01 on the seventh falling edge of SCLK. The START pin must be held low if the START and STOP commands are used.

8.5.1.8.4 RDATA (0001 0010)

The RDATA command reloads the output shift register to the MSB of the most recent data. The RDATA command is decoded on the eighth SCLK falling edge, and begins shifting out the MSB of the data word on DOUT on the ninth SCLK.

8.5.1.8.5 RREG (0010 rrrr 0000 nnnn)

The RREG command reads the number of bytes specified by *nnnn* (number of registers to be read – 1) from the device configuration register, starting at register address *rrrr*. The command is completed after *nnnn* + 1 bytes are clocked out after the RREG command byte. For example, the command to read three registers (*nnnn* = 0010) starting at register address 00h (*rrrr* = 0000) is 0010 0000 0000 0010 as shown in Figure 92. The communication length must be extended by the proper number of SCLKs to shift register contents out.

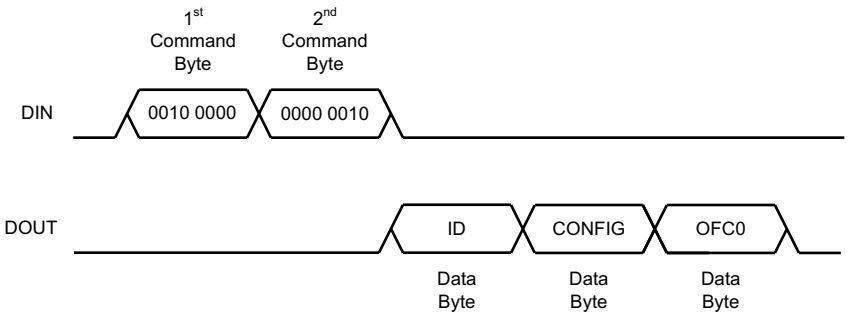


Figure 92. Read from Register

8.5.1.8.6 WREG (0100 rrrr 0000 nnnn)

The wREG command writes the number of bytes specified by *nnnn* (number of registers to be written – 1) to the device configuration register, starting at register address *rrrr*. The command is completed after *nnnn* + 1 bytes are clocked in after the WREG command byte. For example, the command to write two registers (*nnnn* = 0001) starting at register address 01h (*rrrr* = 0001) is 0100 0001 0000 0001 as shown in Figure 93. Two bytes follow the command to write the contents to the registers. The frame must extend by the proper number of SCLKs to write data to the registers.

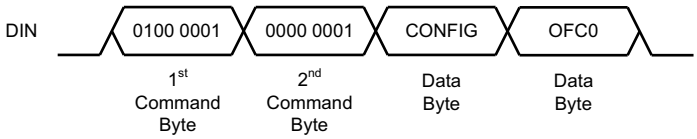


Figure 93. Write to Register

8.5.2 Frame-Sync Programming

Frame-sync interface is similar to the interface often used on audio ADCs. The ADS127L01 offers both frame-sync master and frame-sync slave modes that are selectable using the FSMODE pin. In frame-sync format, commands and register assignments are not available. Tie DIN low to DGND.

8.5.2.1 Frame-Sync Master Mode

When operating in frame-sync master mode, the ADC acts as the system master, and provides the FSYNC, SCLK, and DOUT signals. The FSYNC and SCLK signals are derived as a function of the master clock input, f_{CLK}. The data are output MSB first on the rising edge of FSYNC.

8.5.2.1.1 Chip Select ($\overline{CS}$) in Frame-Sync Master Mode

$\overline{CS}$ is not used in frame-sync interface mode.. Tie the $\overline{CS}$ pin to DGND.

8.5.2.1.2 Serial Clock (SCLK) in Frame-Sync Master Mode

When operating in frame-sync master mode, the serial clock (SCLK) is derived from the master clock and provided from the ADC to the microprocessor. Every frame period, $t_{c(FRAME)}$, includes 32 SCLKs to shift all data out before new data are ready. This SCLK speed is proportional to the frame size, $t_{c(FRAME)}$ / 32 in frame-sync master mode. The frame size is determined by the data rate setting using the hardware FILTER pin settings, OSR pin settings, and speed of the master clock, f_{CLK}. The data on DOUT are clocked out on the falling edge of SCLK to be latched by the host processor on the rising edge of SCLK.

8.5.2.1.3 Frame-Sync ($\overline{\text{DRDY}}$/FSYNC) in Frame-Sync Master Mode

In frame-sync master mode, the FSYNC pin is an output whose period is proportional to the ADC programmed data rate. Within each FSYNC period are 32 SCLKs to shift out the data on DOUT. The FSYNC duty cycle is designed to be 50-50, where an FSYNC low-to-high transition takes place before the MSB of new data, and high-to-low transition takes place before bit 15 on the falling edge of SCLK. For more information on FSYNC master-mode timing, see the *Frame-Sync Master Mode Timing Requirements*.

8.5.2.1.4 Data Input (DIN) in Frame-Sync Master Mode

DIN is not available in frame-sync master mode. Tie DIN to DGND.

8.5.2.1.5 Data Output (DOUT) in Frame-Sync Master Mode

The conversion data are clocked out on the falling edge of SCLK to be latched by the host processor on the rising edge of SCLK. The MSB data become valid on DOUT after FSYNC goes high. The subsequent bits are shifted out with each falling edge of SCLK.

8.5.2.1.6 Daisy-Chain Input (DAISYIN) in Frame-Sync Master Mode

DAISYIN and daisy-chain operation are not supported in frame-sync master mode. Tie DAISYIN to DGND.

8.5.2.2 Frame-Sync Slave Mode

When operating in frame-sync slave mode, the user must supply the framing signal FSYNC (similar to the *left/right clock* on stereo audio ADCs) and the serial clock SCLK (similar to the *bit clock* on audio ADCs). The data are output MSB first or left-justified on the rising edge of FSYNC. The FSYNC and SCLK inputs must be continuously running with the relationships shown in the *Frame-Sync Timing Requirements*.

8.5.2.2.1 Chip Select ($\overline{\text{CS}}$) in Frame-Sync Slave Mode

$\overline{\text{CS}}$ is not used in frame-sync programming. Tie $\overline{\text{CS}}$ to DGND.

8.5.2.2.2 Serial Clock (SCLK) in Frame-Sync Slave Mode

In frame-sync slave mode, use SCLK to clock data out on DOUT. SCLK must run continuously; if SCLK is shut down, the data read back is corrupted. The number of SCLKs within a frame period ($t_{c(FRAME)}$) can be any power-of-two ratio of CLK cycles (1, 1/2, 1/4, and so on), as long as the number of cycles is sufficient to shift the data output within one frame.

Use SCLK to also shift data into DAISYIN when multiple devices are configured for daisy-chain operation. Even though SCLK has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally shifting the data.

8.5.2.2.3 Frame-Sync ($\overline{\text{DRDY}}$/FSYNC) in Frame-Sync Slave Mode

In frame-sync slave mode, the FSYNC pin is an input that transitions low to high at the data-rate frequency. The required number of f_{CLK} cycles to each FSYNC period depends on the configuration of the FILTER[1:0] and OSR[1:0] pins. If the FSYNC period is not the proper value, data read back is corrupted. For more information on frame-sync slave-mode timing, see the *Frame-Sync Slave Mode Timing Requirements*.

8.5.2.2.4 Data Input (DIN) in Frame-Sync Slave Mode

DIN is not used in frame-sync slave mode. Tie the DIN pin to DGND.

8.5.2.2.5 Data Output (DOUT) in Frame-Sync Slave Mode

The conversion data are clocked out on the falling edge of SCLK to be latched by the host processor on the rising edge of SCLK. The MSB data become valid on DOUT after FSYNC goes high. The subsequent bits are shifted out with each falling edge of SCLK.

8.5.2.2.6 Daisy-Chain Input (DAISYIN) in Frame-Sync Slave Mode

DAISYIN is an optional pin used along with SCLK to shift data from a secondary ADS127L01 device. Data are shifted out from DOUT of a secondary device into the DAISYIN pin of the first device. The data on DOUT is latched into DAISYIN on the SCLK falling edge. See the *Multiple Device Configuration* section for more information on using daisy-chain mode. Tie the DAISYIN pin to DGND if not used.

8.5.3 Data Format

The ADS127L01 provides either a 24-bit or 32-bit output word, 24 bits of which are data in binary twos complement format with an optional eight LSBs containing status word information. The size of one code (LSB) is calculated using Equation 8:

$$1\ \text{LSB} = (2 \times V_{REF}) / 2^{24} = +FS / 2^{23} \quad (8)$$

A positive full-scale input [$V_{IN} \geq (+FS - 1\ \text{LSB}) = (V_{REF} - 1\ \text{LSB})$] produces an output code of 7FFFFFh, and a negative full-scale input ($V_{IN} \leq -FS = -V_{REF}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 20 summarizes the ideal output codes for different input signals.

Table 20. Ideal Output Code Versus Input Signal

INPUT SIGNAL, V_{IN} ($V_{AINP} - V_{AINN}$)	IDEAL OUTPUT CODE(1)
≥ +FS ($2^{23} - 1$) / 2^{23}	7FFFFFh
+FS / 2^{23}	000001h
0	0
–FS / 2^{23}	FFFFFFh
≤ –FS	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

8.5.4 Status Word

Trailing the 24 bits of data is an optional 8-bit status word. The status word provides a real-time update of internal system monitors and data integrity. By default, the contents are a mixture of 4-bit CRC data integrity and system monitors. Alternatively, the status word can be set to output an 8-bit CRC without the system monitors. The CRCB bit in the CONFIG regsiter controls the status word contents. Set the CRCB bit to 0 for the status word to contain 4-bit CRC [bits 7:4], one bit [bit 3] to monitor out of range input (INP), and three bits [bits 2:0] to read back as 0. Set the CRCB bit to 1 for all eight bits [bits 7:0] of the status word to contain 8-bit CRC. See Figure 94 for a visual representation of the two modes.

By default, the optional 8-bit status word is enabled, but can be disabled when operating in SPI interface mode and setting the CS_ENB bit to 1 in the CONFIG register.

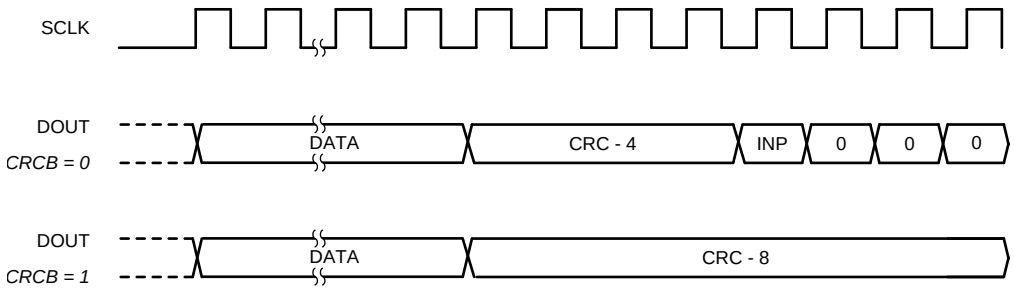


Figure 94. Status Word

8.5.5 Cyclic Redundancy Check (CRC)

The ADS127L01 implements two standard CRC algorithms: CRC-4-ITU to provide a 4-bit CRC, and CRC-8-CCITT for an 8-bit CRC. By default, the CRC-4-ITU option is enabled. Set the CRCB bit to 1 in the CONFIG register to change the format to CRC-8-CCITT and remove the system monitor bits from the status word.

The CRC is placed after the ADC data. The CRC is calculated using only the ADC output. When the 4-bit CRC is enabled, the ADS127L01 outputs a 4-bit status block after the CRC that is not used as part of the CRC check.

8.5.5.1 Computing the CRC

To calculate the CRC, divide the data bytes by the CRC polynomial using an XOR operation.

In 4-bit CRC mode, the CRC value is the 4-bit remainder of the division of the data bytes by a CRC polynomial of $P(x) = x^4 + x + 1$.

In 8-bit CRC mode, the CRC value is the 8-bit remainder of the division of the ADC data bytes by a CRC polynomial of $P(x) = x^8 + x^2 + x + 1$.

Then compare the calculated CRC values to the provided CRC value in the ADC output.

If the values do not match, a data-transmission error has occurred. In the event of a data-transmission error, read the data again. The CRC provides a higher level of detection of multiple-bit errors.

The following list shows a general procedure to compute the CRC value. Assume the shift register is n bits wide, where n is the number of CRC bits:

1. Set the polynomial value to 0x3 for an 4-bit CRC, or 0x07 for an 8-bit CRC .
2. Set the shift register to all zeros.
3. Begin with the MSB in the data stream. For every *n* bits:
   (a) Align the MSB of the data stream with the MSB of the shift register. XOR the data with the shift register, and place the result in the shift register.
   (b) Test the MSB of the shift register *n* times, and do one of the following each time:
      (a) If the most significant bit of the shift register is set, shift the register left by one bit, XOR the result with the polynomial, and place the result into the shift register.
      (b) If the most significant bit of the shift register is not set, shift the register left by one bit.
4. The result in the shift register is the CRC check value.

NOTE

The CRC algorithm used here employs an *assumed* set high bit. This bit is divided out by left-shifting the bit out of the register prior to XORing with the polynomial shift register. This process allows for calculation of the CRC with 8-bit hardware.

8.6 Register Maps

Table 21 describes the various ADS127L01 registers. Access to the registers is available in SPI interface mode. Register access is not available in frame-sync master or slave interface modes.

Table 21. ADS127L01 Register Assignments

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device ID (Read-Only Registers)										
00h	ID	x3h(1)	REV_ID[4:0]					DEV_ID[2:0]		
Configuration Settings										
01h	CONFIG	00h	0	0	FSC	OFC	TOUT_DEL	SPI_TOUT	CS_ENB	CRCB
02h	OFC0	00h	OFC_B[7:0]							
03h	OFC1	00h	OFC_B[15:8]							
04h	OFC2	00h	OFC_B[23:16]							
05h	FSC0	00h	FSC_B[7:0]							
06h	FSC1	80h	FSC_B[15:8]							
Device Settings (Read-Only Registers)										
07h	MODE	xx(1)	0	HR	OSR[1:0]		OSR[1:0]	FILTER[1:0]	FILTER[1:0]	FORMAT	FSMODE

(1) x is undefined.

8.6.1 ID: ID Control Register (address = 00h) [reset = x3h]

This register is programmed during device manufacture to indicate device characteristics.

Figure 95. ID Register

7	6	5	4	3	2	1	0
REV_ID[4:0]					DEV_ID[2:0]		
R-Undefined(1)					R-3h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) Reset values are device dependent.

Table 22. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	REV_ID[4:0]	R	xh(1)	**Revision ID**. These bits indicate the revision of the device and are subject to change without notice.
2:0	DEV_ID[2:0]	R	3h	**Device Family Identification.** 011 = ADS127L01

(1) Reset values are device dependent.

8.6.2 CONFIG: ADC Configuration Register (address = 01h) [reset = 00h]

This register contains the software controlled device options.

Figure 96. CONFIG Register

7	6	5	4	3	2	1	0
0	0	FSC	OFC	TOUT_DEL	SPI_TOUT	CS_ENB	CRCB
R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	0h	**Reserved** Always write 0
5	FSC	R/W	0h	**System Gain Correction** This bit enables system gain correction using the register contents from FSC0 and FSC1 registers. 0 = Disable system gain correction 1 = Enable system gain correction
4	OFC	R/W	0h	**Offset Correction** This bit enables Offset Correction using the register contents from OFC0, OFC1, and OFC2 registers. 0 = Disable offset correction 1 = Enable offset correction
3	TOUT_DEL	R/W	0h	**SPI Timeout** This bit sets the time limit to hold SCLK in an idle position for the SPI reset. 0 = SPI timeout delay set to 2^{16} t_{CLK}. 1 = SPI timeout delay set to 2^{14} t_{CLK}.
2	SPI_TOUT	R/W	0h	**SPI Timeout Enable** This bit enables or disables the SPI timeout function. 0 = Disable SPI timeout 1 = Enable SPI timeout
1	CS_ENB	R/W	0h	**Status Word Enable** This bit enables or disables the status word that is present following the 24-bit data output. 0 = Enable status word 1 = Disable status word
0	CRCB	R/W	0h	**Status Word Contents** This bit sets the contents used in the status word. 0 = CRC-4 and 4 bits of ADC diagnostics 1 = CRC-8

8.6.3 OFC0: System Offset Calibration Register 0 (address = 02h) [reset = 00h]

This register contains the least significant byte for the system offset calibration. The system offset calibration is a total of three bytes or 24 bits.

Figure 97. OFC0 Register

7	6	5	4	3	2	1	0
OFC_B[7:0]							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. OFC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC_B[7:0]	R/W	00h	**Offset Correction Bits** These bits set the system offset error correction.

8.6.4 OFC1: System Offset Calibration Register 1 (address = 03h) [reset = 00h]

This register contains the middle byte for the system offset calibration. The system offset calibration is a total of three bytes or 24 bits.

Figure 98. OFC1 Register

7	6	5	4	3	2	1	0
OFC_B[15:8]							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. OFC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC_B[15:8]	R/W	00h	**Offset Correction Bits** These bits set the system offset error correction.

8.6.5 OFC2: System Offset Calibration Register 2 (address = 04h) [reset = 00h]

This register contains the most significant byte for the system offset calibration. The system offset calibration is a total of three bytes or 24 bits.

Figure 99. OFC2 Register

7	6	5	4	3	2	1	0
OFC_B[23:16]							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. OFC2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OFC_B[23:16]	R/W	00h	**Offset Correction Bits** These bits set the system offset error correction.

8.6.6 FSC0: System Gain Calibration Register 0 (address = 05h) [reset = 00h]

This register contains the least significant byte for the system gain calibration. The system gain calibration is a total of two bytes or 16 bits.

Figure 100. FSC0 Register

7	6	5	4	3	2	1	0
FSC_B[7:0]							
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. FSC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FSC_B[7:0]	R/W	00h	**Gain Correction Bits** These bits set the system gain calibration value.

8.6.7 FSC1: System Gain Calibration Register 1 (address = 06h) [reset = 80h]

This register contains the most significant byte for the system gain calibration. The system gain calibration is a total of two bytes or 16 bits.

Figure 101. FSC1 Register

7	6	5	4	3	2	1	0
FSC_B[15:8]							
R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. FSC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FSC_B[15:8]	R/W	80h	**Gain Correction Bits** These bits set the system gain calibration value.

8.6.8 MODE: Mode Settings (address = 07h) [reset = xxh]

This register displays the hardware bit settings.

Figure 102. MODE Register

7	6	5	4	3	2	1	0
0	HR	OSR[1:0]		FILTER[1:0]		FORMAT	FSMODE
R-0h	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh	R-xh

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	**Reserved** Always reads 0
6	HR	R	xh	**High-Resolution Setting** This bit shows the readback status of HR (pin 29) 0 = LP Mode 1 = HR mode
5:4	OSR[1:0]	R	xh	**OSR Setting** This bit shows the readback status of OSR1 (pin 15) and OSR2 (pin 16) If FILTER[1:0] = 00 or 01 (Wideband filters): 00 = 32 01 = 64 10 = 128 11 = 256 If FILTER[1:0] = 10 (Low-latency filter): 00 = 32 01 = 128 10 = 512 11 = 2048
3:2	FILTER[1:0]	R	xh	**Filter Option Setting** This bit shows the readback status of FILTER1 (pin 12) and FILTER0 (pin 13) Digital-filter mode select: 00 = Wideband 1 filter 01 = Wideband 2 filter 10 = Low-latency filter (SINC5 and SINC) 11 = Reserved
1	FORMAT	R	xh	**Interface Mode Setting** This bit shows the readback status of FORMAT (pin 30) 0 = SPI interface mode 1 = Frame-sync interface mode
0	FSMODE	R	xh	**Frame-sync mode setting** This bit shows the readback status of FSMODE (pin 14) 0 = Frame-sync slave interface mode 1 = Frame-sync master interface mode

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Unused Inputs and Outputs

Do not float unused digital inputs because excessive power-supply leakage current might result.

The DIN and $\overline{CS}$ pins are only used in SPI interface mode. Tie DIN (pin 21) and $\overline{CS}$ (pin 23) directly to DGND when in frame-sync master mode or frame-sync slave mode.

If not daisy-chaining devices, tie DAISYIN directly to DGND.

In SPI interface mode, leave the unused $\overline{DRDY}$/FSYNC pin floating, or tie the unused pin to DVDD through high impedance resistors.

9.1.2 Multiple Device Configuration

The ADS127L01 provides configuration flexibility when multiple devices are connected in a system:

- SPI interface mode supports two methods to synchronize multiple devices: cascaded or daisy-chain.
- Frame-sync slave interface mode also supports the same two methods to synchronize multiple devices: cascaded or daisy-chain.
- Frame-sync master interface mode only supports the cascaded method to synchronize multiple devices. Daisy-chain configuration is not available in frame-sync master mode.

9.1.2.1 Cascaded Configuration

Two or more ADS127L01 devices can be cascaded together when using either SPI interface mode or Frame-Sync interface mode. Cascading devices allows multiple devices to share the same interface bus and reduces pin connections to the host processor.

Application Information (continued)

9.1.2.1.1 SPI interface Mode

In SPI interface mode, CLK, SCLK, DIN, and DOUT from each device are shared with independent $\overline{CS}$ signals. Monitor the $\overline{DRDY}$ signal from only one device. Leave the remaining $\overline{DRDY}$ pins floating. Figure 103 shows the required connections for cascading multiple devices in SPI interface mode.

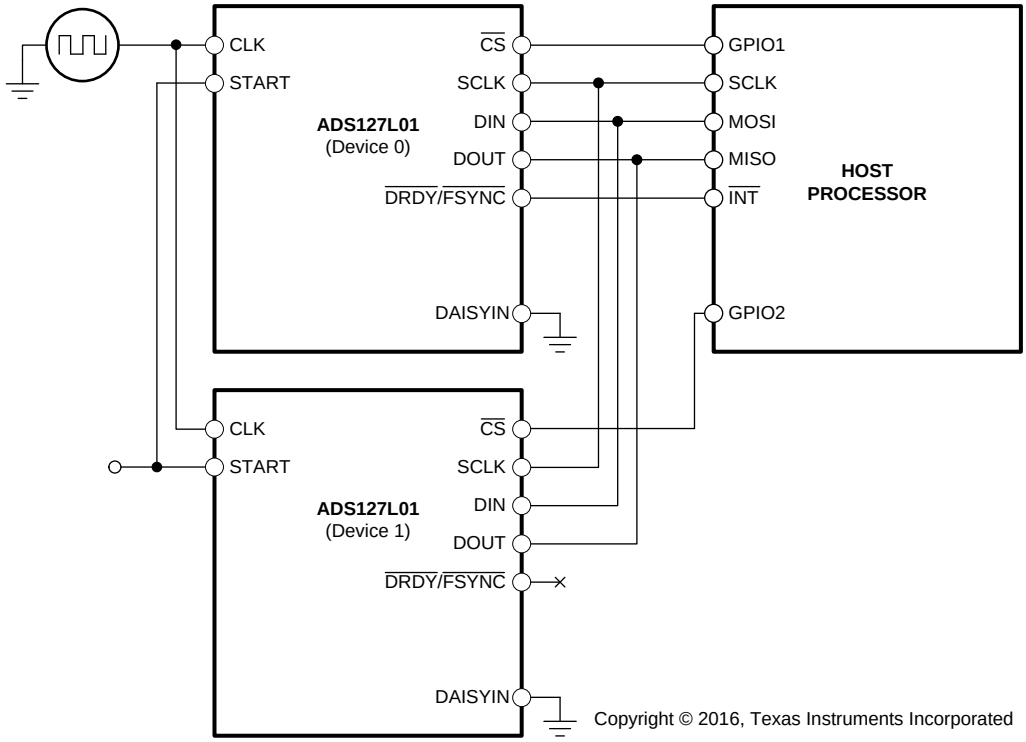


Figure 103. Cascaded Devices in SPI Interface Mode

The host processor must use a separate GPIO to control the $\overline{CS}$ pins on each ADS127L01 device. When $\overline{CS}$ is driven to a logic 1, the DOUT of that device is high-impedance. This structure allows another device to take control of the DOUT bus. The SCLK frequency must be high enough to read all of the data from each device before the next $\overline{DRDY}$ pulse arrives. Alternatively, tie the DOUT pin from each device to a separate pin on the host processor to collect data from multiple devices in parallel.

Equation 9 calculates the maximum number of devices that can share the same bus in a cascaded configuration in terms of data rate, SCLK frequency, and total number of bits per device.

$$\text{Number of Devices} \le (t_{DATA} - t_{CSDO} - t_{CSDOZ}) / (n \times t_{SCLK}) \quad (9)$$

where

- n = 24 or 32 bits

Application Information (continued)

9.1.2.1.2 Frame-Sync interface Mode

In frame-sync interface mode, the $\overline{CS}$ pin is unused and must be tied to DGND. CLK, SCLK, DIN, and FSYNC from each device are shared with independent DOUT signals. Connect the DOUT pin from each device to a separate input pin on the host processor to read the data from multiple devices in parallel. Figure 104 shows the required connections for cascading multiple devices in frame-sync interface mode.

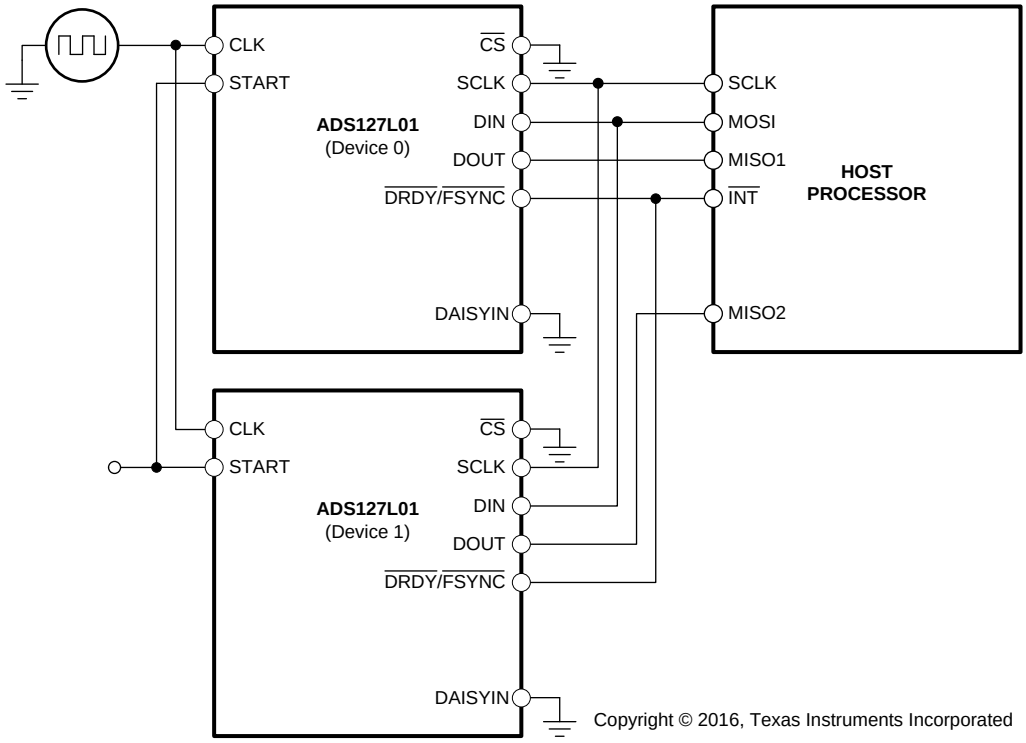


Figure 104. Cascaded Devices in Frame-Sync Mode

Only one device can be configured in frame-sync master mode; remaining devices must be configured in frame-sync slave mode. Otherwise, configure all devices in frame-sync slave mode.

Equation 10 calculates the maximum number of devices that can be daisy-chained for SPI and frame-sync slave mode in terms of data rate, SCLK frequency, and total number of bits to read from each device.

$$\text{Number of Devices} \le (t_{DATA}) / (n \times t_{SCLK}) \quad (10)$$

where

- n = 24 or 32 bits

9.1.2.2 Daisy-Chain Configuration

Two or more ADS127L01 devices can be daisy-chained together in either SPI interface mode or frame-sync slave mode. Frame-sync master mode does not support daisy-chain configurations. For both SPI and frame-sync slave mode, connect the DOUT pin of the first device in the chain to an input pin on the host processor. Connect the DOUT pin of the remaining devices to the DAISYIN pin of the next device. Connect the DAISYIN pin on the last device to DGND.

Equation 11 calculates the maximum number of devices that can share the same bus in a cascaded configuration in terms of data rate, SCLK frequency, and total number of bits per device.

$$\text{Number of Devices} \le (t_{DATA}) / (n \times t_{SCLK}) \quad (11)$$

where

- n = 32 bits

Application Information (continued)

9.1.2.2.1 Daisy-Chain Operation Using SPI interface Mode

In SPI interface mode, CLK, SCLK, DIN and $\overline{CS}$ are shared. Monitor only the $\overline{DRDY}$ signal from one device. Leave the remaining $\overline{DRDY}$ pins floating. The SCLK frequency must be high enough to read all the data from each device before the next $\overline{DRDY}$ pulse arrives. Figure 105 shows the required connections for daisy-chaining multiple devices in SPI interface mode.

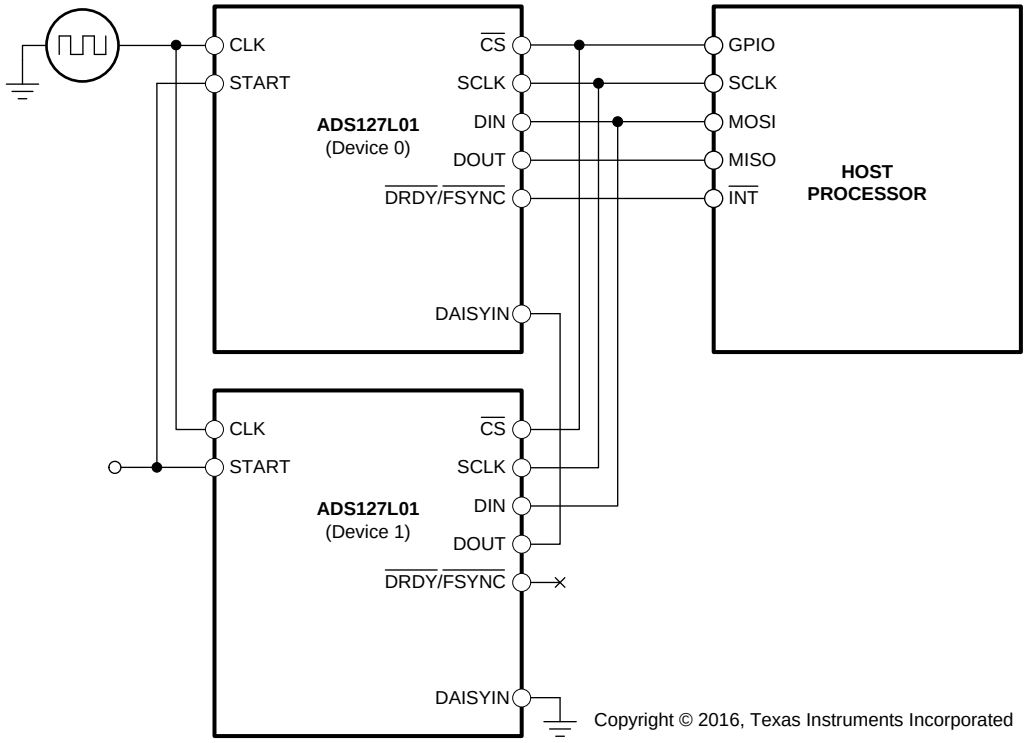


Figure 105. Daisy-Chained Devices in SPI Mode

All data from *Device 0* is shifted into *Device 1* on the DAISYIN pin. The MSB from the *Device 0* data immediately follows the LSB from *Device 1* on the DOUT pin of *Device 0*. Figure 106 illustrates the timing relationship for daisy-chaining devices in SPI interface mode.

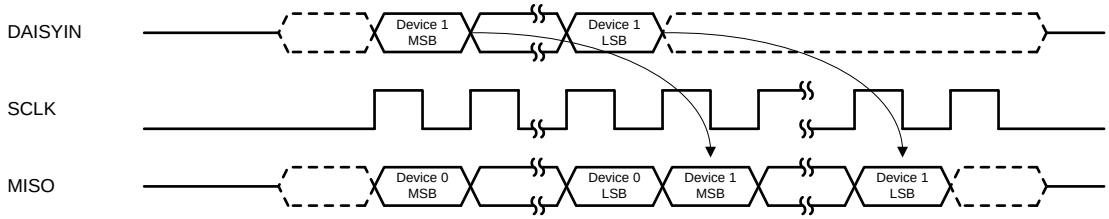


Figure 106. Daisy-Chain Timing in SPI interface Mode

Application Information (continued)

9.1.2.2.2 Daisy-Chain Operation Using Frame-Sync interface Mode

In frame-sync slave mode, CLK, SCLK, DIN and FSYNC are shared. The $\overline{CS}$ pin is unused and must be tied to DGND. The SCLK frequency must be high enough to read all the data from each device before the next frame begins. Figure 107 shows the required connections for daisy-chaining multiple devices in frame-sync slave mode.

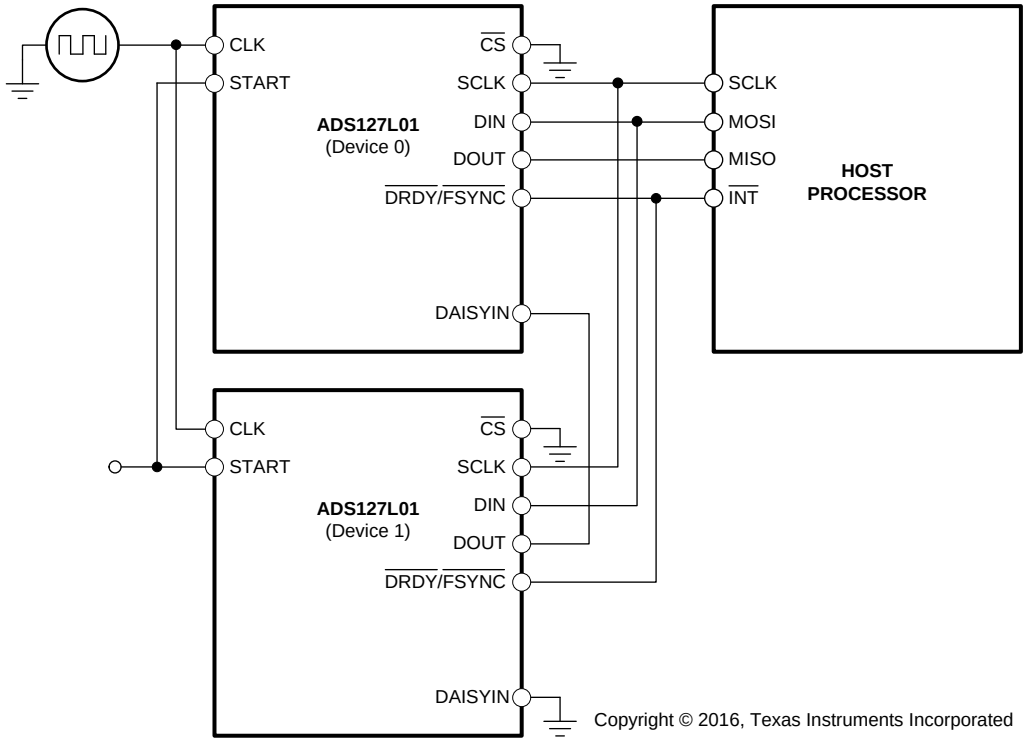


Figure 107. Daisy-Chained Devices in Frame-Sync Slave Mode

All data from *Device 1* are shifted into *Device 0* on the DAISYIN pin. The MSB from the *Device 1* data immediately follows the LSB from *Device 0* on the DOUT pin of *Device 1*. Figure 108 illustrates the timing relationship for daisy-chaining devices in frame-sync slave mode.

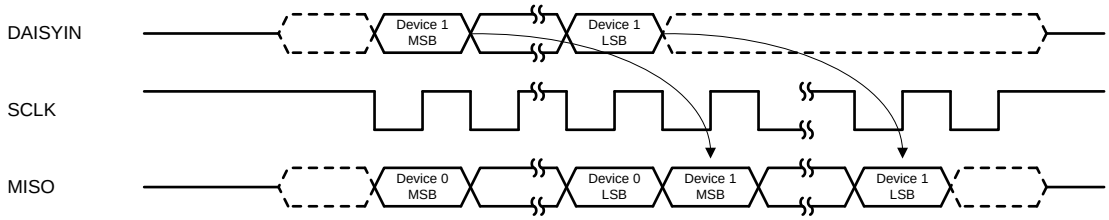


Figure 108. Daisy-Chain Timing in Frame-Sync Slave Mode

Application Information (continued)

9.1.2.3 Synchronizing Devices

Use the START pin or the $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin to synchronize multiple devices. The START pin does not reset the device registers to the default settings. The $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin resets the device to the factory default settings, and resets the interface when in frame-sync master mode. The delay from the START signal high to the first data ready is fixed for a given data rate (see the *Start Pin (START)* section for more details on the delay times).

An alternate way to synchronize multiple devices is using the $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin. The $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin resets the digital interface in addition to the digital filters and registers, making it the recommended synchronization method for frame-sync master mode. The delay from the $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin high to the first data ready is fixed for a given data rate (see the *Reset and Power-Down Pin ($\overline{\text{RESET}}$/$\overline{\text{PWDN}}$)* section for more details on the delay times). The $\overline{\text{RESET}}$/$\overline{\text{PWDN}}$ pin is also used to synchronize multiple devices in SPI interface mode or frame-sync slave mode.

When synchronizing multiple devices, the master clock, f_{clk}, must be shared from the same signal source.

9.1.3 ADC Input Driver

The input driver circuit for a high-precision delta-sigma ADC consists of two parts: a driving amplifier and a low-pass, antialiasing filter. The amplifier is used to condition the input signal voltage and provide a low output-impedance buffer between the signal source and the switched-capacitor inputs of the ADC. The low-pass antialiasing filter, comprised of series resistors and a differential capacitor, helps to attenuate the voltage transients created by the ADC switched-capacitor input stage, and also serves to band-limit the wideband noise contributed by the front-end circuit. Careful design of the input driver circuit is critical to take advantage of the linearity and noise performance of the ADS127L01.

9.1.3.1 Antialiasing Filter

Signal aliasing in data-acquisition systems occurs when continuous-time signals are discretely sampled at a constant rate. To properly represent an analog signal in the digital domain, the system must sample the input at a sampling rate greater than twice the maximum frequency content, known as the Nyquist rate. Frequencies that are greater than one-half the sampling rate are not represented properly in the digital domain and appear as aliases of the original input instead.

Delta-sigma ADCs exhibit two Nyquist frequencies, as shown in Figure 109. The first Nyquist frequency occurs in the analog domain at one-half the modulator sampling rate (f_{MOD} / 2). The second Nyquist frequency occurs in the digital domain at one-half the decimated output data rate (f_{DATA} / 2). Frequency content repeats at multiples of f_{MOD} and f_{DATA}. Both Nyquist frequencies allow for out-of-band signals to alias into the ADC pass band, including noise from the front-end driver circuit. This aliasing increases the in-band noise level of the system and degrades overall performance if not adequately filtered.

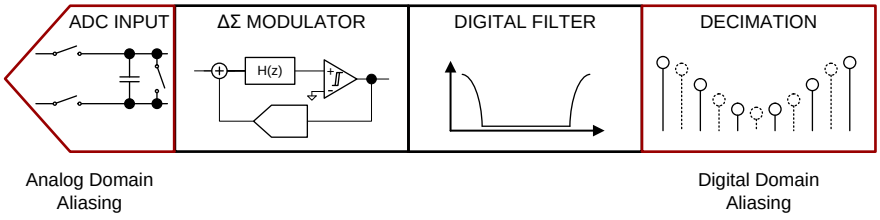


Figure 109. Delta-Sigma ADC Internal Signal Chain

Application Information (continued)

Figure 110 and Figure 111 illustrate the two aliasing domains in delta-sigma ADCs. Figure 110 shows a higher-frequency, out-of-band signal aliasing around the modulator Nyquist frequency (f_{MOD} / 2) into the pass band. Figure 111 shows a lower-frequency, out-of-band signal aliasing around the data rate Nyquist frequency (f_{DATA} / 2) into the pass band after being attenuated by the digital filter.

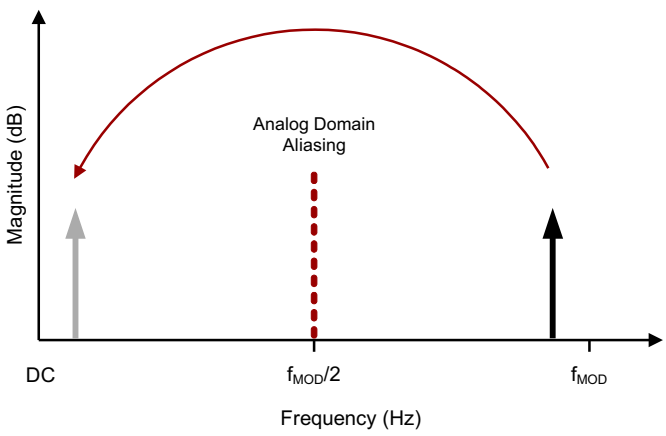


Figure 110. Analog Domain Aliasing Around f_{MOD} / 2

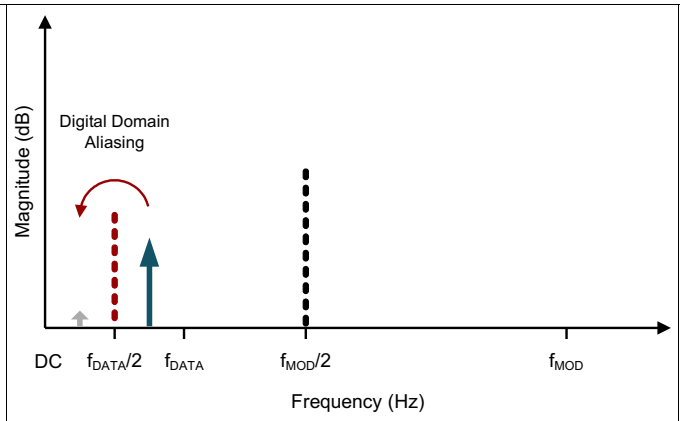


Figure 111. Digital Domain Aliasing Around f_{DATA} / 2

To prevent signals from aliasing, use a low-pass antialiasing filter to attenuate the out-of-band signals. The simplest antialiasing filter is a discrete first-order, low-pass, RC filter. To achieve a higher level of attenuation at the Nyquist frequency requires a higher-order filter response, usually before the last amplifier stage.

The digital filter in delta-sigma ADCs reduces the attenuation requirement of the antialiasing filter by providing a high stop-band attenuation between f_{DATA} / 2 and f_{MOD}. At multiples of f_{MOD}, the digital filter response returns to 0 dB and repeats. This portion of the digital filter response is the sensitive frequency band where an antialiasing filter is needed. Figure 112 overlays a digital filter response with first-, second-, and third-order antialiasing filters, attenuating both out-of-band signals.

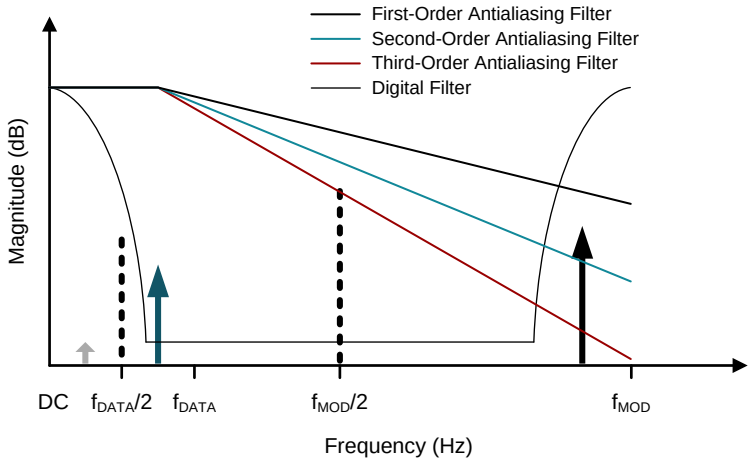


Figure 112. Antialiasing and Digital Filters

Application Information (continued)

The antialiasing RC filter also helps to attenuate the voltage transients from the sampling network at the ADC inputs. Figure 113 shows a simplified switch-capacitor circuit at the inputs of an ADC modulator. The sampling network, described in Figure 60, places a transient load on the external drive circuit. The differential capacitor in the RC filter, C_{DIFF}, acts as a charge reservoir and transfers charge to the internal sampling capacitor, C_{SAMPLE}, while S1 is closed. The input driver circuit must restore the charge at the input nodes (AINP and AINN) so that the voltage settles before S1 opens. After S1 opens, S2 closes, discharging the C_{SAMPLE} capacitor. The faster the modulator sampling rate, the less time the input voltage has to settle. An amplifier with a gain-bandwidth product (GBP) that is too low fails to provide adequate settling because of the higher output impedance over frequency, and results in increased distortion.

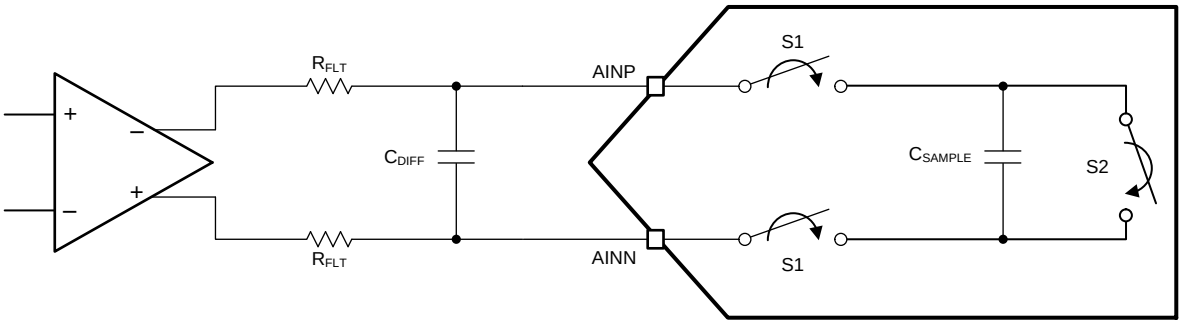


Figure 113. Delta-Sigma Modulator Sampling Network

The sampling capacitors of the ADS127L01 have an equivalent capacitance of 8 pF. Scale C_{DIFF} to be at least 100 times larger than C_{SAMPLE}. Connect C_{DIFF} directly across the ADC input pins to help provide adequate charge with each ADC sample. C_{DIFF} must be C0G or NP0 dielectric type because these components have a high-Q, low-temperature coefficient, and stable electrical characteristics to withstand varying voltages and frequencies. Common-mode capacitors, C_{CM}, can also be added at each input to ground to attenuate common-mode noise and sampling glitches. Size the common-mode capacitors to be one order of magnitude smaller than C_{DIFF} in order to maintain system common-mode rejection (CMR).

Figure 114 shows an example of the voltage transient created by the ADC sampling event at the inputs of an unbuffered delta-sigma ADC. The larger transients mark the moment when S1 closes to connect C_{SAMPLE} to the external front-end circuitry. The smaller transient occurs when the S1 switch opens passing the charge through the modulator. The sequence repeats at 1 / f_{MOD}. The data were recorded using a passive 10x probe on the AINP pin only. The same transient is observed on AINN as well. The differential transient voltage is more than an order of magnitude smaller.

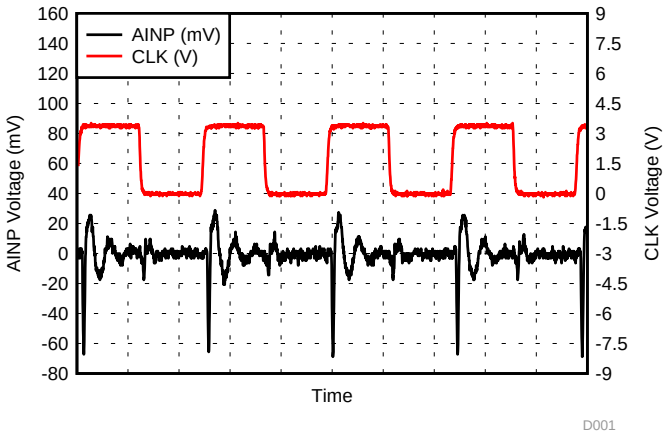


Figure 114. ADC Input During Sampling

Application Information (continued)

When S1 opens, the input signal is sampled and converted by the modulator. Increasing C_{DIFF} provides a larger charge reservoir to the ADC, and reduces the initial voltage droop. For ADCs with a faster sampling frequency, there is less time for this voltage transient to fully settle before the next sample. The ADC input relies on a driver amplifier with sufficient bandwidth and low output impedance at high frequencies to provide recovery charge and fully settle the voltage transient before S1 opens.

9.1.3.2 Input Driver Selection

Selection criteria for the input amplifiers are highly dependent on the input signal type, as well as the performance goals of the data-acquisition system. Consider the following amplifier specifications when selecting the appropriate driver amplifier for the application:

- *Noise*. The output noise density of the front-end amplifiers must be kept as low as possible to prevent any degradation in system SNR performance. The total noise from the input stage is determined by the –3-dB bandwidth of the ADS127L01 digital filter. Make sure that the total output noise is less than 20% of the input-referred noise of the ADC, as explained in Equation 12:

$$e_{o\_RMS} \times \sqrt{f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (12)$$

  where
  - e_{o_RMS} = Broadband output noise of the input driver stage in nV/√Hz
  - f_{-3dB} = –3-dB bandwidth of the ADS127L01 digital filter in Hz

- *Distortion*. Keep the distortion from the front-end drivers as low as possible, especially in the presence of a switching load. Harmonics produced by the amplifier are also compounded by harmonics produced by the ADC. Minimize the amplifier distortion by using the widest allowable supply voltage and highest output load resistance for the application. Select an amplifier with high open-loop gain and at least –10 dB better distortion than the ADC distortion in order to prevent any degradation to system THD performance, as explained by Equation 13.

$$THD_{AMP} \leq THD_{ADC} - 10 \text{ dB} \quad (13)$$

  where
  - THD_{AMP} = Total harmonic distortion from input driver
  - THD_{ADC} = Total harmonic distortion specification of the ADC

- *Small-signal bandwidth*. Select the small-signal bandwidth of the input amplifiers to be as high as possible, after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive a larger capacitive load with a smaller series resistor. For a given low-pass filter cutoff, keep the series resistor as small as possible and increase the differential capacitor to minimize gain error and distortion (see the *Antialiasing Filter* section). Higher bandwidth also minimizes harmonic distortion caused by faster settling of the input transients from the ADC sampling. The required amplifier bandwidth depends on the size of the sampling capacitor, the sampling frequency, and the size of the external differential capacitor. TINA-TI simulations help model the small-signal settling behavior and the stability of the input driver circuit for a given load.

The THS45xx family of fully-differential amplifiers offers the low noise and distortion specifications needed in high-performance data-acquisition systems. Table 30 shows the power versus performance tradeoff offered between the THS4531A, THS4551, and the highest performing THS4541.

Table 30. Input Driver Selection

DRIVER	GAIN BANDWIDTH PRODUCT (MHz)	NOISE DENSITY (nV/√Hz)	QUIESCENT CURRENT Iq (mA)	NOMINAL R_F AND R_G (Ω)
THS4531A	36	10	0.23	2 k
THS4551	135	3.4	1.31	1.2 k
THS4541	850	2.2	9.7	402

Figure 115 and Figure 116 compare the distortion and noise performance of the THS4531A, THS4541, and THS4551 as they drive the inputs of the ADS127L01. Each input driver circuit was configured for a gain of one using the nominal feedback resistor values in Table 30. An AP2700 function generator provided a full-scale, sine wave input at frequencies of 2 kHz and below, such that at least five harmonics were present in the fast Fourier transform (FFT) calculated from 8,192 samples. An Agilent 33522A provided the clock input for the ADS127L01 (CLK) to set the modulator clock frequency between 100 kHz and 16.384 MHz.

To quantify the distortion performance of each input driver circuit, the spurious-free dynamic range (SFDR) is calculated at each modulator clock frequency. A third-order polynomial, best-fit curve is applied to the raw data to show the overall trend for each amplifier.

Figure 115 illustrates that at slower modulator clock frequencies, a lower power amplifier with less bandwidth can be used to achieve similar SFDR performance as higher power amplifiers with more bandwidth. However, faster modulator clock frequencies require the use of a wide-bandwidth amplifier to get the best performance out of the ADC.

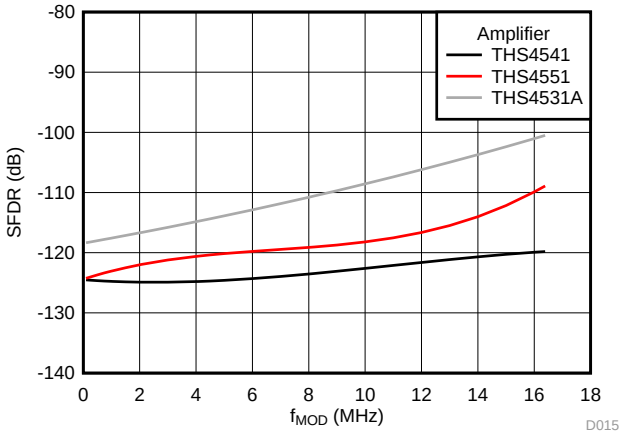


Figure 115. SFDR vs f_{MOD}

In contrast to SFDR, the signal-to-noise ratio (SNR) of a data-acquisition signal chain is more dependent on the input amplifier noise density, as well as the ADC output data rate. Figure 116 displays the SNR performance of the ADS127L01 measured while driving the inputs with the THS4531A, THS4541, and THS4551. The digital filter in the ADS127L01 is configured to use the Wideband 2 transition band and an OSR of 256 throughout the SNR measurements. An AP2700 provided a small-signal 1 kHz input sine wave of 100 mVpp. An Agilent 33522A provided the clock input (CLK) for the ADS127L01 to set the modulator clock frequency between 100 kHz and 16.384 MHz. The measured SNR is normalized to full-scale.

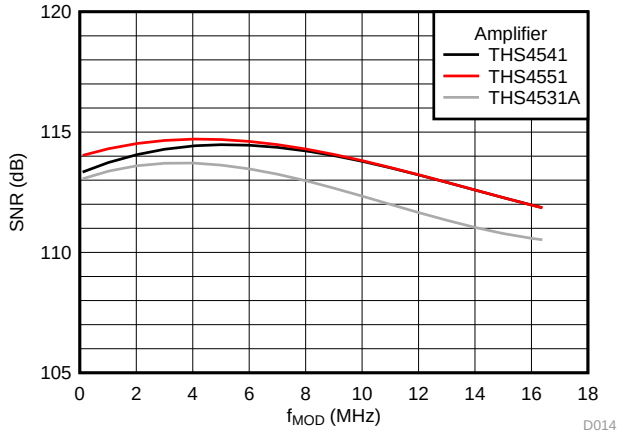


Figure 116. SNR vs f_{MOD}

The SNR performance is expected to remain relatively constant for all three amplifiers across modulator frequencies. However, the improvement in SNR at slower modulator frequencies is because of the reduced bandwidth of the digital filter as it scales down with modulator clock, limiting the input source broadband noise. At higher frequencies, noise from the input source dominates as the digital-filter bandwidth increases. The difference in amplifier noise density, listed in Table 30, has the largest effect on the system noise performance.

9.1.3.3 Amplifier Stability

Driving a capacitive load can degrade the phase margin of the input amplifier, and can make the amplifier unstable. To prevent the amplifier from becoming unstable, a series isolation resistor (R_{FLT}) is used at the amplifier output, as shown in Figure 113. A higher resistance value increases phase margin and makes the amplifier more stable, but also increases distortion caused by the interaction with the nonlinear input impedance of the ADC modulator. Distortion increases with source output impedance, input-signal frequency, and input-signal amplitude.

The selection of R_{FLT} requires a balance between distortion and the stability of the input driver design. The use of 1% components is allowed because the C_{DIFF} mitigates the degradation of CMR caused by input imbalances.

The input amplifier must be selected with a bandwidth higher than the cutoff frequency, f_C, of the antialiasing filter at the ADC inputs. Use a TINA-TI simulation to confirm that the amplifier has more than 30° of phase margin when driving the selected filter to verify stability. Simulation is critical because some amplifiers require more bandwidth than others to drive the same filter. If the input amplifier circuit has less than 20° of phase margin, consider adding a capacitor at the amplifier inputs to increase phase margin.

9.1.4 Modulator Saturation

The ADS127L01 features a third-order modulator and a 5-bit quantizer in order to achieve excellent SNR performance, resolution, and linearity. However, as with all high-order, delta-sigma modulators, certain input conditions may saturate the modulator and increase the quantization noise. These conditions include input signals that are less than full-scale and contain frequency content that falls within the stop band of the digital filter. Most notably, a saturated modulator increases the ADC in-band noise floor and degrades SNR performance.

To prevent the ADS127L01 from reaching a saturated condition, use an antialiasing filter at the inputs to attenuate out-of-band signals. Table 31 shows the differential input amplitude limits at frequencies from 100 kHz to 15 MHz for discrete modulator rates in order to prevent saturation. In general, a multiple-order, low-pass response with a –3-dB cutoff placed one decade beyond the pass band is sufficient for most applications.

Table 31. Differential Input Amplitude Limits (dBFS)

f_{IN} (MHz)	f_{MOD}			
	4.096 MHz	8.192 MHz	12 MHz	16.384 MHz
0.1	0	—	—	—
0.2	0	0	—	—
1	–3	–2	–2	–2
2	–7	–6.5	–3	–2.5
8	–18	–18	–18	–18
10	–19	–19	–19	–19
15	–20	–20	–20	–20

9.1.5 ADC Reference Driver

Design the reference driver to provide a precision, low-drift reference voltage to the ADC for best performance. Similar to the input of the ADC, a switched-capacitor circuit samples the reference voltage between REFP and REFN. The switched capacitor imposes a transient load on the external reference driver circuit at the modulator frequency. A reference buffer is required to restore the charge across the differential capacitor at the reference input pins so that the voltage settles before the next acquisition. The integrated broadband reference noise must remain significantly less than the ADC integrated noise to minimize SNR degradation. Choose a reference driver with relatively low noise density. Reference noise can be heavily filtered with a low-pass filter.

Below are two options for driving the reference input of the ADS127L01. Option 1 presents a single-chip solution with an integrated buffer. Option 2 presents a multichip solution with a precision reference and an external buffer.

9.1.5.1 Single Chip Solution: REF6xxx

The REF6xxx is a family of very high-precision, low-noise, and low-drift voltage references. This single-chip solution has an integrated high-bandwidth buffer that presents a low output impedance to the ADC reference input. The REF6025 outputs a fixed 2.5-V output voltage; however, other devices from the same family are available to offer various output voltages and temperature drift specifications

The ADS127L01 has the ability to maintain a high level of performance at relatively low levels of power consumption. The REF6025 only adds 750 μA of typical quiescent current to the system power budget, while still showcasing the performance of the ADS127L01 when sampling at full-speed, making it a great fit for low-power applications with limited board space.

Figure 117 shows typical connections for the REF6025 as a reference driver circuit to the ADS127L01. The output of the REF6025 uses a Kelvin connection to correct for the voltage drop between the voltage output pins and the pads of the output capacitor. A small series resistance is required to keep the reference output stable. See the REF60xx device datasheet (SBOS708) for more details on the required connections and component values.

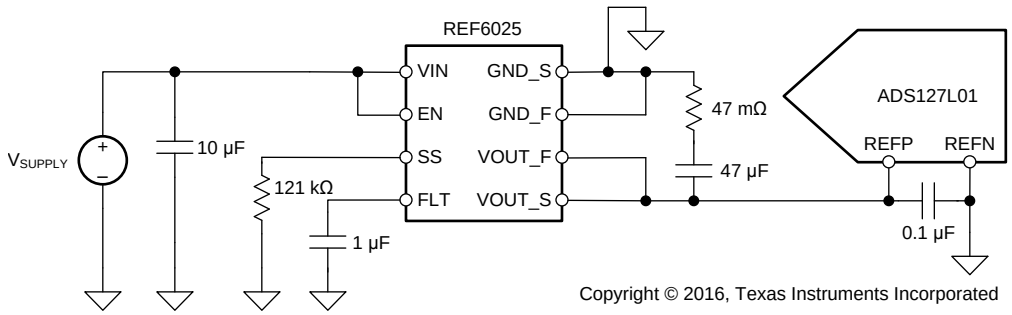


Figure 117. REF6025 Connection to ADS127L01

9.1.5.2 Multichip Solution: REF50xx + OPA320

The REF50xx is another family of low-noise, low-drift, high-precision voltage references. The REF5025 outputs a fixed 2.5-V output voltage; however, other devices from the same family are available to offer various output voltages. Buffer the output of the REF5025 with a low-noise, wide bandwidth amplifier such as the OPA320 to achieve the best performance with the ADS127L01.

The OPA320 is a precision, low-voltage CMOS operational amplifier optimized for low noise and wide bandwidth with a typical quiescent current of 1.5 mA. From 0.1 Hz to 10 Hz, the OPA320 features an output noise of 2.8 μV_{PP}. With a unity gain-bandwidth product of 20 MHz, the OPA320 is able to drive the ADS127L01 reference inputs while sampling at full-speed without degrading linear performance of the system.

Figure 118 shows an example reference circuit using the REF5025 and the OPA320. The output of the REF5025 is low-pass filtered to less than 2 Hz before the input of the OPA320. The OPA320 is placed in a noninverting buffer configuration with dual-feedback to compensate for the large capacitive output load and maintain stability. See the respective device data sheets for more details on the required connections and component values.

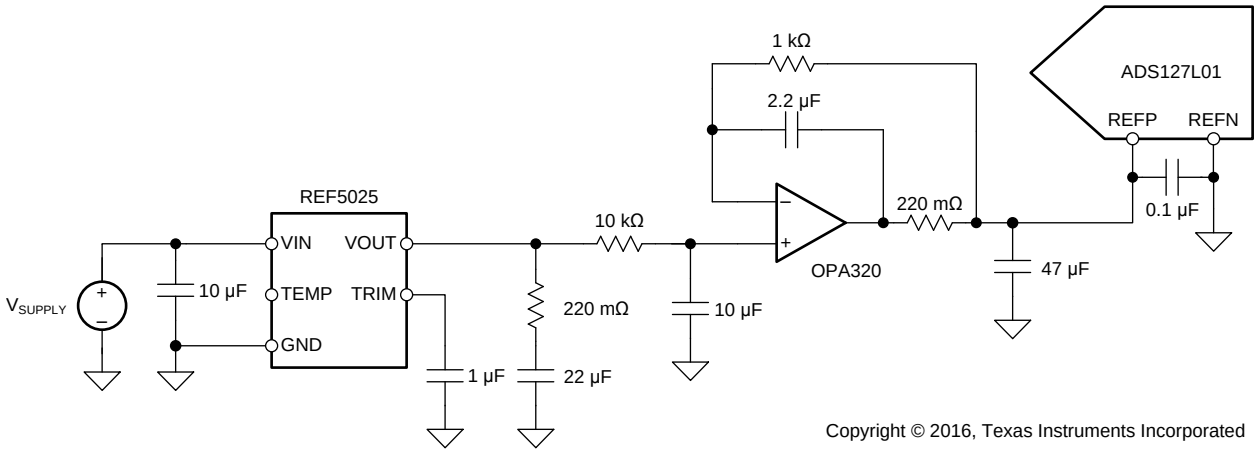


Figure 118. REF5025 + OPA320 Connection to ADS127L01

Table 32 compares the performance characteristics of the two reference driver solutions discussed in this section.

Table 32. Reference Selection

DEVICE	I_Q (µA)	TEMPERATURE DRIFT TYP (µV/°C)	TEMPERATURE DRIFT MAX (µV/°C)	NOISE (μV_{PP})(1)	TEMPERATURE RANGE (°C)
REF5025 + OPA320	2300	8.0	22.9	9.04	-40°C to +125°C
REF6025	750	7.5	12.5	20.53	-40°C to +125°C
REF6125	750	10.0	20	20.53	-40°C to +125°C

(1) Total noise for 230 kHz ADC bandwidth simulated from TINA-TI.

The two reference solutions are capable of driving the ADS127L01 to meet datasheet specifications. While the multichip solution has a larger PCB footprint, the multichip solution offers similar noise performance, and allows more customization than the REF6x25, including the ability to low-pass filter the broadband noise of the REF5025. This multichip solution may provide a lower-cost alternative to the REF6x25 for applications that can tolerate a higher component count and power consumption. The REF6x25 has a smaller PCB footprint, and offers tighter drift specifications at a fraction of the power.

9.1.6 Driving LVDD With an External Supply

A portion of the ADC modulator in the ADS127L01 is powered from a separate low-voltage analog supply (LVDD) to achieve lower overall power consumption. This supply is nominally 1.8 V and can be sourced by either an internal LDO ($\overline{\text{INTLDO}}$ = 0) or an external supply ($\overline{\text{INTLDO}}$ = 1). When the internal LDO supply is used, the LVDD current is sourced from AVDD.

While LDOs are known to be smaller and less noisy than other power supply topologies, LDOs are much less efficient and can consume large amounts of power. An LDO dissipates excess power as heat in order to regulate the output voltage. The higher the dropout voltage is between the supply input and the LDO output, the more power is wasted.

Alternatively, an external switching power supply can drive LVDD. Switching power supplies are much more efficient and consume less power; however, a small switching ripple could appear on the output. The frequency content from this ripple can appear in the ADC output if:

- The switching frequency falls *directly* in the ADC pass band.
- The switching frequency *aliases* into the ADC pass band from an out-of-band frequency.

Consider carefully when choosing the switching frequency (f_{SW}) in order to maintain the highest system power-supply rejection (PSR). The LVDD supply pin offers at least 75 dB of PSR at 60 Hz. Choose an out-of-band switching frequency that falls within the stop band of the wideband FIR filter, or within the notches of the low-latency sinc filter, as shown in Figure 119 and Figure 120, respectively. If possible, an ideal design synchronizes the switching supply frequency to a $1/2^n$ ratio of the modulator clock frequency. Any remaining frequency content that is not suppressed by the LVDD PSR will fall into the nulls of the digital filter or fold back to dc.

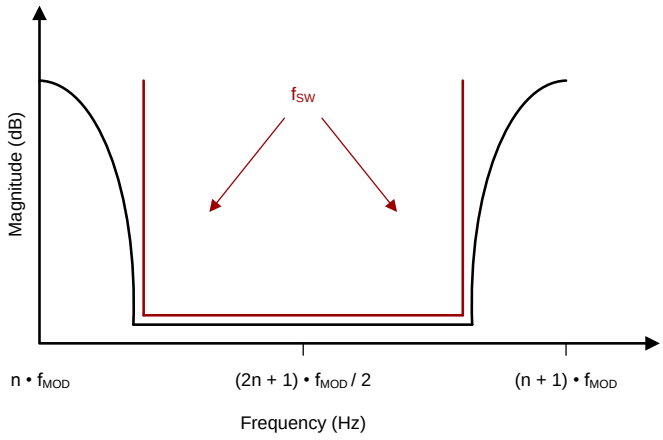


Figure 119. Suggested f_{SW} for Wideband Filters

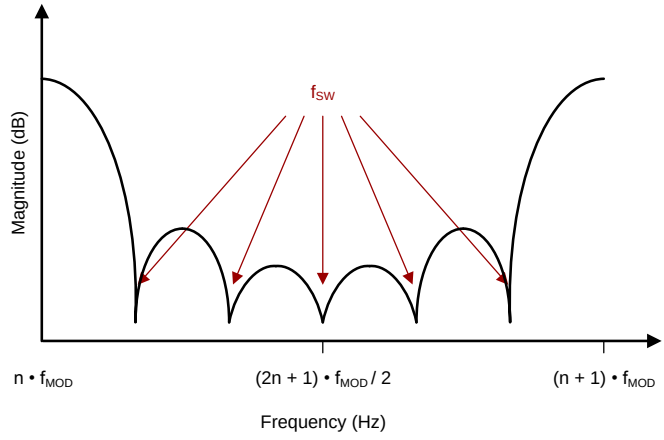


Figure 120. Suggested f_{SW} for Low-Latency Filter

9.2 Typical Application

Test and measurement applications interface sensor inputs with a precision data-acquisition signal chain. This signal chain must be capable of measuring a wide frequency range with very low noise and minimal harmonic distortion. Figure 121 illustrates the main components of a sensor signal chain, consisting of a conditioning stage at the sensor output, followed by a high-speed, low-noise amplifier driving a wide-bandwidth, delta-sigma ADC.

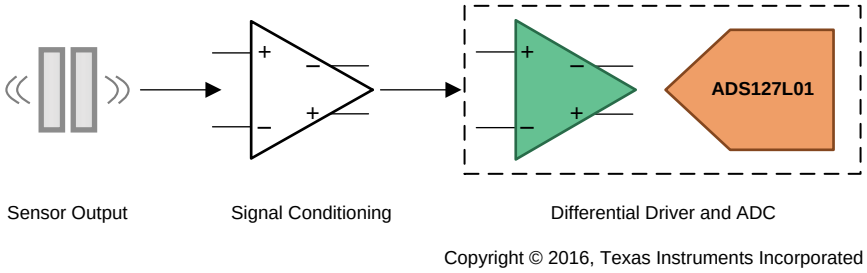


Figure 121. Test and Measurement Block Diagram

In data-acquisition systems, signal distortion can come from the amplifier, the settling of the switched-capacitor load transients, and the ADC. Choose both the differential drive amplifier and the ADC such that neither one limits the distortion performance of the signal chain. This section details the design procedure for the fully-differential input stage to an ADC optimized for low noise and minimal harmonic distortion.

9.2.1 Design Requirements

Table 33. Design Requirements

DESIGN PARAMETER	VALUE
Analog supply voltage	3.0 V
Modulator sampling frequency (f_{MOD})	16 MHz
Filter pass band	DC to 100 kHz (f_{DATA} = 250 kSPS)
Antialiasing filter rejection	–100 dB at f_{MOD}
Total harmonic distortion (THD)	–110 dB at –0.5-dBFS input signal amplitude
Signal-to-noise ratio (SNR)	70 dB at 100-mV input signal amplitude (104 dB normalized to 2.5-V full-scale)
Power consumption	20 mA (50 mW) ADS127L01, input drive amplifier, reference device + drive amplifier

9.2.2 Detailed Design Procedure

The ADS127L01 offers a typical THD level of –110 dB for a modulator frequency of 16.384 MHz. Target the distortion from the input driver to be at least 10 dB better than the distortion of the ADC. The THS4551 provides exceptional ac performance with extremely low distortion levels near –120 dB. With a 135-MHz gain-bandwidth product, the THS4551 can drive the switched-capacitor input stage so that the load transients are mostly settled. For higher levels of performance, use a faster amplifier with more bandwidth as long as the increased current consumption fits within the system power budget. At 3.4 nV/√Hz broadband noise density and 1.35 mA of quiescent current, the THS4551 offers an attractive performance versus power tradeoff that is well-suited for these applications.

Single-ended inputs have a varying input common-mode, and can produce larger even harmonics and decrease distortion performance. Use a fully-differential input to the ADC to help suppress even harmonics and provide a fixed common-mode voltage for the input signal.

For this design, the THS4551 is placed in a multiple-feedback (MFB) filter configuration, as shown in Figure 122. Nominal resistance values of 1.2 kΩ are used in the amplifier feedback path to optimize power consumption, while keeping the added broadband noise of the front-end driver circuit less than that of the ADS127L01. An MFB filter produces a second-order, low-pass response.

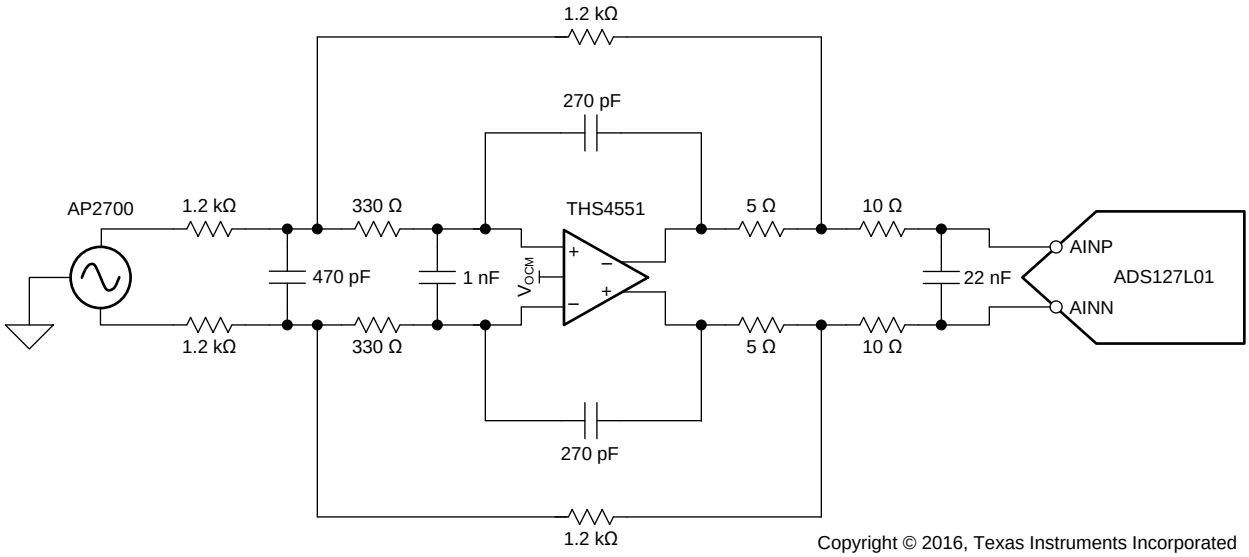


Figure 122. Multiple Feedback ADC Drive Circuit

The discrete low-pass RC filter components (10 Ω and 22 nF) are small enough to increase the antialiasing filter rolloff without adding significant distortion or gain error to the system. Combined with the active MFB filter, the net result is a third-order antialiasing filter. Figure 123 plots the magnitude response of the front-end driver circuit and illustrates how it supplements the Wideband 2 FIR filter in the ADS127L01.

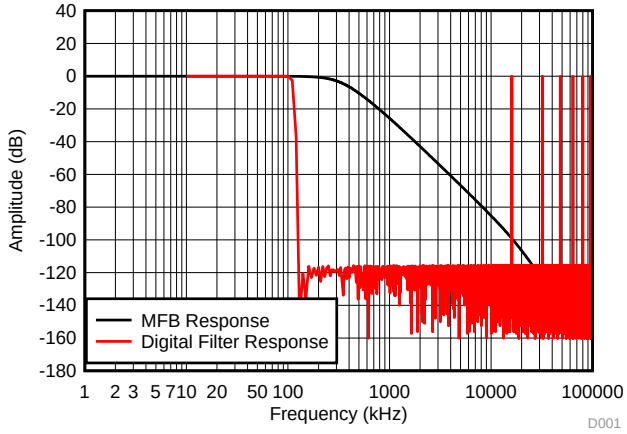


Figure 123. THS4551 MFB Filter Magnitude Response

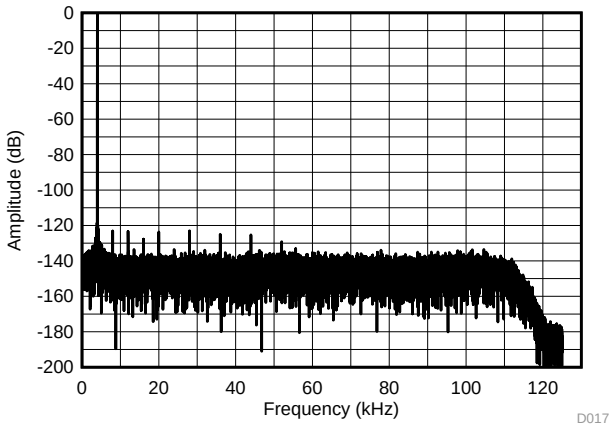
The response of the third-order antialiasing filter remains flat beyond the digital filter pass band. Signals within the bandwidth of interest are left unattenuated by the antialiasing filter. The Wideband 2 filter is used to provide an average stop-band attenuation of –116 dB beginning at f_{DATA} / 2. This transition band prevents signals from aliasing in the digital domain.

At f_c = 304 kHz, the antialiasing filter reaches –3 dB, and rolls off sharply at a rate of –60 dB per decade. At 16 MHz, the filter response reaches –100 dB of attenuation, effectively eliminating unwanted frequency content around the modulator rate. The antialiasing filter attenuates the frequency content that alias around the modulator Nyquist frequency (f_{MOD} / 2). The REF6025 circuit proposed in Figure 117 was selected to drive the ADS127L01 reference. This device enables the design to meet the outlined performance goals while remaining within the target power budget.

9.2.3 Application Curves

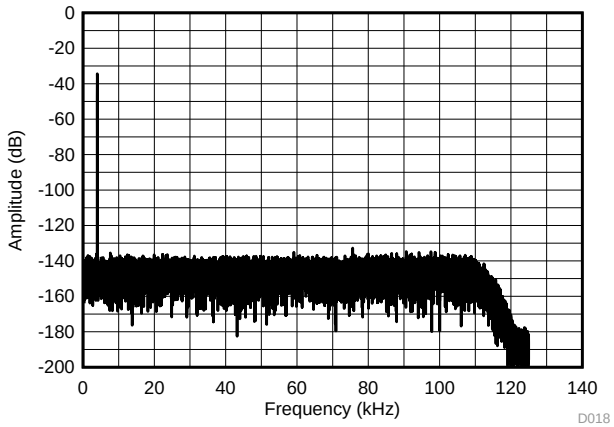
Figure 124 shows a fast Fourier transform (FFT) of the 32,768 samples collected at 250 kSPS (OSR 64). An AP2700 generated a 4-kHz sine wave with a differential amplitude of –0.5 dB below full-scale (±2.36 V). The fundamental input frequency at 4 kHz is the dominate tone in the FFT. The first 15 harmonics are used to calculate the total harmonic distortion (THD) as –114.4 dB. The input amplifier and the antialiasing filter do not degrade the overall distortion performance of the signal chain.

SNR was measured with a small-signal 100 mV_{PP} (–34 dB from full-scale) input sine wave generated by the AP2700. The SNR result is the difference in magnitude between the fundamental frequency and the integrated noise of the ADC output up until f_{DATA} / 2. Figure 125 shows the FFT of the 32,768 samples collected at 256 kSPS (OSR = 64). The result is then normalized to full-scale to yield 106.3 dB.



f_{IN} = 4 kHz, amplitude = –0.5 dBFS, THD = –114.4 dB

Figure 124. THD Results

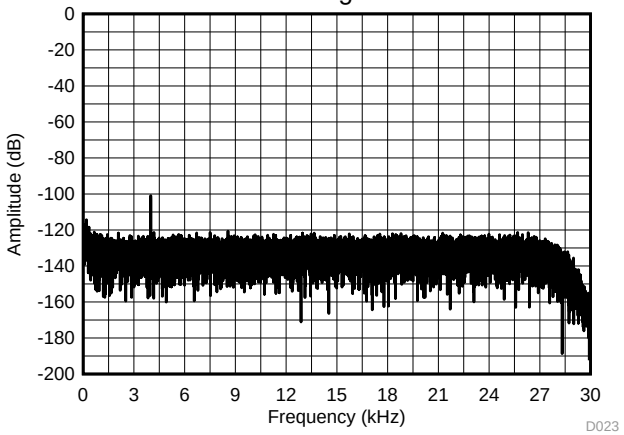


f_{IN} = 4 kHz, amplitude = 100 mV_{PP}, SNR = 106.3 dB (normalized to FS)

Figure 125. SNR Results

To verify the effectiveness of an antialiasing filter, input a sine wave at the frequency of interest and measure how much that signal is attenuated at the output. In order to measure the attenuation at f_{MOD} = 16 MHz, input a signal around or at that frequency and measure the alias of the signal that folds into the ADC pass band.

Figure 126 shows the FFT results of the 32,768 samples collected at 64 kSPS (OSR 256) for finer frequency bin resolution. An Agilent 33522A was used to generate a differential -0.5 dBFS sine wave input at 16.004 MHz. Because 16.004 MHz is offset from 16 MHz (f_{MOD}) by 4 kHz, the input signal aliases to 4 kHz. The magnitude of the frequency tone is the attenuation level of the antialiasing filter.



f_{MOD} = 16 MHz, f_{IN}= 16.004 MHz, amplitude = –0.5 dBFS, OSR = 256 (64 kSPS)

Figure 126. Antialiasing Filter Attenuation Results

Table 34 lists the typical current consumption and power dissipation for the ADS127L01, the THS4551, and the REF6025.

Table 34. Power Consumption

COMPONENT	QUIESCENT CURRENT (mA)	POWER DISSIPATION (mW)
ADS127L01 (AVDD)	10.6	31.8
ADS127L01 (DVDD)	4.4	7.8
THS4551	1.3	3.9
REF6025	0.8	2.3
TOTAL	**17.1**	**45.8**

9.3 Do's and Don'ts

- Do partition the analog, digital, and power supply circuitry into separate sections on the printed circuit board (PCB).
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.
- Do verify that the analog input voltages are within the specified input voltage range under all input conditions.
- Do tie unused digital input pins to DGND to minimize input leakage current.
- Do use an LDO to reduce voltage ripple generated by switch-mode power supplies.
- Do synchronize clock signals and switching supply frequencies to minimize intermodulation artifacts and noise degradation.
- Don't cross analog and digital signals.
- Don't route digital clock traces in the vicinity of the analog inputs or CAP1 and CAP2 analog bias voltages.
- Don't allow the analog and digital power supply voltages to exceed 3.9 V under any condition, including during power-up and power-down.
- Don’t use inductive supply or ground connections.
- Don’t isolate analog ground (AGND) from digital ground (DGND).

Figure 127 illustrates examples of correct and incorrect ADC circuit connections.

Do's and Don'ts (continued)

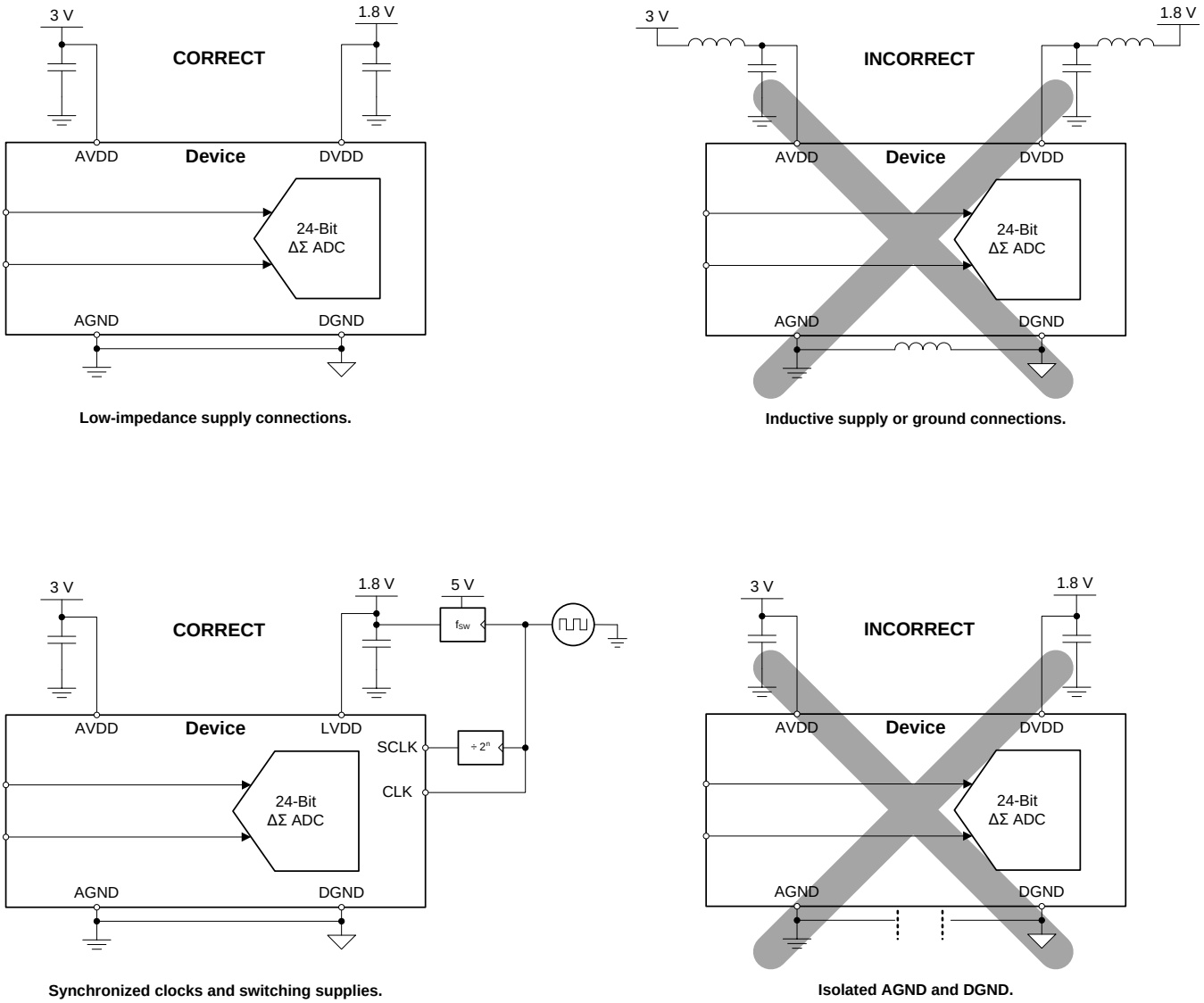


Figure 127. Correct and Incorrect Circuit Connections

9.4 Initialization Setup

Figure 128 illustrates a general procedure to configure the ADS127L01 to collect data.

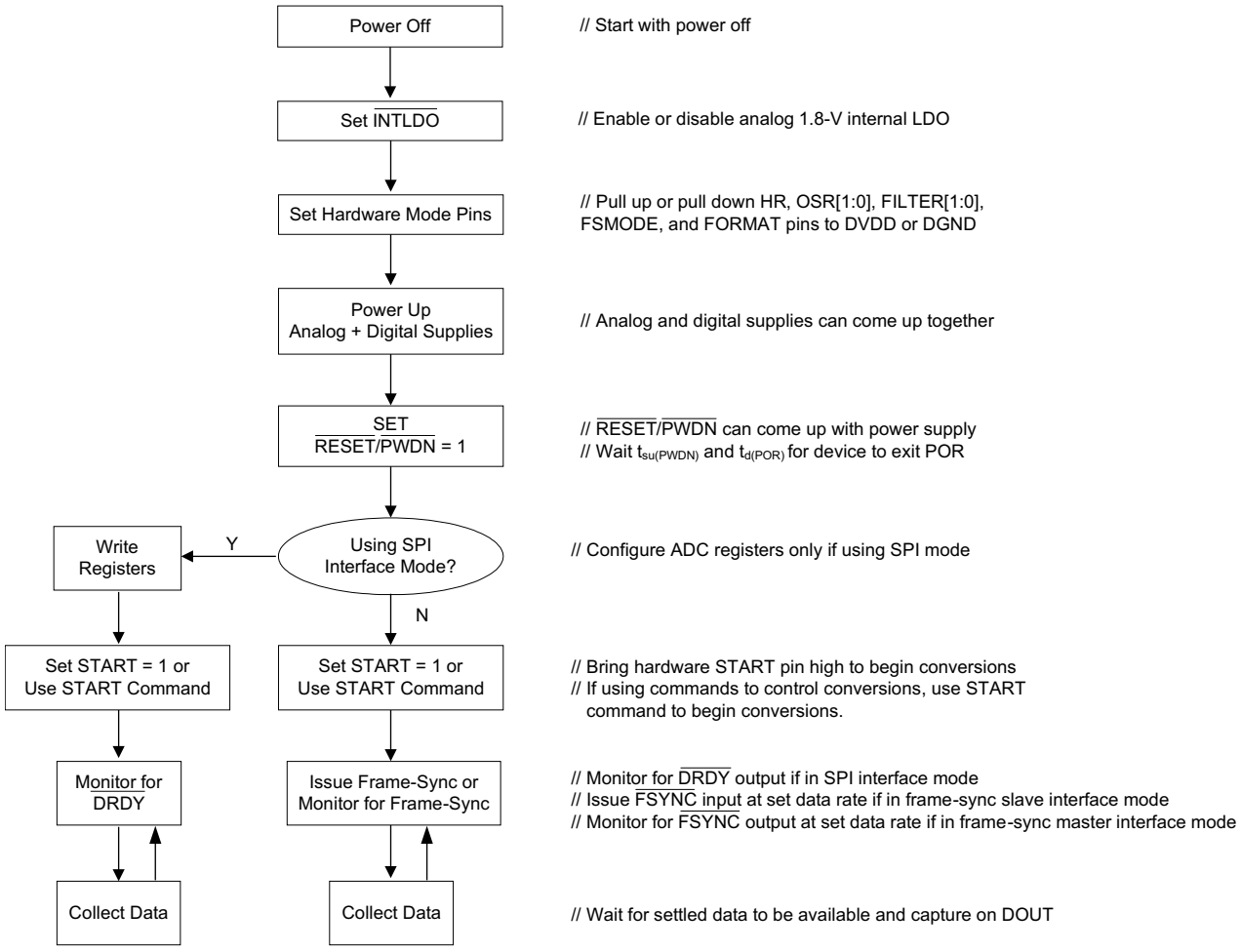


Figure 128. ADS127L01 Configuration Sequence

10 Power Supply Recommendations

The ADS127L01 requires either two or three power supplies, depending on if the internal LDO is used to supply the LVDD analog supply. The AVDD analog supply is referenced to AGND, the LVDD analog supply is referenced to AGND, and the DVDD digital supply is referenced to DGND. The analog power supply can only be unipolar (for example, AVDD = 3.0 V, AGND = 0 V) and is independent of the digital power supply. If $\overline{\text{INTLDO}}$ = 0, the LVDD supply is internally generated using the AVDD supply. If $\overline{\text{INTLDO}}$ = 1, the internal LDO is disabled and LVDD supply must be externally supplied. The digital supply sets the digital I/O levels.

10.1 Power-Supply Sequencing

The power supplies can be sequenced in any order, but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage limits. Bring the $\overline{\text{RESET}}/\overline{\text{PWDN}}$ pin high after the analog and digital supplies are up, or bring the pin high with the DVDD supply (assuming the AVDD and LVDD supplies come up with or before DVDD). After all supplies are stabilized, wait for the $t_{d(POR)}$ timing for the power-on-reset to complete before communicating with the device in order to allow the power-up reset process to complete.

10.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD, LVDD, and DVDD must be decoupled with at least a 1-µF capacitor, as shown in Figure 129. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. Use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoid the use of vias for connecting the capacitors to the device pins for superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Connect analog and digital ground together as close to the device as possible.

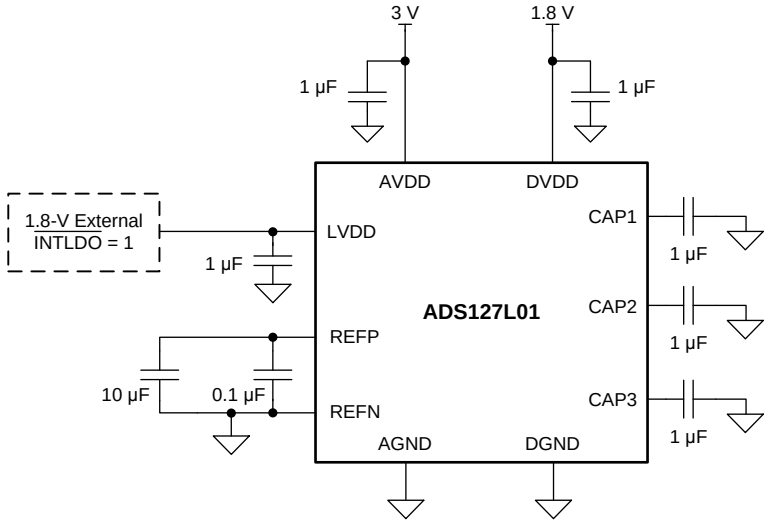


Figure 129. ADS127L01 Recommended Power-Supply Decoupling

11 Layout

11.1 Layout Guidelines

TI recommends employing best design practices when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog multiplexers] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio-frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 130. Although Figure 130 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design, and careful consideration must always be used when designing with any analog component.

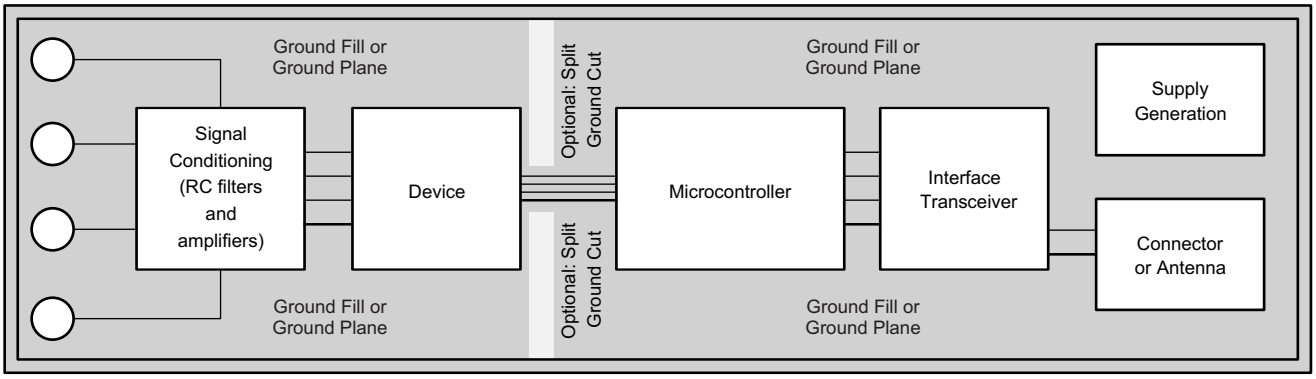


Figure 130. System Component Placement

The following bullet items outline some basic recommendations for the layout of the ADS127L01 to get the best possible performance of the ADC. A good design can be ruined with bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital traces away from analog traces. This separation prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but this split is not necessary. Place analog signals over the analog plane and digital signals over the digital plane. As a final step in the layout, completely remove the split between the analog and digital grounds. If ground plane separation is necessary, make the connection between AGND and DGND as close to the ADC as possible.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, the return current must find another path to return to the source and complete the circuit. If the return current is forced into a larger path, the chance is increased that the signal will radiate. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on power supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Flow the supply current through the bypass capacitor pins first and then to the ADC supply pins. Placing the bypass capacitors on the same layer close to the active device yields the best results. If multiple ADCs are on the same PCB, use wide power-supply traces or dedicated power-supply planes to minimize the potential of crosstalk between ADCs.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and the high-frequency impedance seen by the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor may create a parasitic thermocouple that can add an offset to the measurement. Match the differential inputs for both inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. The

Layout Guidelines (continued)

differential capacitors must be high quality. The best ceramic chip capacitors are C0G (NP0), with both stable properties and low noise characteristics.

- When REFN is tied to AGND, run the two traces separately as a star connection back to the AGND pin in order to minimize coupling between the power-supply trace and reference-return trace.
- It is important that the clock inputs are free from noise and glitches. Even with relatively slow clock frequencies, short digital-signal rise-and-fall times can cause excessive ringing and noise. For best performance, keep the digital signal traces short, use termination resistors as needed, and make sure all digital signals are routed directly above the ground plane with minimal use of vias.

11.2 Layout Example

Figure 131 is an example layout of the ADS127L01, input driver circuit, and reference driver circuit using four PCB layers. In this example, the top and bottom layers are used for analog and digital signals. The first inner layer is dedicated to the ground plane and the second inner layer is dedicated to the power supplies. The PCB is partitioned with analog signals routed on the left, and digital signals routed on the right. Polygon pours are used to provide low-impedance connections between the power supplies and the reference voltage for the ADC.

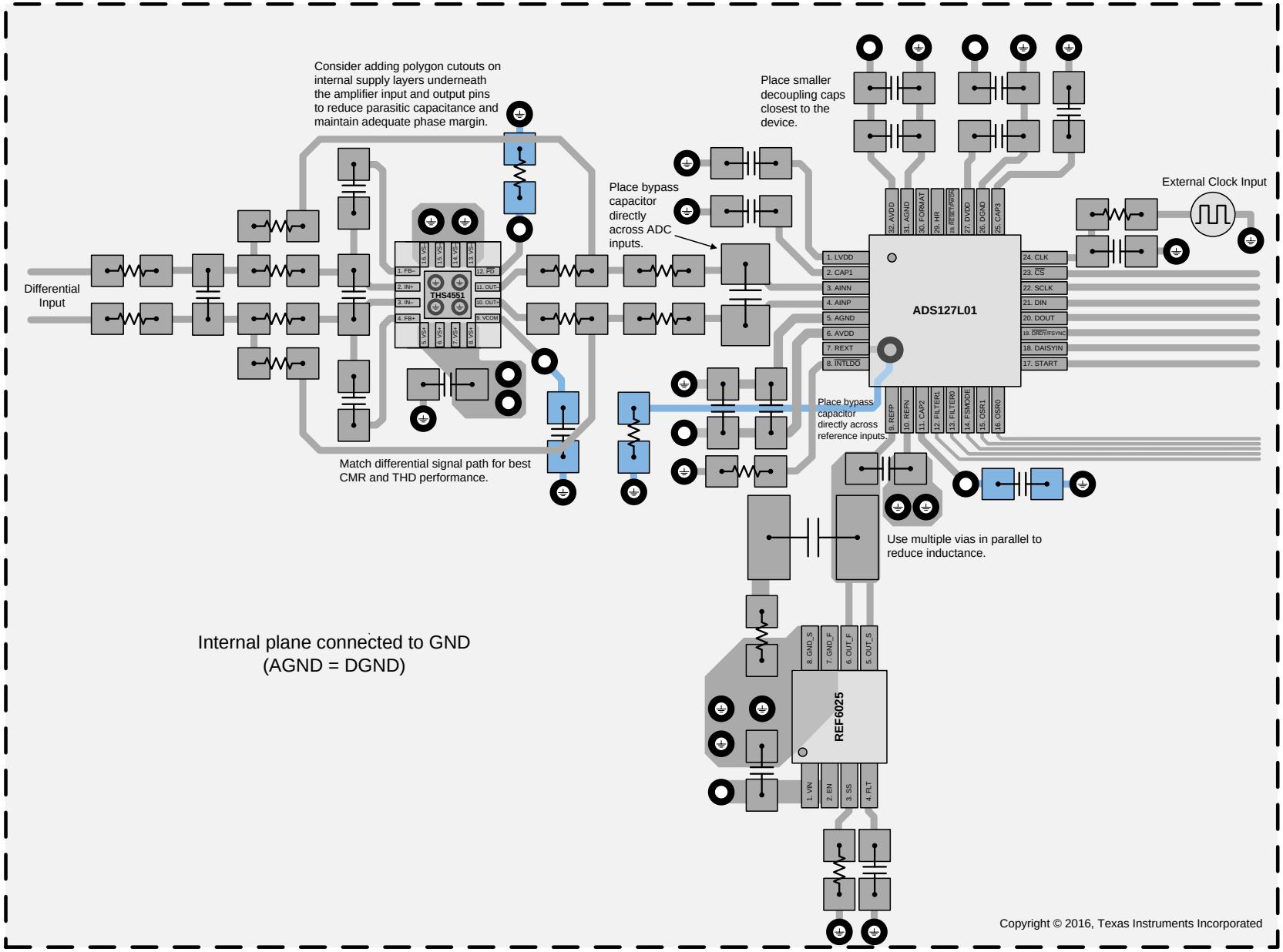


Figure 131. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *THS4541 Negative Rail Input, Rail-to-Rail Output, Precision, 850-MHz Fully Differential Amplifier* (SLOS375)
- *THS4551 Low-Power, Precision, 150-MHz, Fully-Differential Amplifier* (SBOS778)
- *THS4531A Ultra Low-Power, Rail-to-Rail Output, Fully Differential Amplifier* (SLOS823)
- *REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer* (SBOS708)
- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* (SBOS410)
- *OPA320 Precision, 20MHz, 0.9pA, Low-Noise, RRIO, CMOS Op Amp with Shutdown* (SBOS513)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
SPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS127L01IPBS	ACTIVE	TQFP	PBS	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	127L01	Samples
ADS127L01IPBSR	ACTIVE	TQFP	PBS	32	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	127L01	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

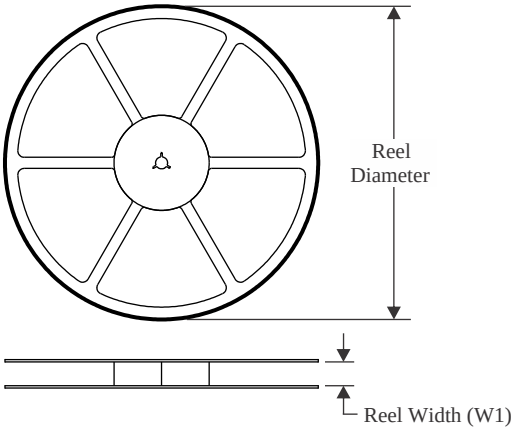
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

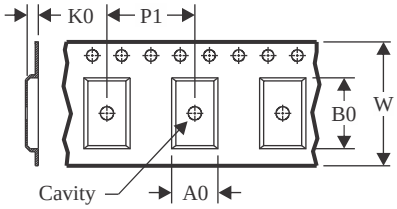
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

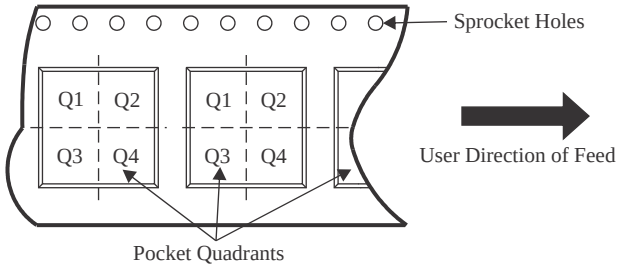


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

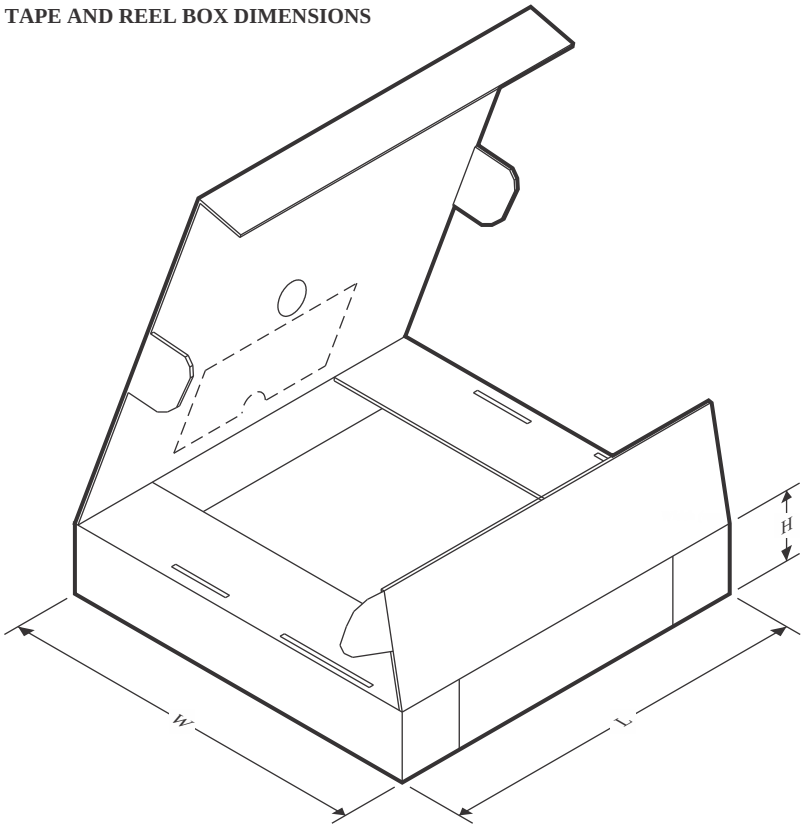
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS127L01IPBSR	TQFP	PBS	32	1000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2

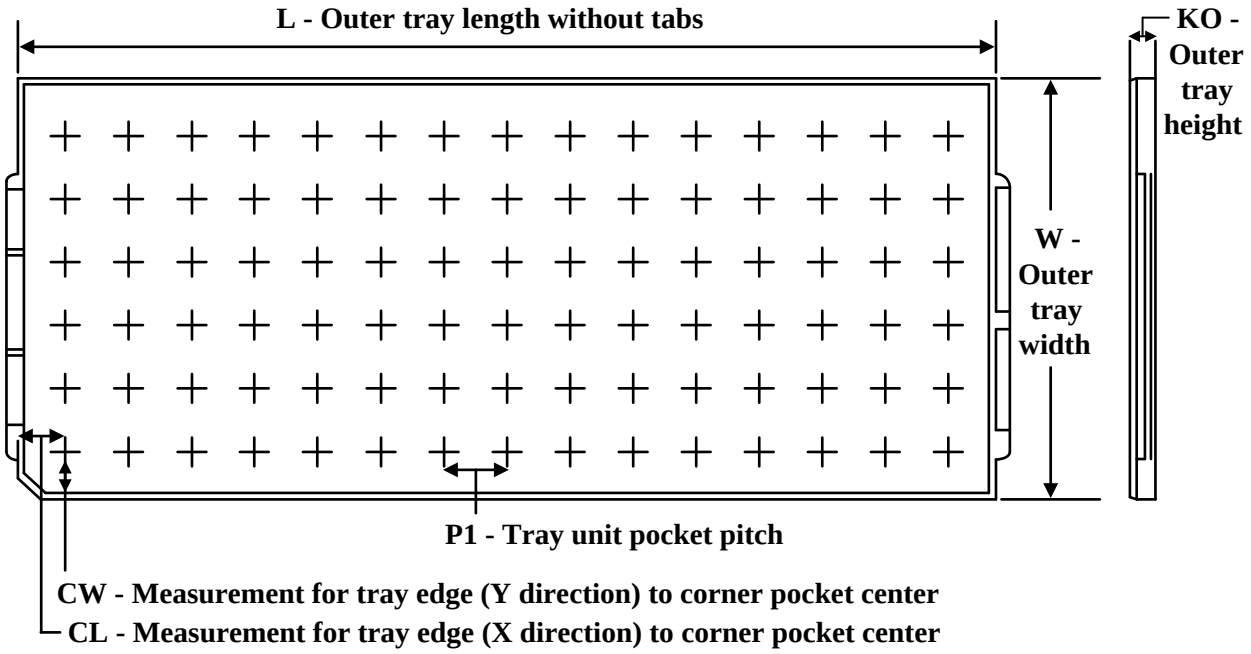
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS127L01IPBSR	TQFP	PBS	32	1000	350.0	350.0	43.0

TRAY

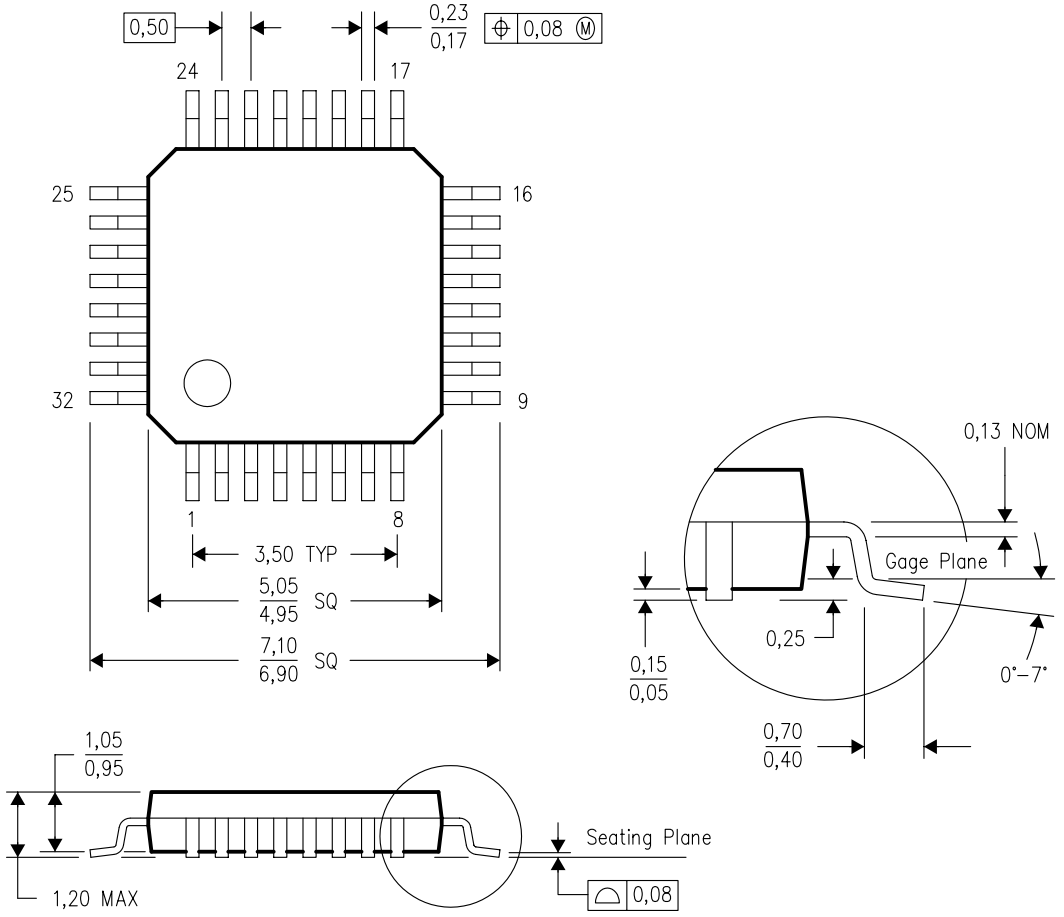


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS127L01IPBS	PBS	TQFP	32	250	10 X 25	150	315	135.9	7620	12.2	11.1	11.25

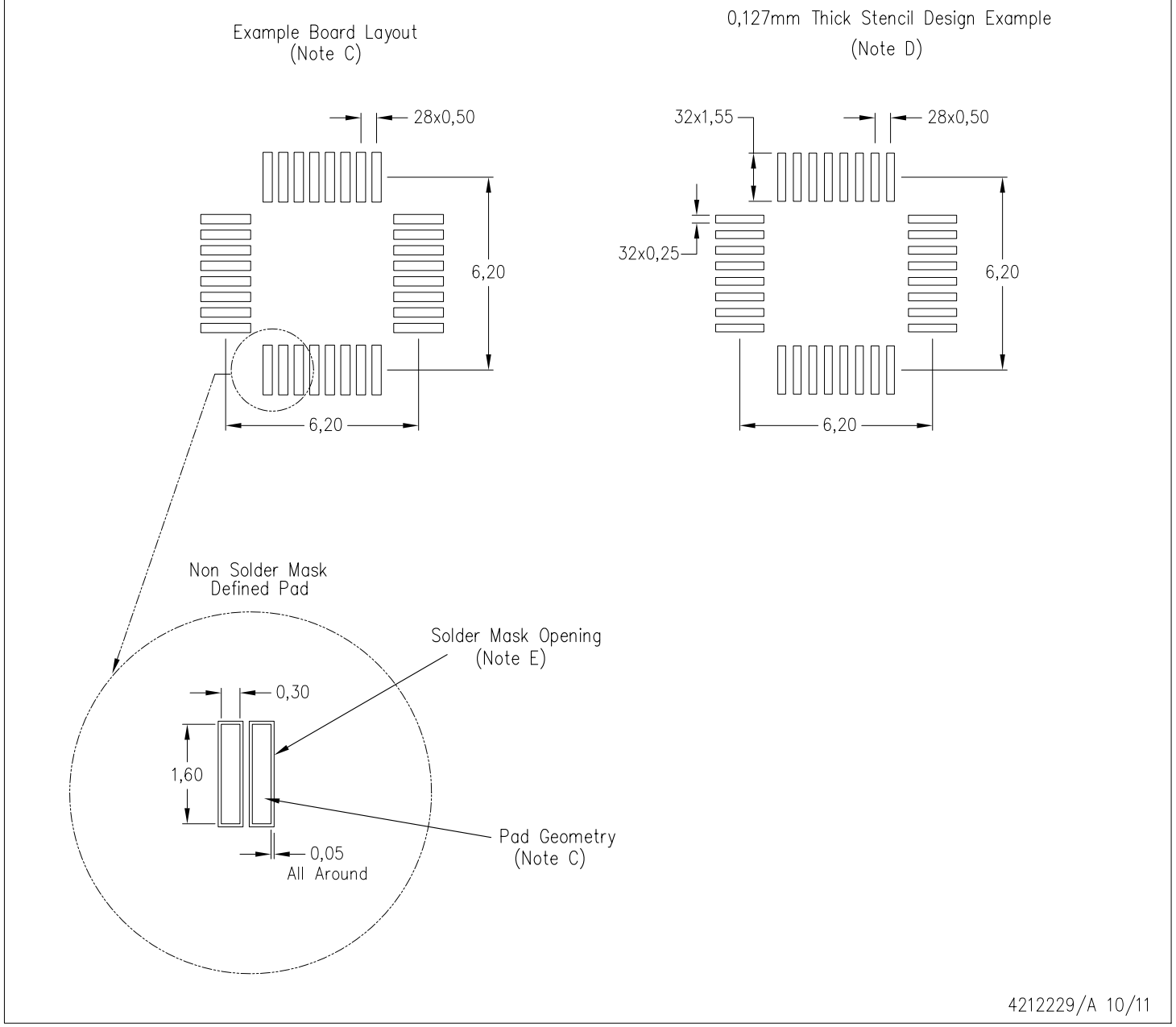
PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



4087735/B 07/05

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

PBS (S–PQFP–G32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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