



## F100131 Triple D Flip-Flop

### General Description

The F100131 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Master Reset (MR) input, a Common Clock ( $CP_C$ ), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock ( $CP_n$ ), Direct Set ( $SD_n$ ) and Direct Clear ( $CD_n$ ) inputs. Data enters a master when both  $CP_n$  and  $CP_C$  are LOW and transfers to a slave when  $CP_n$  or  $CP_C$  (or both) go HIGH. The Master Set,

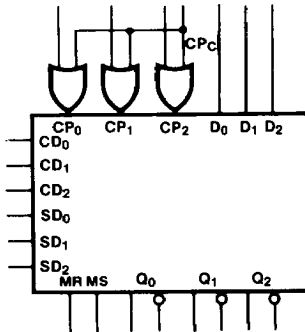
Master Reset and individual  $CD_n$  and  $SD_n$  inputs override the Clock inputs. All inputs have 50 k $\Omega$  pull-down resistors. Refer to the F100331 datasheet for:

Refer to the F100331 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

**Ordering Code:** See Section 8

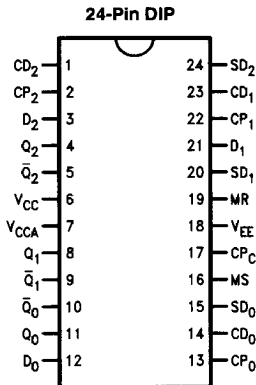
### Logic Symbol



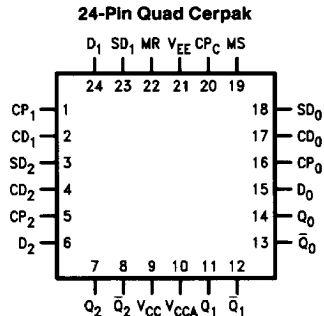
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Pin Names	Description
$CP_0$ - $CP_2$	Individual Clock Inputs
$CP_C$	Common Clock Input
$D_0$ - $D_2$	Data Inputs
$CD_0$ - $CD_2$	Individual Direct Clear Inputs
$SD_n$	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
$Q_0$ - $Q_2$	Data Outputs
$\bar{Q}_0$ - $\bar{Q}_2$	Complementary Data Outputs

### Connection Diagrams

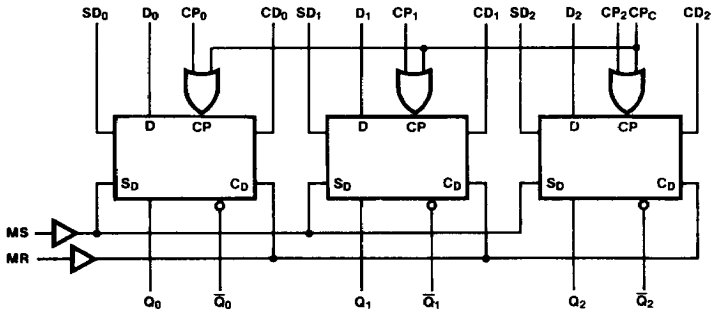


TL/F/9853-1



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# Logic Diagram



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## Truth Tables (Each Flip-Flop)

Synchronous Operation

Inputs					Outputs
$D_n$	$CP_n$	$CP_C$	$MS$ $SD_n$	$MR$ $CD_n$	$Q_n(t+1)$
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	L	L	L	L	$Q_n(t)$
X	H	X	L	L	$Q_n(t)$
X	X	H	L	L	$Q_n(t)$

Asynchronous Operation

Inputs					Outputs
$D_n$	$CP_n$	$CP_C$	$MS$ $SD_n$	$MR$ $CD_n$	$Q_n(t+1)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 U = Undefined  
 t = Time before CP Positive Transition  
 t+1 = Time after CP Positive Transition  
 ↗ = LOW to HIGH Transition

## Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature                    -65°C to +150°C  
Maximum Junction Temperature (T<sub>J</sub>)           +150°C

Case Temperature under Bias (T<sub>C</sub>)           0°C to +85°C  
V<sub>EE</sub> Pin Potential to Ground Pin           -7.0V to +0.5V  
Input Voltage (DC)                            V<sub>EE</sub> to +0.5V  
Output Current (DC Output HIGH)           -50 mA  
Operating Range (Note 2)                   -5.7V to -4.2V

## DC Electrical Characteristics

V<sub>EE</sub> = -4.5V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V <sub>OH</sub>	Output HIGH Voltage	-1025	-955	-880	mV	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V
V <sub>OL</sub>	Output LOW Voltage	-1810	-1705	-1620			
V <sub>OHC</sub>	Output HIGH Voltage	-1035			mV	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V
V <sub>OLC</sub>	Output LOW Voltage			-1610			
V <sub>IH</sub>	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.50			μA	V <sub>IN</sub> = V <sub>IL</sub> (Min)	

## DC Electrical Characteristics

V<sub>EE</sub> = -4.2V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V <sub>OH</sub>	Output HIGH Voltage	-1020		-870	mV	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V
V <sub>OL</sub>	Output LOW Voltage	-1810		-1605			
V <sub>OHC</sub>	Output HIGH Voltage	-1030			mV	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V
V <sub>OLC</sub>	Output LOW Voltage			-1595			
V <sub>IH</sub>	Input HIGH Voltage	-1150		-870	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1810		-1475	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.50			μA	V <sub>IN</sub> = V <sub>IL</sub> (Min)	

## DC Electrical Characteristics

V<sub>EE</sub> = -4.8V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V <sub>OH</sub>	Output HIGH Voltage	-1035		-880	mV	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V
V <sub>OL</sub>	Output LOW Voltage	-1830		-1620			
V <sub>OHC</sub>	Output HIGH Voltage	-1045			mV	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V
V <sub>OLC</sub>	Output LOW Voltage			-1610			
V <sub>IH</sub>	Input HIGH Voltage	-1165		-880	mV	Guaranteed HIGH Signal for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	-1830		-1490	mV	Guaranteed LOW Signal for All Inputs	
I <sub>IL</sub>	Input LOW Current	0.50			μA	V <sub>IN</sub> = V <sub>IL</sub> (Min)	

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Parametric values specified at -4.2V to -4.8V.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

**Note 4:** Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**DC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-4.8V$  unless otherwise specified,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ 

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$I_{IH}$	Input HIGH Current $CP_n, D_n$ $MS, MR, CP_C$ $CD_n, SD_n$			240 450 530	$\mu A$	$V_{IN} = V_{IH} (Max)$
$I_{EE}$	Power Supply Current	-149	-106	-74	mA	Inputs Open

**Ceramic Dual-In-Line Package AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
$f_{max}$	Toggle Frequency	325		325		325		MHz	Figures 2 and 3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $CP_C$ to Output	0.75	2.40	0.75	2.15	0.70	2.30	ns	Figures 1 and 3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $CP_n$ to Output	0.70	2.20	0.70	2.00	0.70	2.20	ns		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $CD_n, SD_n$ to Output	0.70	1.90	0.70	1.70	0.70	1.80	ns	$CP_n, CP_C = L$	Figures 1 and 4
$t_{PLH}$ $t_{PHL}$		0.70	2.10	0.70	2.00	0.70	2.20		$CP_n, CP_C = H$	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $MS, MR$ to Output	1.10	2.70	1.10	2.60	1.10	2.70	ns	$CP_n, CP_C = L$	
$t_{PLH}$ $t_{PHL}$		1.05	3.05	1.05	2.95	1.05	3.05		$CP_n, CP_C = H$	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	2.20	0.45	1.80	0.45	1.90	ns	Figures 1, 3 and 4	
$t_s$	Setup Time $D_n$ $CD_n, SD_n$ (Release Time) $MS, MR$ (Release Time)	0.90		0.70		0.90		ns	Figure 5	
		1.50		1.30		1.50			Figure 4	
		2.50		2.30		2.50				
$t_h$	Hold Time $D_n$	0.60		0.60		0.80		ns	Figure 5	
$t_{pw}(H)$	Pulse Width HIGH $CP_n, CP_C, CD_n,$ $SD_n, MR, MS$	2.00		2.00		2.00		ns	Figures 3 and 4	

**Cerpak AC Electrical Characteristics**  $V_{EE} = -4.2V$  to  $-4.8V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
$f_{max}$	Toggle Frequency	350		350		350		MHz	Figures 2 and 3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP <sub>C</sub> to Output	0.75	2.20	0.75	1.95	0.70	2.10	ns	Figures 1 and 3	
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP <sub>n</sub> to Output	0.70	2.00	0.70	1.80	0.70	2.00	ns		
$t_{PLH}$ $t_{PHL}$	Propagation Delay CD <sub>n</sub> , SD <sub>n</sub> to Output	0.70	1.70	0.70	1.50	0.70	1.60	ns	CP <sub>n</sub> , CP <sub>C</sub> = L	Figures 1 and 4
$t_{PLH}$ $t_{PHL}$		0.70	1.90	0.70	1.80	0.70	2.00		CP <sub>n</sub> , CP <sub>C</sub> = H	
$t_{PLH}$ $t_{PHL}$	Propagation Delay MS, MR to Output	1.10	2.50	1.10	2.40	1.10	2.50	ns	CP <sub>n</sub> , CP <sub>C</sub> = L	
$t_{PLH}$ $t_{PHL}$		1.05	2.85	1.05	2.75	1.05	2.85		CP <sub>n</sub> , CP <sub>C</sub> = H	
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	1.60	0.45	1.70	ns	Figures 1, 3 and 4	
$t_s$	Setup Time	0.80		0.60		0.80		ns	Figure 5	
	D <sub>n</sub>	1.40		1.20		1.40			Figure 4	
	CD <sub>n</sub> , SD <sub>n</sub> (Release Time) MS, MR (Release Time)	2.40		2.20		2.40				
$t_h$	Hold Time D <sub>n</sub>	0.50		0.50		0.70		ns	Figure 5	
$t_{pw(H)}$	Pulse Width HIGH CP <sub>n</sub> , CP <sub>C</sub> , CD <sub>n</sub> , SD <sub>n</sub> , MR, MS	2.00		2.00		2.00		ns	Figure 3 and 4	

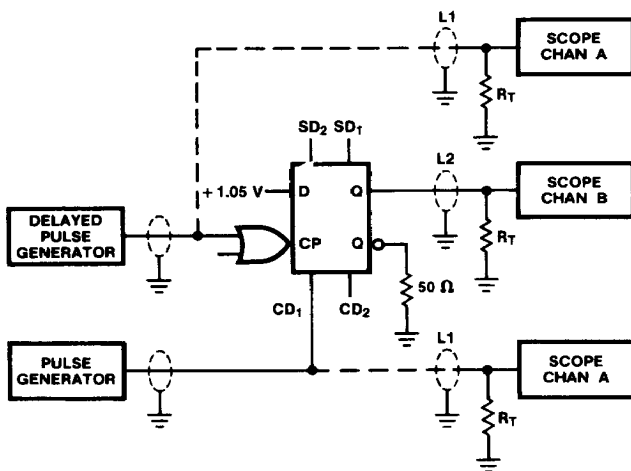


FIGURE 1. AC Test Circuit

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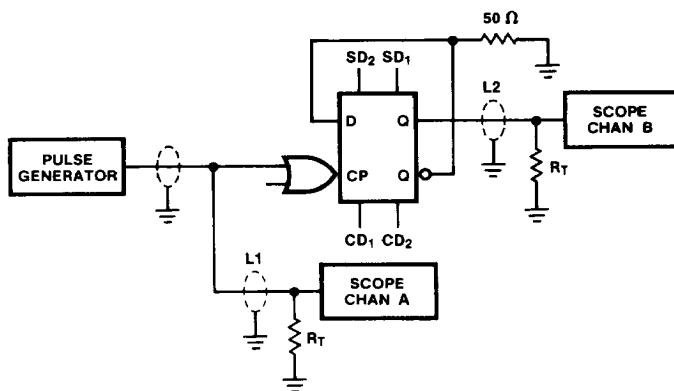


FIGURE 2. Toggle Frequency Test Circuit

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**Note:** $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$ L1 and L2 = equal length 50 $\Omega$  impedance lines $R_T = 50\Omega$  terminator internal to scopeDecoupling 0.1  $\mu F$  from GND to  $V_{CC}$  and  $V_{EE}$ All unused outputs are loaded with 50 $\Omega$  to GND $C_L$  = Fixture and stray capacitance  $\leq 3$  pF

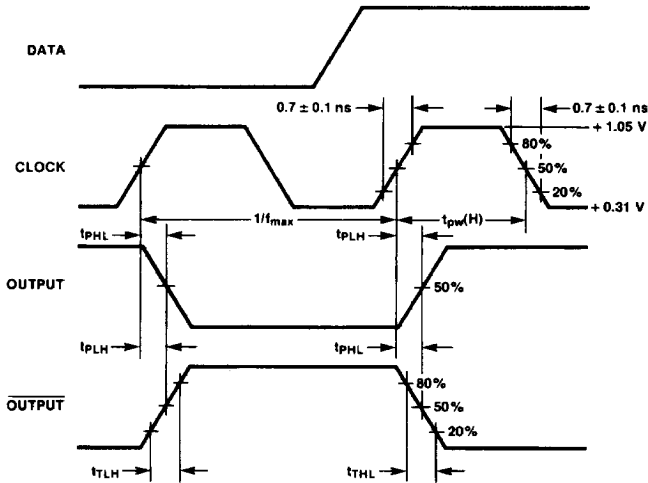


FIGURE 3. Propagation Delay (Clock) and Transition Times

TL/F/9853-8

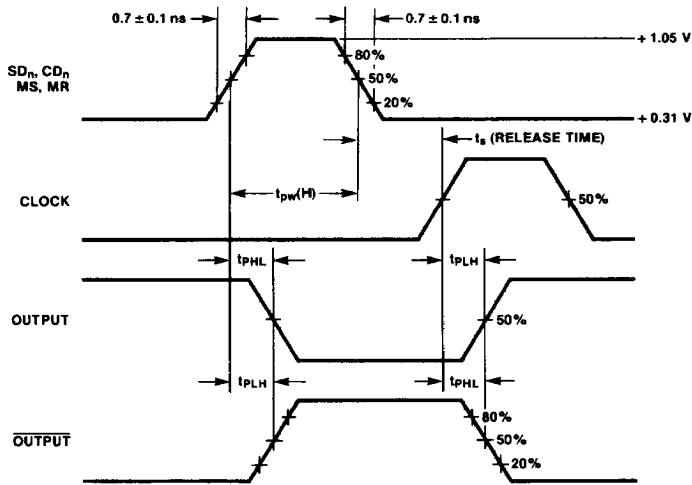
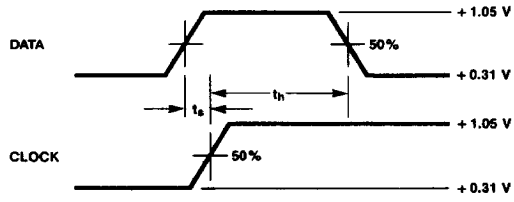


FIGURE 4. Propagation Delay (Resets)

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TL/F/9653-10

**FIGURE 5. Data Setup and Hold Time**

**Note:**

$t_s$  is the minimum time before the transition of the clock that information must be present at the data input.  
 $t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.