User manual for MA evaluation boards

MA2304DNS/MA2304PNS

About this document

Scope and purpose

This document describes the use and operation of the EVAL_AUDIO_MA2304xNS evaluation kit (EVK). The MA2304xNS EVK is an evaluation and demonstration kit for MA2304DNS and MA2304PNS proprietary multilevel amplifiers.

Intended audience

Audio amplifier design engineers.

Attention: ***Please read this user manual before operating the board. When powering up the board, make sure to follow the instructions in the "MA2304xNS start-up sequence" section.***

Stuck or in need of help?

Support for Infineon's class D audio portfolio can be found quickly and easily by visiting the **Class D Audio Amplifier IC Forum** or by visiting **community.infineon.com**. The community forum features members of the audio applications team that are ready to provide timely support, helping you get your designs done quickly, reliably, and right the first time.

Safety precautions

Note: *Please note the following warning regarding hazards associated with development systems.*

Table 1 **Safety precautions**

	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with ESD control procedures, refer to the applicable ESD protection handbooks and guidelines.*

Table of contents

1 Overview

The demonstration board EVAL_AUDIO_MA2304xNS is an evaluation and demonstration board for MERUS™ audio's MA2304DNS and MA2304PNS amplifiers.

It contains digital input/output (I/O) and a variety of output and setup/selection features. It also contains one onboard buck power supply generator (1.8 V/3.3 V selectable) so only one external power supply (PVDD) is necessary.

The board can be used for evaluating or demonstrating key features/advantages of the MERUS™ technology:

- Energy efficiency
  - Power losses at typical audio listening levels
  - Idle power loss
- Adaptive power management system
- No output filter components
  - Solution cost and size reduction
- Audio performance
  - THD performance and audio quality

1.1 Board features and audio performance

• Number of audio channels	2 (BTL) or 1 (PBTL)
• Audio input format	Digital (I^2S, LJF, RJF or TDM)
• Typical supply voltage	18 V (PVDD)
• Output noise level	52 μV_{RMS} (high audio performance mode)
• Dynamic range	106 dB (high audio performance mode)
• Idle consumption at PVDD = 18 V	61 mW (low power consumption mode)
• Efficiency	
– 1 W, 8 Ω	More than 79 percent
– Full-scale, 8 Ω	More than 90 percent

*Note: Idle consumption is the sum of output stage (PVDD) current, VDD, and VDD_IO supply current. As all the supplies are tied to PVDD, the efficiency of the buck-converter should be taken into account when measuring idle current consumption directly from PVDD. Features on the EVK make it possible to break the input and output of the buck converters for these purposes (see **Table 3**). Please refer to the MA2304xNS device datasheet for exact current figures.*

1.2 EVK device type

The type of device – MA2304DNS/MA2304PNS – is printed on the top of the EVK, and is also stated on the serial number label on the bottom side of the EVK PCB.

2 Setup guide

The following is included in the MA2304xNS evaluation kit:

1. An EVAL_AUDIO_MA2304xNS board
2. I²S interface boards: analog in, S/PDIF coax and S/PDIF optical
3. A micro USB cable
4. A 22 µH power inductor

Additional equipment required for operation and evaluation:

1. A 10 to 20 V DC power supply capable of driving 6 A (BTL) or 12 A (PBTL)
2. Loudspeaker and speaker wires, as shown in **Figure 1**

In addition, for datasheet spec testing, as shown in **Figure 1**:

1. A 2 to 8 Ω resistor load
2. An audio analyzer with a class-D measurement filter

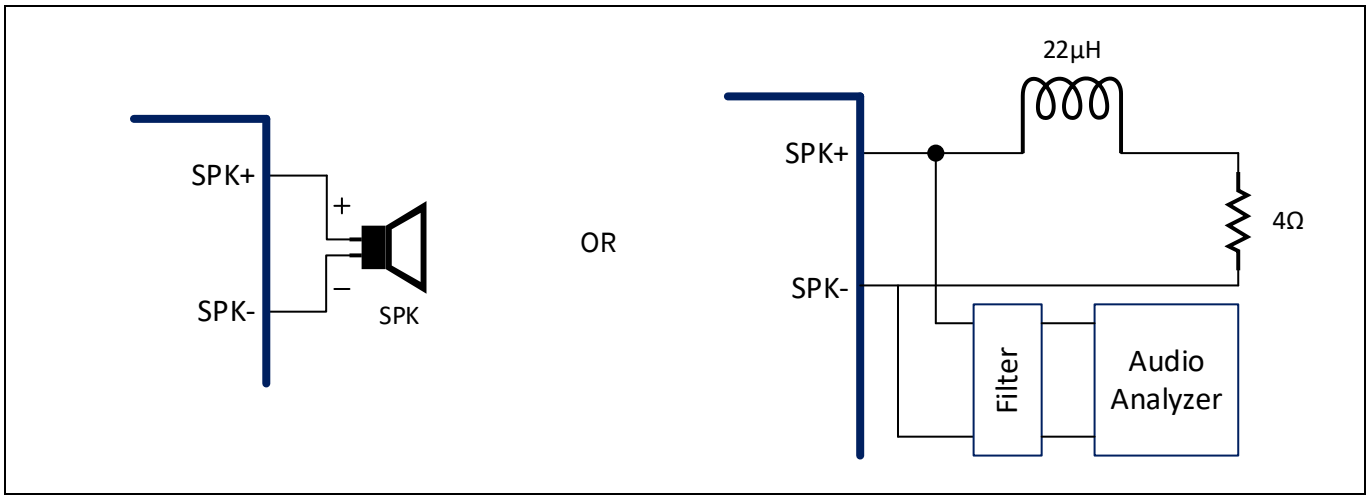

Figure 1 Setup for “speaker test” or “datasheet spec test”

2.1 EVK connections and interfaces

The MA2304xNS EVK includes the main EVAL_AUDIO_MA2304xNS board and three interface boards.

2.1.1 EVAL_AUDIO_MA2304xNS board

The board features MA2304xNS silicon, digital I/O headers, enable and mute switches, speaker terminals, power supply terminal blocks and a USB port.

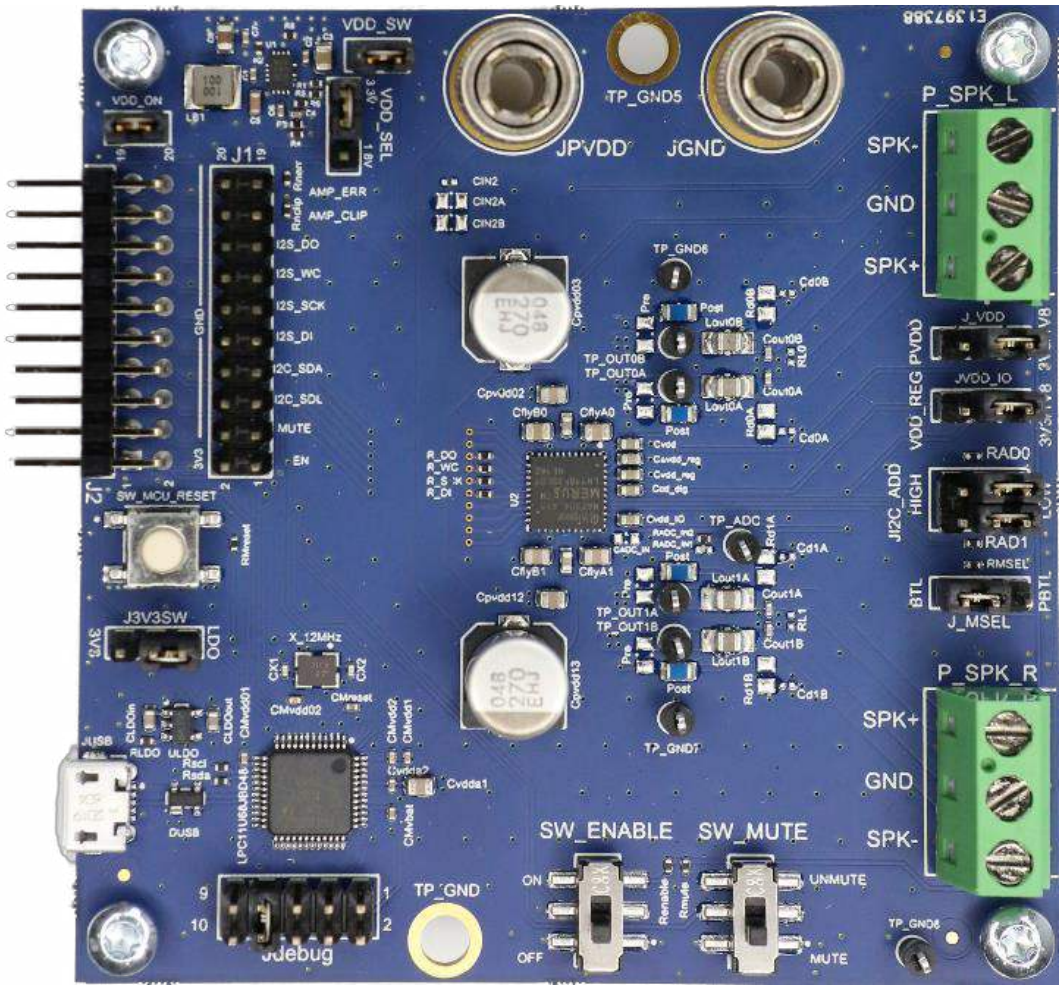

Figure 2 EVAL_AUDIO_MA2304xNS board (top view)

2.1.2 Interface boards

Three interface boards are included: analog in, S/PDIF coax and S/PDIF optical. These are plugged in to the J1 digital I/O breakout header for simple evaluation.

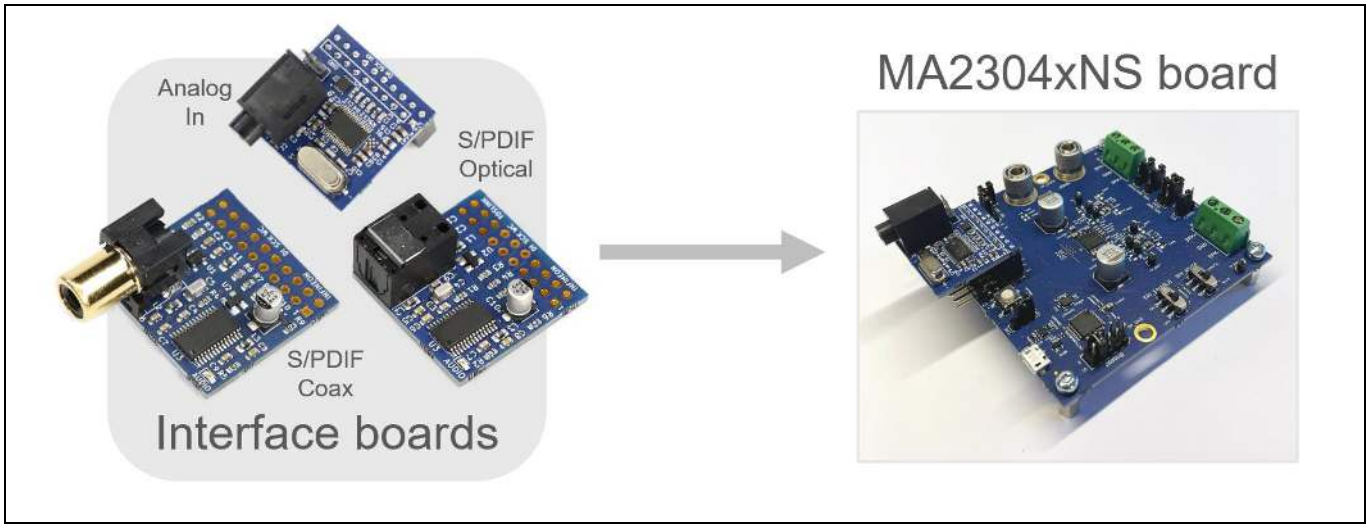

Figure 3 Interface boards

There is no need to configure the MA2304xNS when using these interface boards, as its digital audio output format matches the MA2304xNS defaults.

Note that the interface boards are not compatible with a 1.8 V supply. When using the onboard buck converter, ensure that the MA2304xNS board's VDD_SEL jumper is configured for 3.3 V (pins 1 and 2).

Interface board input/output specifications are provided in **Table 2**.

Table 2 Interface board I/O specifications

Interface board	Input	Output
Analog in[1]	3.5 mm (1/8 in.) stereo TRS jack 2.1 V_{RMS} full-scale	I^2S, 24-bit serial audio at 3.3 V SCK = 64 x WCK WCK = 48 kHz
S/PDIF coax	RCA jack 0.2 V minimum, 5 V tolerant 32 to 96 kHz support	I^2S, 24-bit serial audio at 3.3 V SCK = 64 x WCK WCK = 32 to 96 kHz
S/PDIF optical	Optical input jack 32 to 96 kHz support	I^2S, 24-bit serial audio at 3.3 V SCK = 64 x WCK WCK = 32 to 96 kHz

[1]Noise measurements and other specs will show degraded performance when using the analog in interface board.

2.1.3 EVK headers and connectors

The following table provides a description of each jumper, header, switch and test point. Defaults are shown in the “Comment” column.

Table 3 EVK headers and connectors

Name	Description	Comment
J_MSEL	Selects amplifier output mode between PBTL (L) and BTL(H)	Default: BTL(H)
JI2C_ADD AD1 AD0	These headers select the I²C slave address (see **Table 4**)	Default: I²C address 0b0100000 AD1 and AD0 both jumpered low (GND)
JVDD_IO	Sets VDD_IO source as: VDD_REG onboard supply (pins 1 and 2) VDD 1.8 V/3.3 V onboard supply (pins 2 and 3)	Default: VDD (pins 2 and 3)
J_VDD	Sets VDD source as: PVDD onboard supply (pins 1 and 2) VDD 1.8 V/3.3 V onboard supply (pins 2 and 3)	Default: VDD (pins 2 and 3)
J3V3SW	Sets VDD_MCU source as: VDD 1.8 V/3.3 V onboard supply (pins 1 and 2) VDD_LDO onboard supply (pins 2 and 3)	Default: LDO (pins 2 and 3)
VDD_SEL	Sets the onboard buck converter output as: 3.3 V (pins 1 and 2) 1.8 V (pins 2 and 3)	Default: 3.3 V (pins 1 and 2)
VDD_SW	Provides the option to measure PVDD current into the buck converter	Default: Jumpered
VDD_ON	Provides the option to measure the buck converter output current	Default: Jumpered
Jdebug	For normal operation, place a jumper on pins 7 and 8	Default: Pins 7 and 8 jumpered
J1	Digital I/O breakout header. Refer to **Section 2.2** for details.	I/O pins. Do not jumper.
J2	Interface board connector	I/O pins. Do not jumper.
SW_ENABLE	Controls the amplifier’s ENABLE pin. Sets the amplifier into enabled state when set to on.	Default: Off
SW_MUTE	Controls the amplifier’s NMUTE pin. Mutes the amplifier when set to mute.	Default: Mute
SW_MCU_RESET	Places the onboard MCU into reset state while pressed	
P_SPK_L	OUT0x speaker connection	Three-way screw terminal with positive and negative speaker outputs. Center terminal = GND.
P_SPK_R	OUT1x speaker connection	Three-way screw terminal with positive and negative speaker outputs. Center terminal = GND.
TP_OUT0A	Direct connection to device output node OUT0A	Output measurement pin

Name	Description	Comment
TP_OUT0B	Direct connection to device output node OUT0B	Output measurement pin
TP_OUT1A	Direct connection to device output node OUT1A	Output measurement pin
TP_OUT1B	Direct connection to device output node OUT1B	Output measurement pin
TP_ADC	AUX_ADC input test point	
TP_GND6 TP_GND7 TP_GND8	Ground test points	
TP_GND TP_GND2 TP_GND3 TP_GND4 TP_GND5	Ground-connected mounting holes	

Table 4 I²C address decoding (JI2C_ADD)

I²C device address	AD1	AD0	7-bit I²C address
0x20	L	L	0b0100000
0x21	L	H	0b0100001
0x22	H	L	0b0100010
0x23	H	H	0b0100011

2.2 Notes on the digital I/O breakout header

The digital I/O breakout header (J1) provides access to audio and control signals (I^2S and I^2C, respectively) as well as several MA2304xNS GPIO pins and the onboard VDD supply (3.3 or 1.8 V). The J1 header is meant for use with the interface boards, and/or external connections (external I^2S, MCU, etc.) for measurements and debugging. The J2 header contains exactly the same signals as J1 but can be used for monitoring the I/O digital signals.

The MA2304xNS acts as an I^2S slave, accepting SCK (bit clock) and WC (word clock) as inputs, with SCK = 64 x WC as default.

Table 5 Digital I/O breakout header

Pin	Signal	Signal	Pin
20	GND	/AMP_ERR	19
18	GND	/AMP_CLIP	17
16	GND	I2S_DO	15
14	GND	I2S_WC	13
12	GND	I2S_SCK	11
10	GND	I2S_DI	9
8	GND	I2C_SDA	7
6	GND	I2C_SCL	5
4	GND	/MUTE	3
2	3V3	EN	1

3 Operating the demonstration board

3.1 Recommended operating conditions

Table 6 Recommended operating conditions

Parameter	Minimum	Nominal	Maximum	Unit
PVDD	10	18	20	V
Output peak current (BTL) Output peak current (PBTL)			6.0 12.0	A A

3.2 Toggle switches

The board has two MA2304xNS-related toggle switches, as shown in **Table 7**. The toggle switches have the following functions:

Table 7 Switch function

Switch	Function
SW_ENABLE	Off/on (default set to “off”)
SW_MUTE	Mute/unmute (default set to “mute”)

3.3 Firmware flash for the USB MCU

The evaluation board’s MCU firmware can easily be updated through USB. The latest firmware bin file can be obtained by downloading and installing the latest MERUS™ audio amplifier configurator GUI for the MA2304xNS. The firmware bin file is located in the “[Installation folder]\firmware” folder.

Follow the subsequent steps to flash the MCU:

1. Configure the evaluation board jumpers and switches as described in **Table 3**.
2. Set the Jdebug jumper to the third column from left to right (connecting pin 5 and 6):

Figure 4 Configuring the Jdebug header for firmware flash

3. Connect a USB cable to the evaluation board:

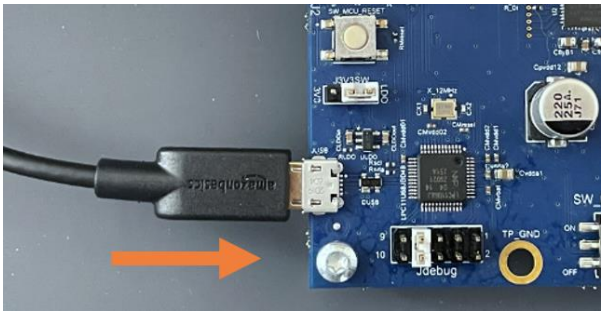

Figure 5 Connecting a USB cable to the evaluation board

4. Open Windows explorer and then the drive called “CRP DISABLD”. Delete the file “firmware.bin”:

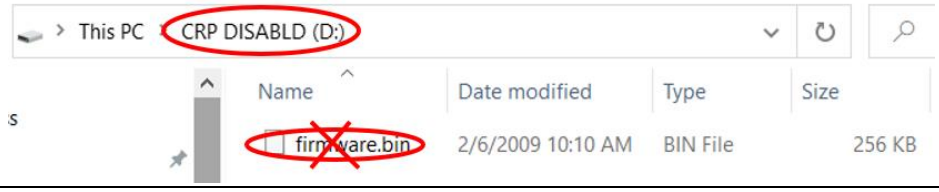

Figure 6 Deleting the contents of the “CRP DISABLD” drive

5. Open another explorer window and browse to the software installation folder, typically “C:\Users\[User]\Infineon\Tools\MERUS-Audio-Amplifier-Configurator”. Copy the .bin file from the firmware folder to the “CRP DISABLD” drive. In this example the .bin file is called “firmware.bin”, but it could have other filenames.

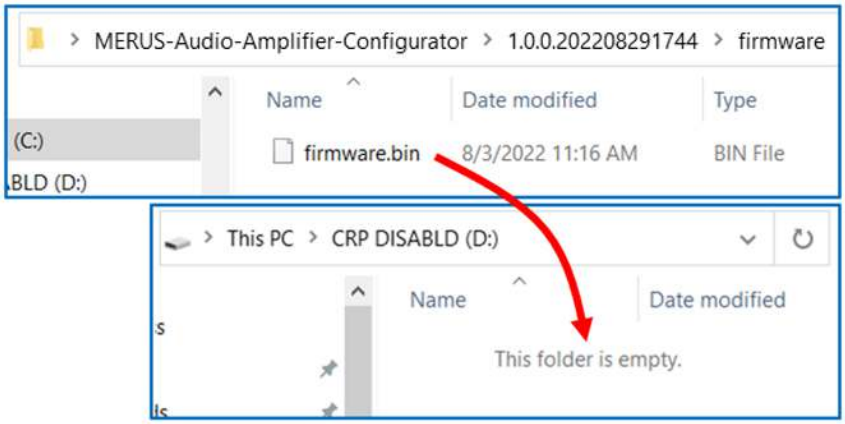

Figure 7 Copying “firmware.bin” to the “CRP DISABLD” drive

6. Move the Jdebug header back to the second column from left to right (connecting pin 7 and 8):

Figure 8 Configuring the Jdebug header for normal operation

7. Close Windows explorer and disconnect the USB cable.

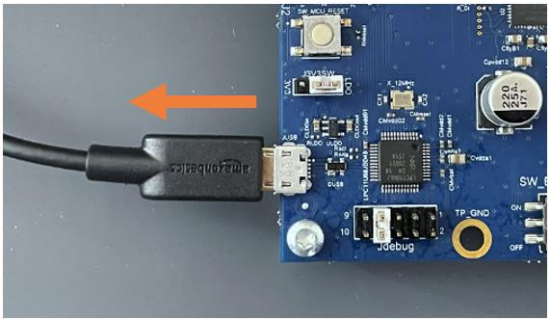

Figure 9 Disconnecting the USB cable from the evaluation board

8. The MCU firmware update is now complete.

3.4 Speaker load

The demonstration board is configured as a filterless amplifier. This means that no LC filter is placed between the amplifier outputs and the load. In normal use the amplifier relies on the inherent inductance of the loudspeaker, so no extra inductance is needed.

Inductors for use in series with power resistors are included with the demonstration board. These can be used when making any measurements without a real loudspeaker as the load, and having no external low-pass filter (LPF) in front of the audio analyzer input section.

Please note that many audio measurement analyzers do not perform correctly when connected directly to a filterless amplifier output. Please refer to **Section 4** for more information on measurement methods.

3.5 MERUS™ audio amplifier configurator

The demonstration board is used with PC graphical user interface (GUI) software to control the MA2304xNS device.

The MA2304xNS can play audio by default without configuration, but to take advantage of the many features the chip offers it is necessary to configure the device.

Refer to the MERUS™ audio amplifier configurator user manual for details on how to install and use this software.

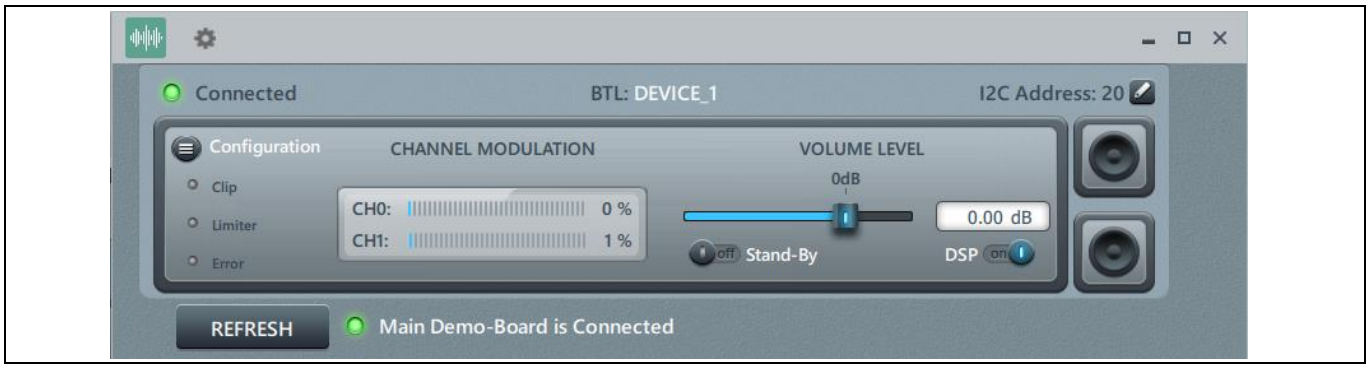

Figure 10 MA2304DNS GUI main window

3.6 MA2304xNS start-up sequence

Follow this (recommended) sequence to start the board:

1. *Make sure toggle buttons are in “off” and “mute” positions.*
2. *Connect all cables (speakers/load, USB and power) to the EVK.*
3. *Connect an external I²S digital audio source to the EVK digital I/O header (J1). The EVK default I/O voltage is 3.3 V.*
4. *Turn on the PVDD power supply.*
5. *Make sure the I²S clocks are present before enabling the amplifier.*
6. *Start board by setting the SW_ENABLE toggle switch to the “on” position.*
7. *Start playing sound by setting the SW_MUTE toggle switch to the “unmute” position.*

Mute and turn off the PVDD power supply when finished.

4 Measurement methods

Setting up a reliable measurement configuration for the MA2304DNS or the MA2304PNS takes a little more effort than for linear amplifiers, and even “regular” switching amplifiers. This is mainly because the MA2304xNS is a filterless amplifier, which means it does not require an external (usually expensive and bulky) LC filter to remove switching residuals. The filterless application is enabled by the MERUS™ audio multilevel technique, which ensures the switching residual is orders lower compared to “regular” switching amplifiers. For more information on the multilevel switching technique, please refer to the datasheet.

To obtain reliable measurement results, the MA2304xNS devices require a separate external LPF in front of the input stage of the audio analyzer. Most audio analyzers are bandwidth-limited at their input stage, which means they cannot follow the rapid changes of the amplifier’s output stage. This can result in inaccurate and high THD+N measurements.

Figure 11 shows the recommended measurement setup. The setup shows a LPF stage (AUX-0025) in front of the audio analyzer (APx525 with the serial interface I/O option installed). In this case the measurement setup has been built around Audio Precision hardware, but this can also be some other audio analyzer hardware. Please note that it is recommended to use a balanced input measurement configuration.

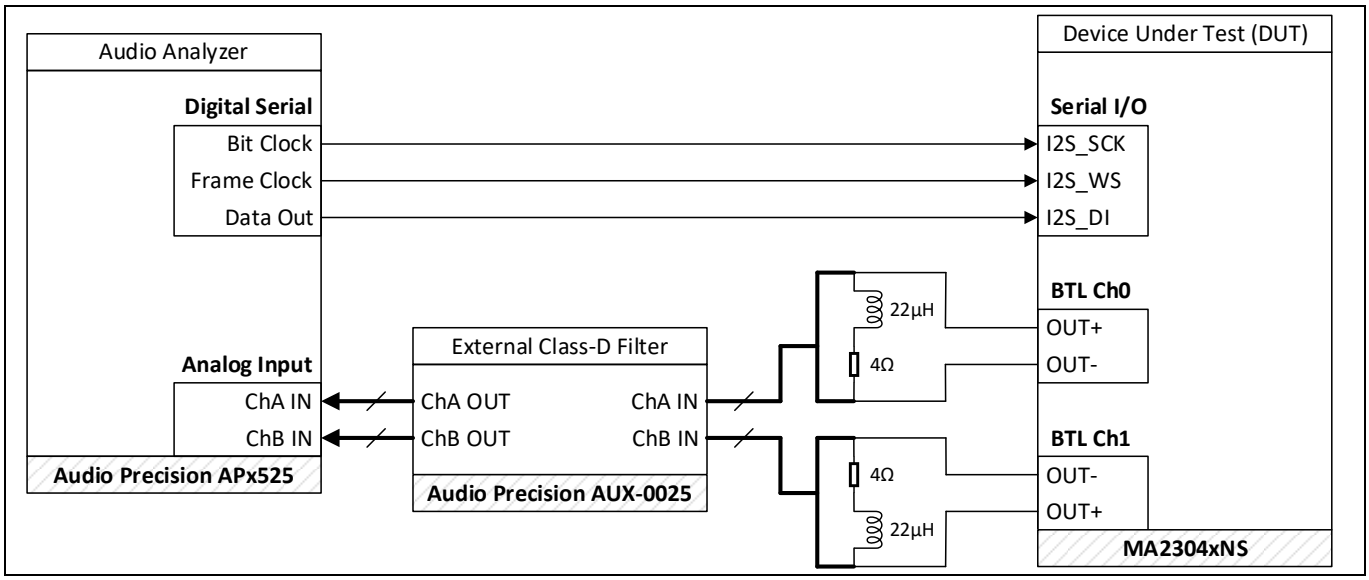

Figure 11 Recommended audio measurement setup

Figure 12 shows an example measurement setup using an 8 Ω/22 µH load, similar to the setup shown in **Figure 11**.

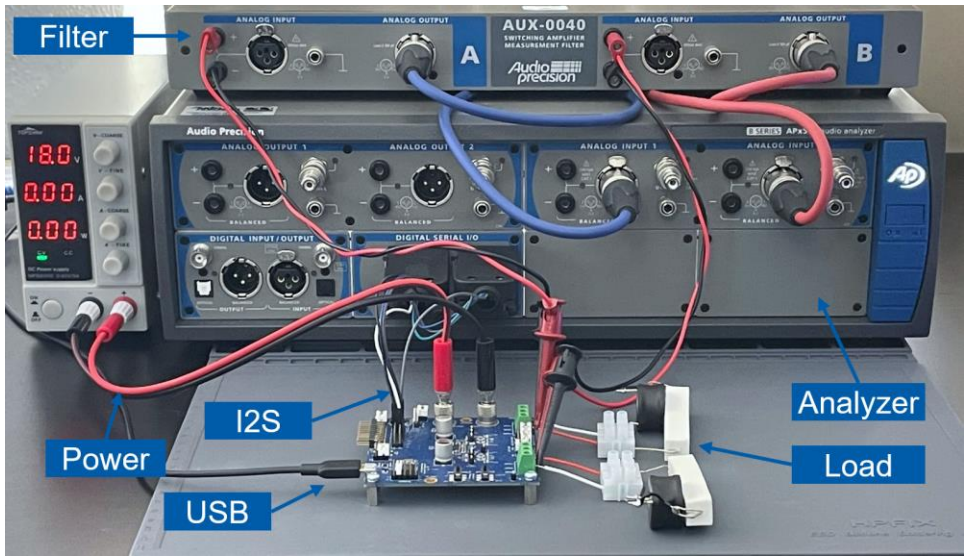

Figure 12 Audio measurement setup example

Figure 13 shows an example dynamic range measurement performed with the previous measurement setup.

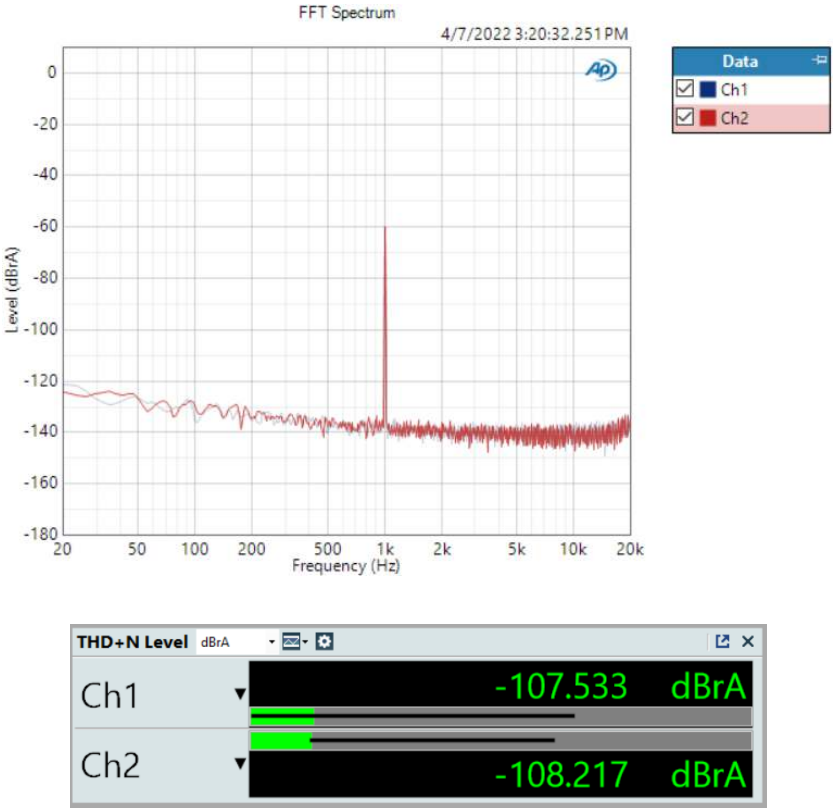

Figure 13 Dynamic range measurement example

5 Schematic

5.1 Amplifier page

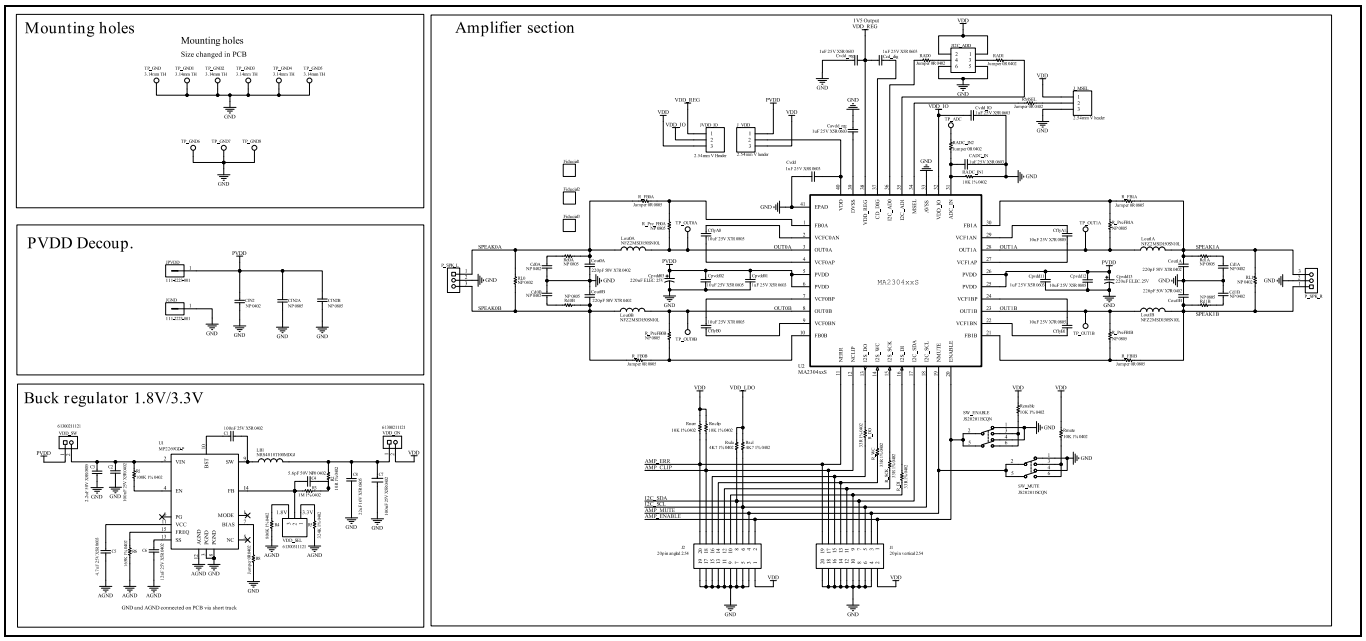

Figure 14 Amplifier page

5.2 MCU page

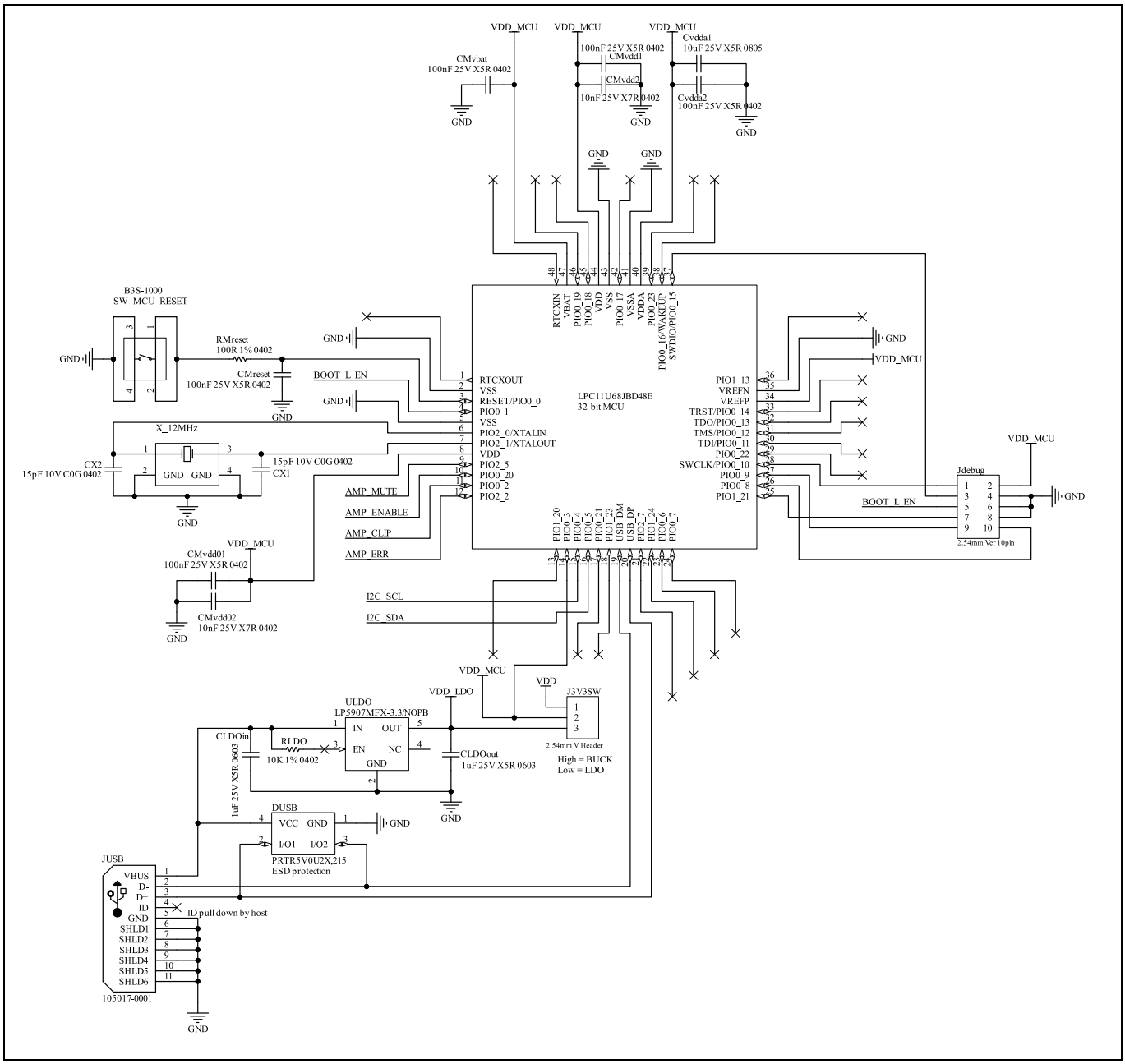

Figure 15 MCU page

6 PCB layout

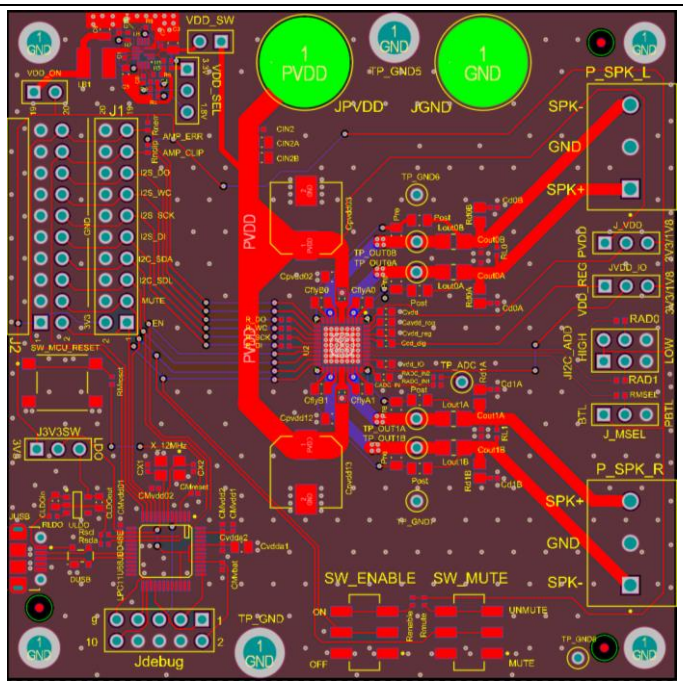

Figure 16 PCB layout (top composite x-ray view)

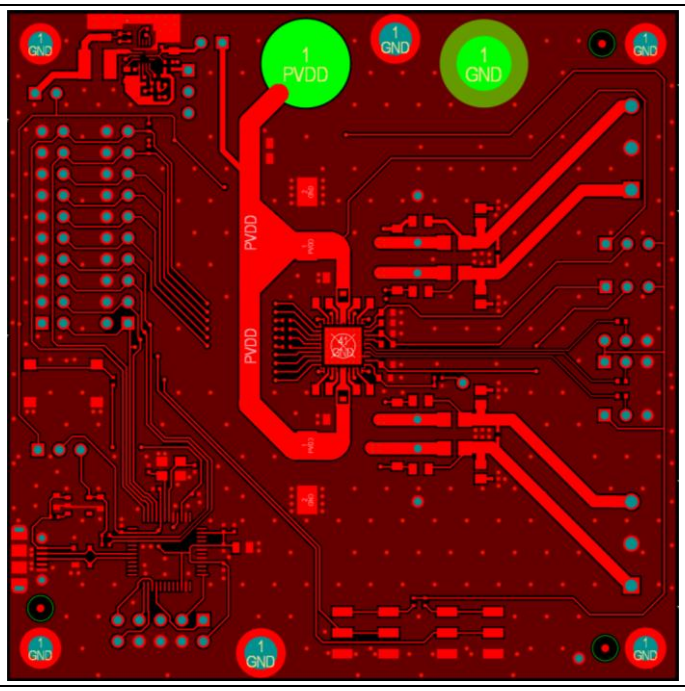

Figure 17 PCB layout (top layer)

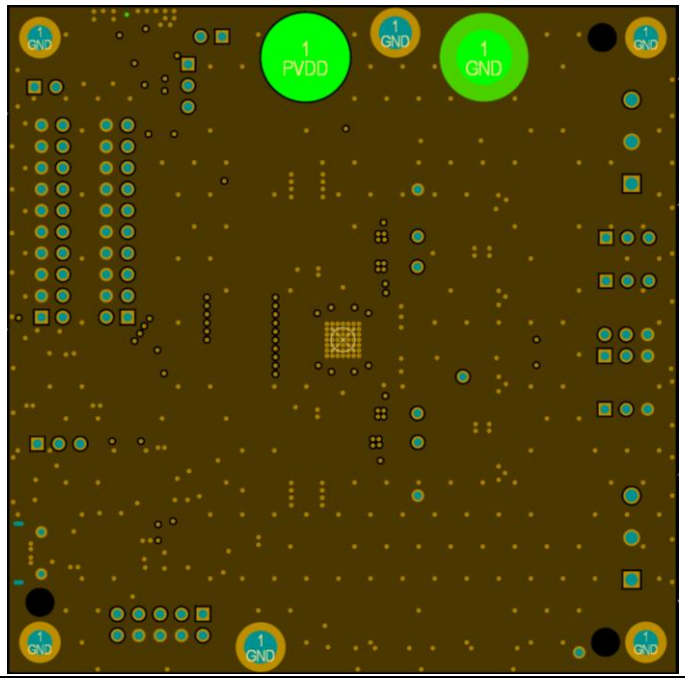

Figure 18 PCB layout (layer 1)

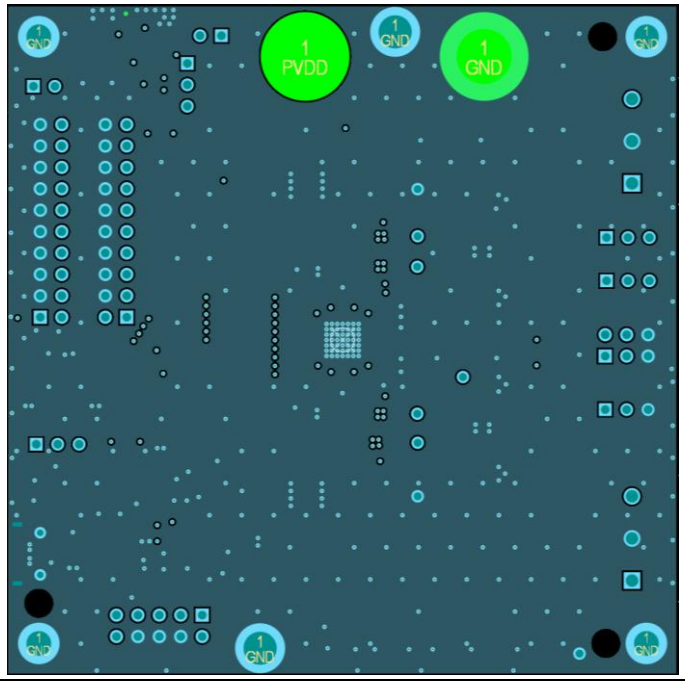

Figure 19 PCB layout (layer 2)

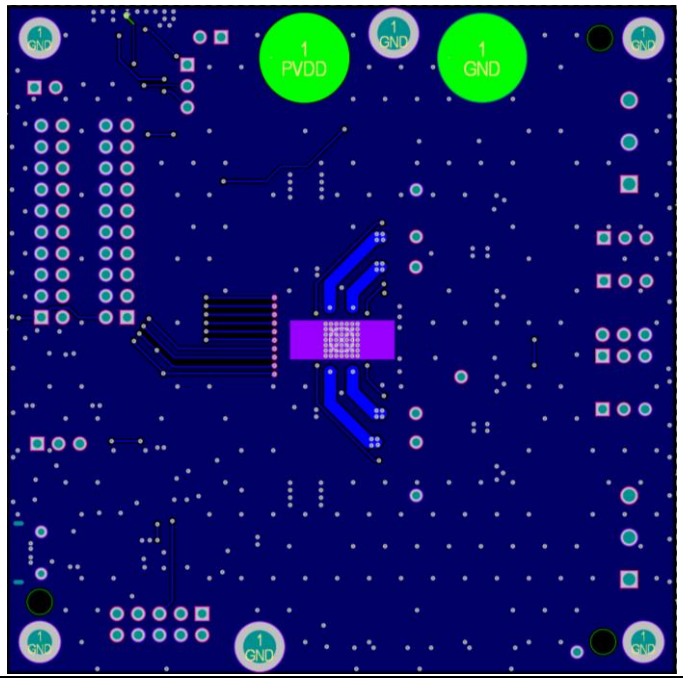

Figure 20 PCB layout (bottom layer)

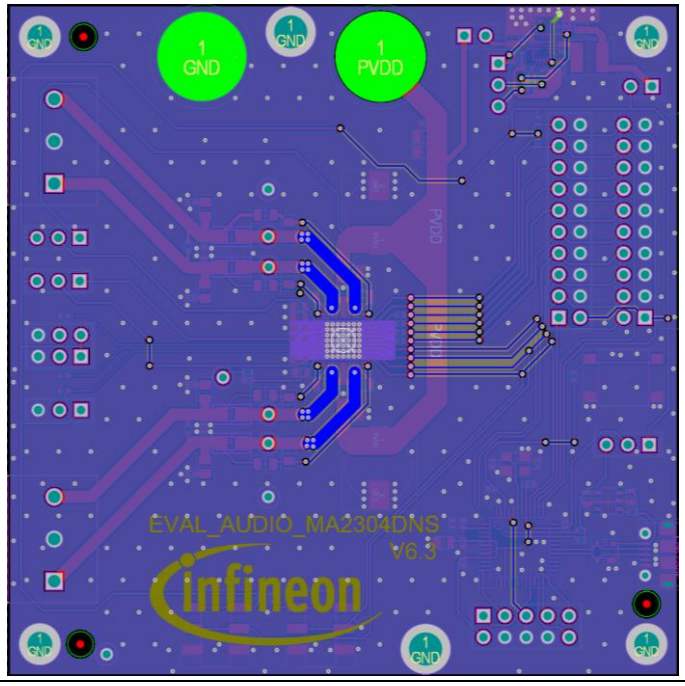

Figure 21 PCB layout (mirrored bottom composite x-ray view)

7 Bill of materials

Table 8 Bill of materials

S. no.	Reference	Qty.	Description	Manufacturer	Part number
1	C1, C2, C7, CMreset, CMvbat, CMvdd1, CMvdd01, Cvdda2	8	100 nF 25V X5R 0402	Samsung Electro-Mechanics	CL05A104KA5NNND
2	C3	1	2.2 uF 50V X5R 0805	Samsung Electro-Mechanics	CL21A225KBQNNNE
3	C4	1	5.6 pF 50V NP0 0402	Samsung Electro-Mechanics	CL05C5R6DB5NNNC
4	C5	1	4.7 uF 25V X5R 0603	Samsung Electro-Mechanics	CL10A475KA8NQNC
5	C6	1	12 nF 25V X5R 0402	Murata Electronics	GCM155R71E123KA55J
6	C8	1	22 uF 10V X5R 0805	Samsung Electro-Mechanics	CL21A226MPCLRNC
7	Cavdd_reg, Ccd_dig, CLDOin, CLDOout, Cpvdd01, Cpvdd11, Cvdd, Cvdd_IO, Cvdd_reg	9	1 uF 25V X5R 0603	Samsung Electro-Mechanics	CL10A105KA8NFNC
8	Cd0A, Cd0B, Cd1A, Cd1B, CIN2	5	NP 0402		
9	CflyA0, CflyA1, CflyB0, CflyB1	4	10 uF 25V X7R 0805	Samsung Electro-Mechanics	CL21B106KAYQNNE
10	CIN2A, CIN2B	2	NP 0805		
11	CMvdd2, CMvdd02	2	10 nF 25V X7R 0402	Samsung Electro-Mechanics	CL05B103KA5NFNC
12	Cout0A, Cout0B, Cout1A, Cout1B	4	220 pF 50V X7R 0402	KEMET	C0402C221K5RACTU
13	Cpvdd02, Cpvdd12, Cvdda1	3	10 uF 25V X5R 0805	Samsung Electro-Mechanics	CL21A106KAYNNNG
14	Cpvdd03, Cpvdd13	2	220 uF ELEC. 25V	Rubycon	25TZV220M8X10.5
15	CX1, CX2	2	15 pF 10V C0G 0402	Vishay/Vitramon	VJ0402A150KXQCW1BC
16	DUSB	1	PRTR5V0U2X,215	NXP Semiconductors	PRTR5V0U2X,215
17	Fiducial1, Fiducial2, Fiducial3	3			
18	J1	1	20-pin vertical 2.54	Würth Elektronik	61302021121
19	J2	1	20-pin angled 2.54	Würth Elektronik	61302021021
20	J3V3SW, J_MSEL, J_VDD, JVDD_IO	4	2.54 mm V Header	Würth Elektronik	61300311121
21	Jdebug	1	2.54 mm Ver 10 pin	Würth Elektronik	61301021121

S. no.	Reference	Qty.	Description	Manufacturer	Part number
22	JGND, JPVDD	2	111-2223-001	CINCH	111-2223-001
23	JI2C_ADD	1	2.54 mm V header	Würth Elektronik	61300621121
24	JUSB	1	105017-0001	Molex	105017-0001
25	LB1	1	IND. 10 uH	Taiyo	NRS4018T100MDGJ
26	Lout0A, Lout0B, Lout1A, Lout1B	4	NFZ2MSD150SN10L	Murata	NFZ2MSD150SN10L
27	LPC11U68JBD48E	1	32-bit MCU	NXP	LPC11U68JBD48E
28	P_SPK_L, P_SPK_R	2	SCREW-5.0/5.08 3WAYS	TE Connectivity	282837-3
29	R1	1	100K 1% 0402	Yageo	RC0402FR-07100KL
30	R2	1	10R 1% 0402	Vishay/Dale	CRCW040210R0FKEE
31	R3	1	1M 1% 0402	Vishay/Dale	CRCW04021M00FKEDC
32	R4	1	806K 1% 0402	Yageo	AC0402FR-07806KL
33	R5	1	324K 1% 0402	Yageo	AC0402FR-07324KL
34	R6	1	165K 1% 0402	Yageo	RC0402FR-07165KL
35	R8, RAD0, RAD1, RADC_IN2, RMSEL	5	Jumper 0R 0402	Vishay/Dale	CRCW04020000Z0EDC
36	R_DI, R_DO, R_SCK, R_WC	4	33R 1% 0402	Vishay/Dale	CRCW040233R0FKEDC
37	R_FB0A, R_FB0B, R_FB1A, R_FB1B	4	Jumper 0R 0805	Vishay/Dale	RCC08050000Z0EA
38	R_Pre_FB0A, R_PreFB0B, R_PreFB1A, R_PreFB1B	4	NP 0805		
39	Renable, RLDO, Rmute, Rnclip, Rnerr	5	10K 1% 0402	Vishay/Dale	CRCW040210K0FKEDC
40	RL0, RL1	2	NP 0402		
41	RMreset	1	100R 1% 0402	Vishay/Dale	CRCW0402100RFKEDC
42	Rscl, Rsda	2	4K7 1% 0402	Panasonic	ERJ-U2RD4701X
43	SW_ENABLE, SW_MUTE	2	JS202011SCQN	C&K Components	JS202011SCQN
44	SW_MCU_RESET	1	B3S-1000	Omron Electronics	B3S-1000
45	TP_ADC, TP_GND6, TP_GND7, TP_GND8, TP_OUT0A, TP_OUT0B, TP_OUT1A, TP_OUT1B	8	5001	Keystone	5001
46	U1	1	MP2269GD-P	Monolithic Power Systems	MP2269GD-P
47	U2	1	MA2304DNS		MA2304DNS

Bill of materials

S. no.	Reference	Qty.	Description	Manufacturer	Part number
48	ULDO	1	LP5907MFX-3.3/NOPB	Texas Instruments	LP5907MFX-3.3/NOPB
49	VDD_ON, VDD_SW	2	61300211121	Würth Elektronik	61300211121
50	VDD_SEL	1	61300311121	Würth Elektronik	61300311121
51	X_12MHz	1	ABM8G-12.000MHZ-18-D2Y-T	ABRACON	ABM8G-12.000MHZ-18-D2Y-T

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-08-26	Initial release
V 1.1	2022-09-12	Replaced "MERUS™ amplifier tool" with "MERUS™ audio amplifier configurator" throughout the document.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-09-12

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

UM_2204_PL88_2206_163320

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.