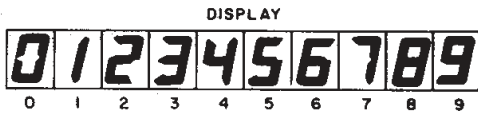


CMOS Decade Up-Down Counter/Latch/Display Driver

High-Voltage Type (20-V Rating)



92CS-31380

Features:

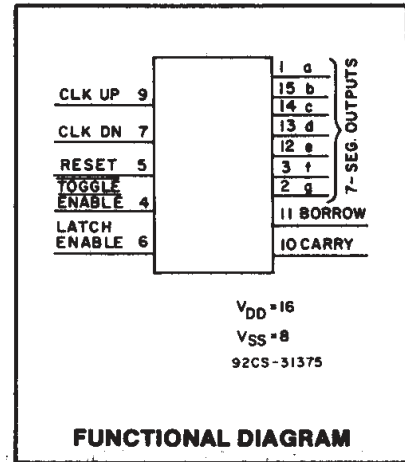
- Separate clock-up and clock-down lines-
- Capable of driving common cathode LEDs and other displays directly
- Allows cascading without any external circuitry
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25° C

■ CD40110B is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked, via positive going inputs, up or down regardless of the state or timing (within 100 ns typ.) of the other clock line.

The clock signal is fed into the control logic and Johnson counter after it is preconditioned. The outputs of the Johnson counter (which include anti-lock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25 mA to drive LEDs and other displays such as low-voltage fluorescent and incandescent lamps.

A short duration negative-going pulse appears on the BORROW output when the count changes from 0 to 9 or the CARRY output when the count changes from 9 to 0. At the other times the BORROW and CARRY outputs are a logic 1.

The CARRY and BORROW outputs can be tied directly to the clock-up and clock-down lines respectively of another CD40110B for easy cascading of several counters.



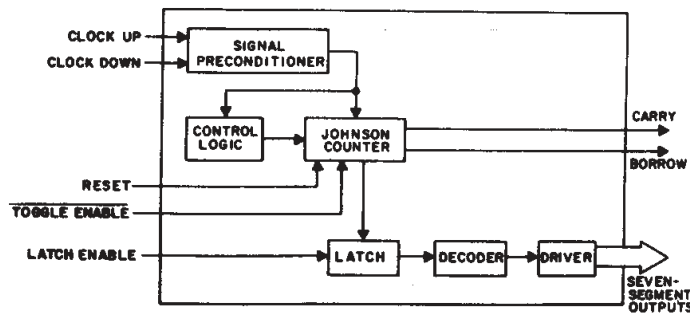
FUNCTIONAL DIAGRAM

- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- 5 V, 10 V and 15 V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices".

Applications:

- Rate comparators
- General counting applications where display is desired
- Up-down counting applications where input pulses are random in nature

The CD40110B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), and 16-lead dual-in-line plastic package (E suffix), and also available in chip form, (H suffix).



92CS-29200R1

Fig. 1 - Functional diagram.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40110B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V _{DD})	-0.5V to +20V
Voltages referenced to V _{SS} Terminal	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V _{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55°C to +100°C	500mW
For T _A = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T _A)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V _{DD} V	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package Temperature Range)	—	3	18	V
Clock Input Frequency (Sum of CL _{UP} & CL _{DN} Freqs.)	5	—	1	MHz
	10	—	3	
	15	—	5	
Clock Pulse Width	5	110	—	ns
	10	40	—	
	15	30	—	
Latch Enable Pulse Width	5	110	—	
	10	30	—	
	15	24	—	
Reset Removal-Time	5	550	—	
	10	200	—	
	15	130	—	
Reset Pulse Width	5	350	—	
	10	170	—	
	15	120	—	

CD40110B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				LIMITS AT INDICATED TEMPERATURES (°C)							Units
	I _{OH} (mA)	V _{OH} (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
									Min.	Typ.	Max.	
Quiescent Device Current Max. I _{DD}	—	—	—	5	5	5	150	150	—	0.04	5	μA
	—	—	—	10	10	10	300	300	—	0.04	10	
	—	—	—	15	20	20	600	600	—	0.04	20	
	—	—	—	20	100	100	3000	3000	—	0.08	100	
Output Voltage Low-Level Max. V _{OL}	—	—	0,5	5	0,05				—	0	0,05	V
	—	—	0,10	10	0,05				—	0	0,05	
	—	—	0,15	15	0,05				—	0	0,05	
High-Level Min. V _{OH}	—	—	0,5	5	—	—	—	—	—	4,55	—	V
	—	—	0,10	10	—	—	—	—	—	9,55	—	
	—	—	0,15	15	—	—	—	—	—	14,55	—	
Input Low Voltage Max. V _{IL}	—	0,5, 3,8	—	5	1,5				—	—	1,5	V
	—	1, 8,8	—	10	3				—	—	3	
	—	1,5, 13,8	—	15	4				—	—	4	
Input High Voltage Min. V _{IH}	—	0,5, 3,8	—	5	3,8				3,5	—	—	V
	—	1, 8,8	—	10	7				7	—	—	
	—	1,5, 13,8	—	15	11				11	—	—	
7-Segment Outputs Output Drive Voltage, High Min. V _{OH}	■	—	—	5	3,9		4		3,9	4,5	—	V
	-5	—	—		3,65		3,7		3,7	4,3	—	
	-10	—	—		3,55		3,65		3,65	4,25	—	
	-15	—	—		3,5		3,5		3,6	4,15	—	
	-20	—	—		3,45		3,35		3,45	4	—	
	■	—	—	10	8,75		8,85		8,75	9,5	—	
	-5	—	—		8,45		8,55		8,55	9,3	—	
	-10	—	—		8,42		8,5		8,5	9,25	—	
	-15	—	—		8,4		8,47		8,47	9,2	—	
	-20	—	—		8,4		8,40		8,45	9,1	—	
	■	—	—	15	13,8		13,9		13,8	14,5	—	
	-5	—	—		13,65		13,75		13,75	14,35	—	
	-10	—	—		13,6		13,72		13,72	14,3	—	
	-15	—	—		13,6		13,7		13,7	14,2	—	
	-20	—	—		13,6		13,6		13,65	14,1	—	
■	—	—	15	13,3		13,25		13,3	14,0	—		
-5	—	—		13,65		13,75		13,75	14,35	—		
-10	—	—		13,6		13,72		13,72	14,3	—		
-15	—	—		13,6		13,7		13,7	14,2	—		
-20	—	—		13,6		13,6		13,65	14,1	—		
7-Segment Outputs Output Low (Sink) Current Min. I _{OL}	—	0,4	0,5	5	1,28	1,22	0,84	0,72	1	2	—	mA
	—	0,5	0,10	10	3,2	3	2,2	1,8	2,6	5,2	—	
	—	1,5	0,15	15	8,4	8	5,6	4,8	6,8	13,6	—	
Carry Outputs Output Low (Sink) Current Min. I _{OL}	—	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	—	mA
	—	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	—	
	—	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	—	
Output High (Source) Current Min. I _{OH}	—	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	—	mA
	—	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	—	
	—	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	—	
	—	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	—	
Input Current Max. I _{IN}	—	0,18	0,18	18	±0,1	±0,1	±1	±1	—	±10 ⁻⁵	±0,1	μA

■ 0(10 μA)

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD40110B Types

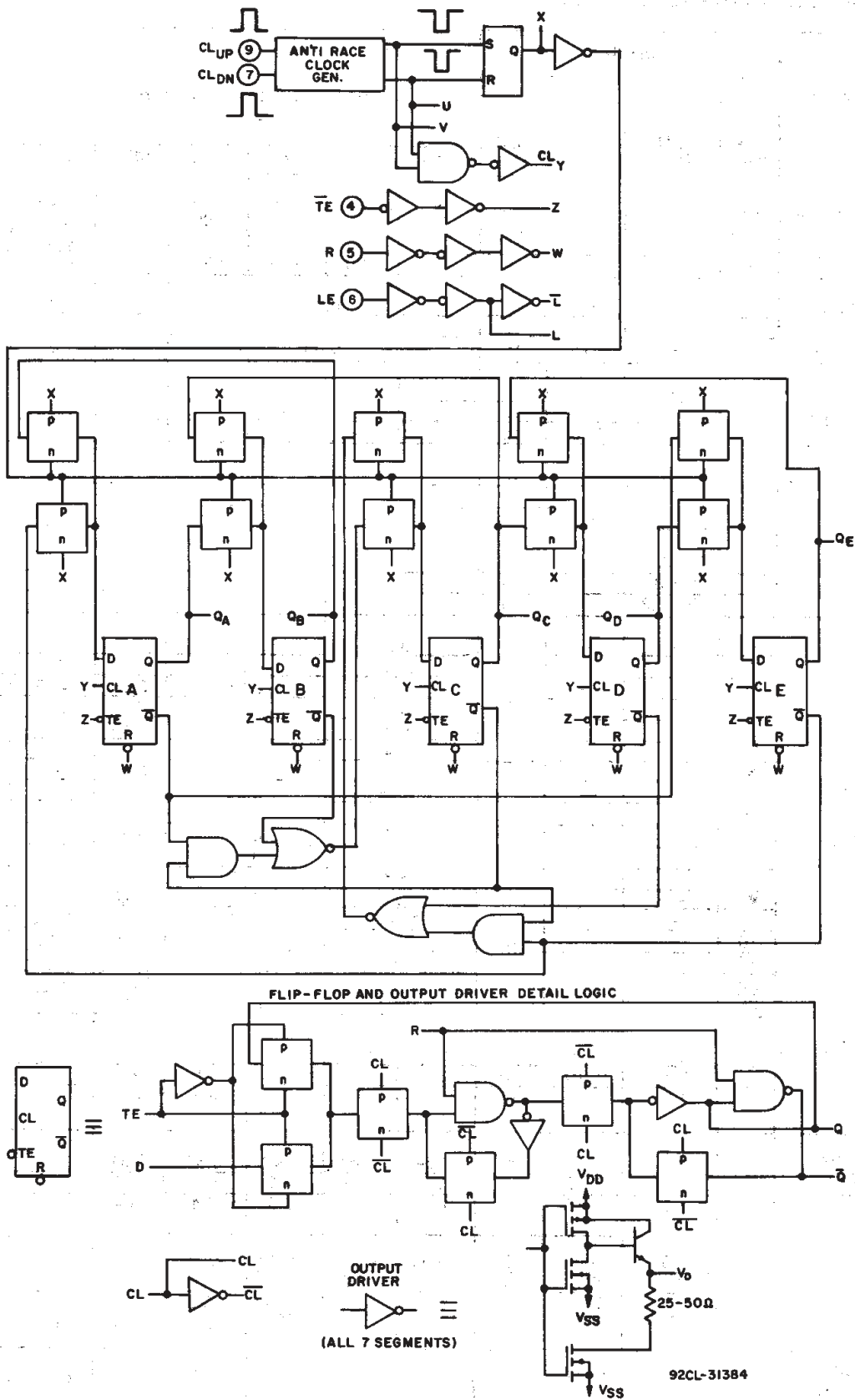
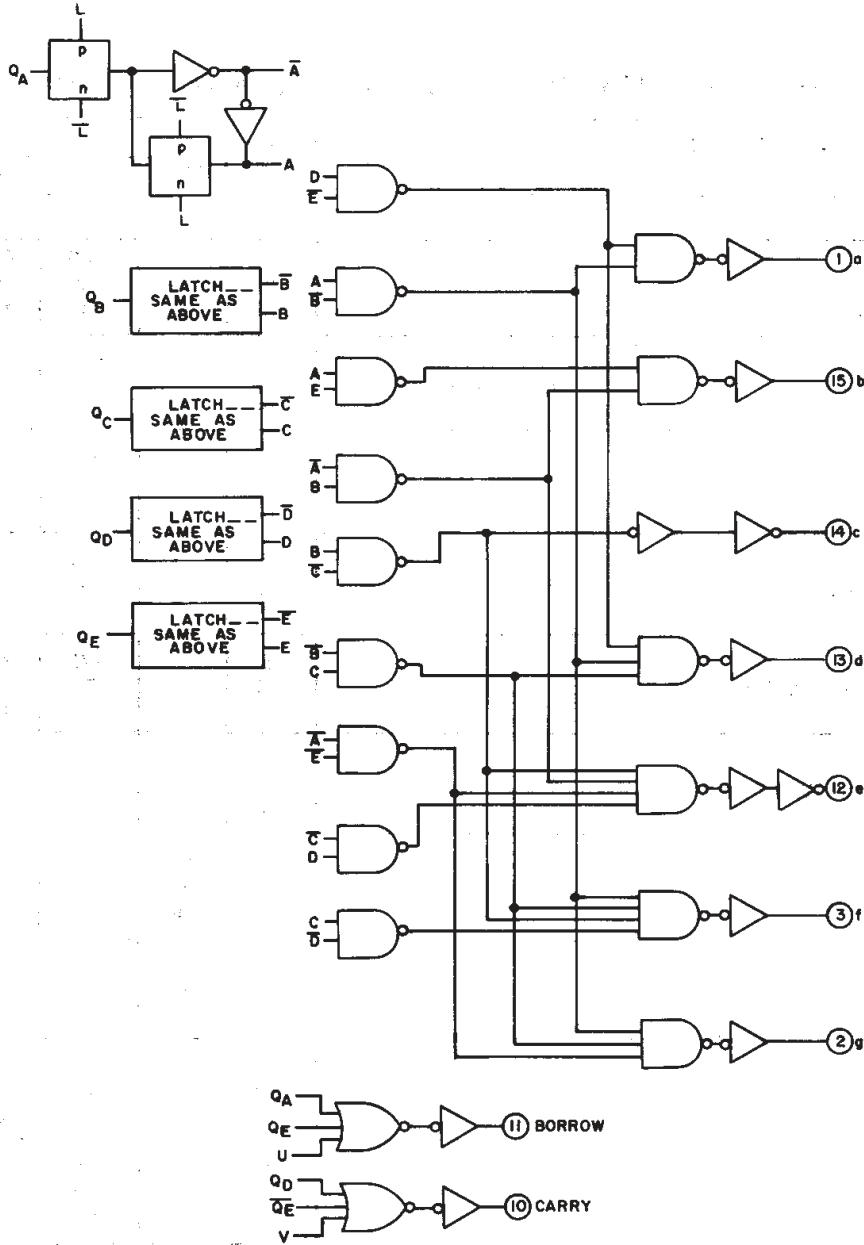


Fig. 2 - Logic diagram with flip-flop and output-driver details.
(cont'd on page 5)

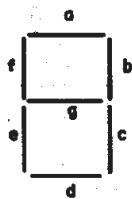
CD40110B Types



92CL-31384

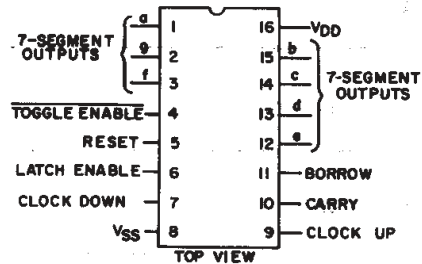
Fig. 2 - Logic diagram with flip-flop and output-driver details.

DISPLAY SEGMENTS



92CS-31376

TERMINAL ASSIGNMENT



92CS-31377

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CD40110B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Clock Up/Clock Down					
Propagation Delay Time: Clock to Carry or Borrow t_{PLH}, t_{PHL}	5	—	300	600	ns
	10	—	100	200	
	15	—	70	140	
Clock to Segment t_{PLH}, t_{PHL}	5	—	925	1850	
	10	—	360	720	
	15	—	250	500	
Minimum Clock Pulse Width	5	—	55	110	
	10	—	20	40	
	15	—	15	30	
Maximum Clock Input Frequency (Sum of CL_{UP} & CL_{DN}) f_{CL}	5	1	2.5	—	MHz
	10	3	6	—	
	15	5	8.5	—	
Minimum Toggle Enable Pulse Width	5	—	175	350	ns
	10	—	75	150	
	15	—	55	110	
Minimum Latch Enable Pulse Width	5	—	55	110	
	10	—	15	30	
	15	—	12	24	
Output Pulse Width: Carry	5	115	230	—	
	10	60	120	—	
	15	40	75	—	
Borrow	5	140	275	—	
	10	65	130	—	
	15	45	85	—	
Transition Time: Carry or Borrow t_{TLH}, t_{THL}	5	—	85	170	
	10	—	45	90	
	15	—	30	60	
Minimum Delay Time Between CL_{UP} & CL_{DN}	5	—	100	—	
	10	—	80	—	
	15	—	60	—	
Maximum Clock Rise or Fall Time t_{rCL}, t_{fCL}	5	—	—	15	μs
	10	—	—	15	
	15	—	—	15	
Reset					
Propagation Delay Time Reset to Output t_{PLH}, t_{PHL}	5	—	650	1300	ns
	10	—	350	700	
	15	—	160	320	
Minimum Reset Removal Time	5	—	-275	0	
	10	—	-100	0	
	15	—	-65	0	
Minimum Reset Pulse Width	5	—	175	350	
	10	—	85	170	
	15	—	60	120	

CD40110B Types

TRUTH TABLE

CLOCK UP*	CLOCK DOWN*	LATCH ENABLE	TOGGLE ENABLE	RESET	COUNTER	DISPLAY
	X	0	0	0	Increments by 1	Follows Counter
X		0	0	0	Decrements by 1	Follows Counter
		X	X	0	No Change	No Change
X	X	1	X	1	Goes to 00000	Remains Fixed
X	X	0	X	1	Goes to 00000	Follows Counter (Display =)
X	X	X	1	0	Inhibited	Remains Fixed
	X	1	0	0	Increments by 1	Remains Fixed
X		1	0	0	Decrements by 1	Remains Fixed

X = Don't Care 1 = High State 0 = Low State

* Typically 100 ns between clock-up and clock-down positive transitions are required to ensure proper counting.

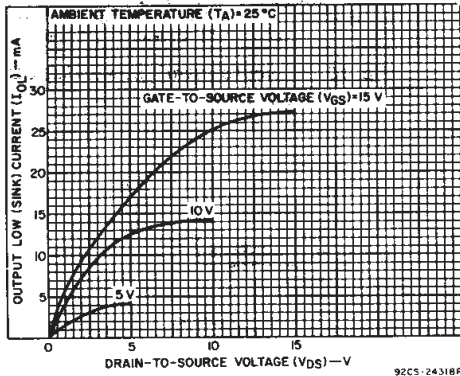


Fig. 3 - Typical carry or borrow output low (sink) current characteristics.

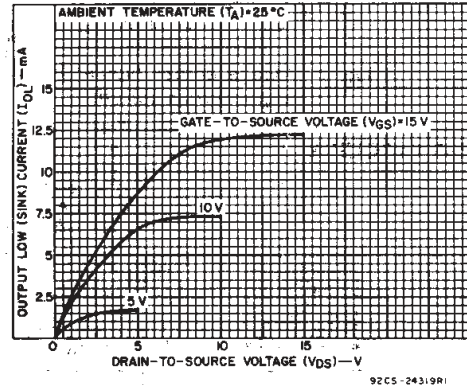


Fig. 4 - Minimum carry or borrow output low (sink) current characteristics.

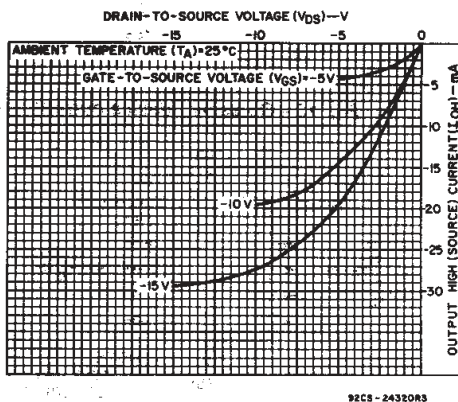


Fig. 5 - Typical carry or borrow output high (source) current characteristics.

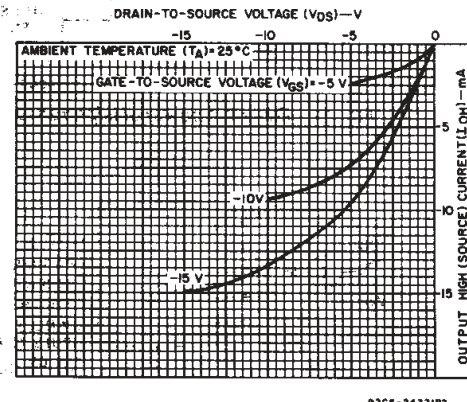


Fig. 6 - Minimum carry or borrow output high (source) current characteristics.

CD40110B Types

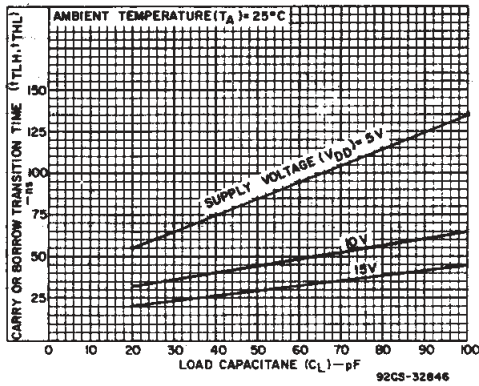


Fig. 7 - Typical carry or borrow transition time vs. load capacitance.

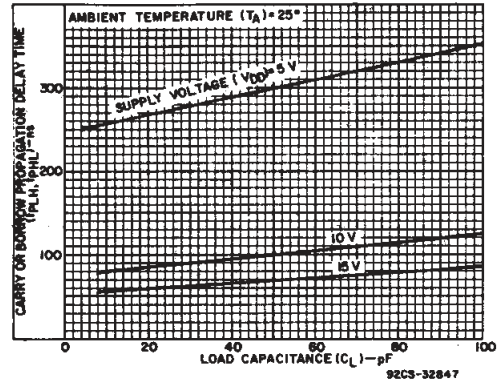


Fig. 8 - Typical carry or borrow propagation delay time vs. load capacitance.

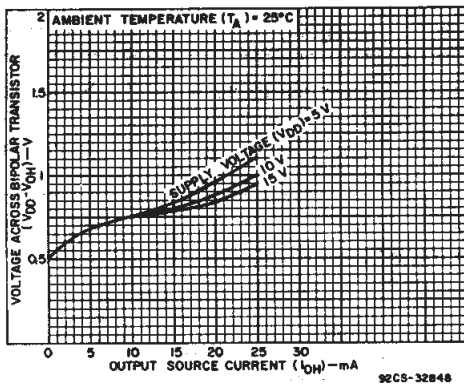


Fig. 9 - Voltage across bipolar transistor vs. output source current.

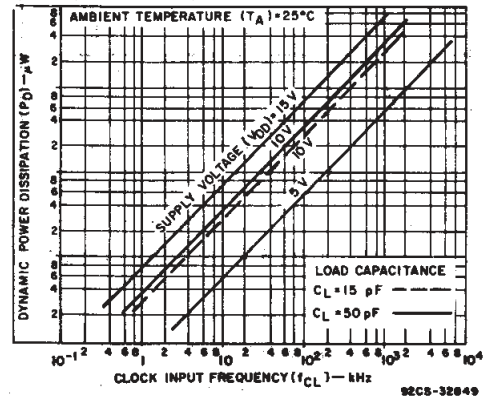


Fig. 10 - Typical dynamic power dissipation vs. frequency.

TEST CIRCUITS

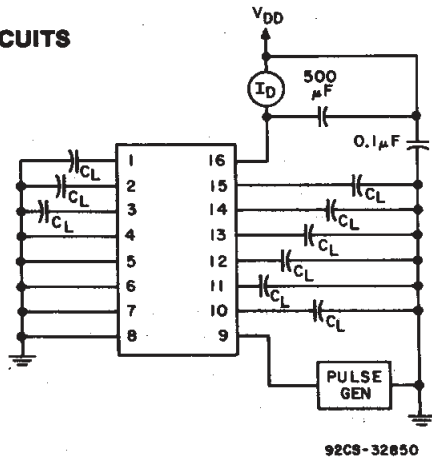


Fig. 11 - Dynamic power dissipation test circuit.

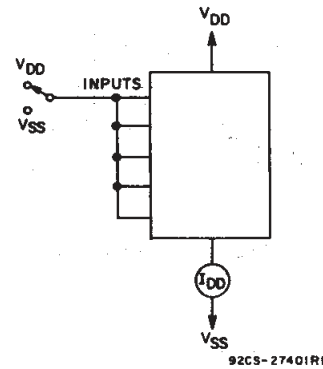


Fig. 12 - Quiescent device current.

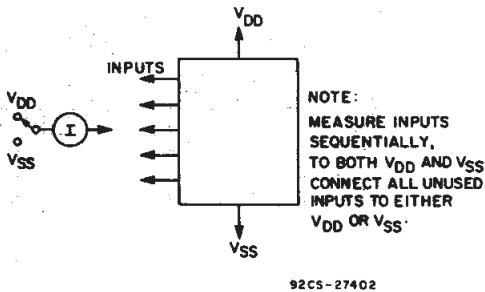


Fig. 13 - Input current.

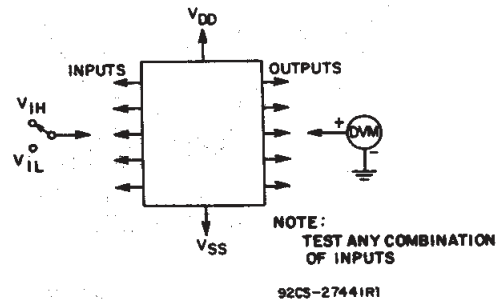


Fig. 14 - Input voltage.

CD40110B Types

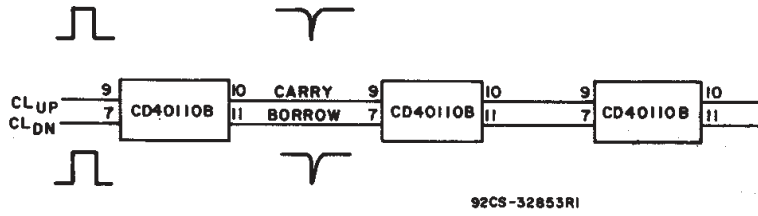
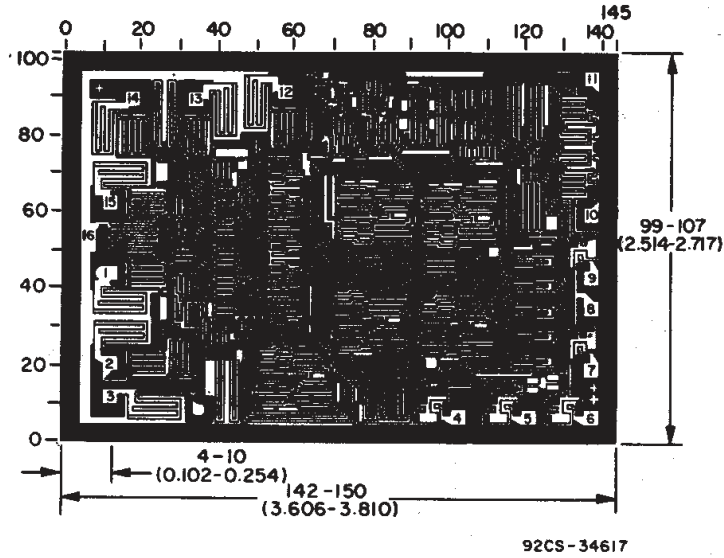


Fig. 15 - Cascading diagram.



Dimensions and pad layout for CD40110B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40110BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD40110BE	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

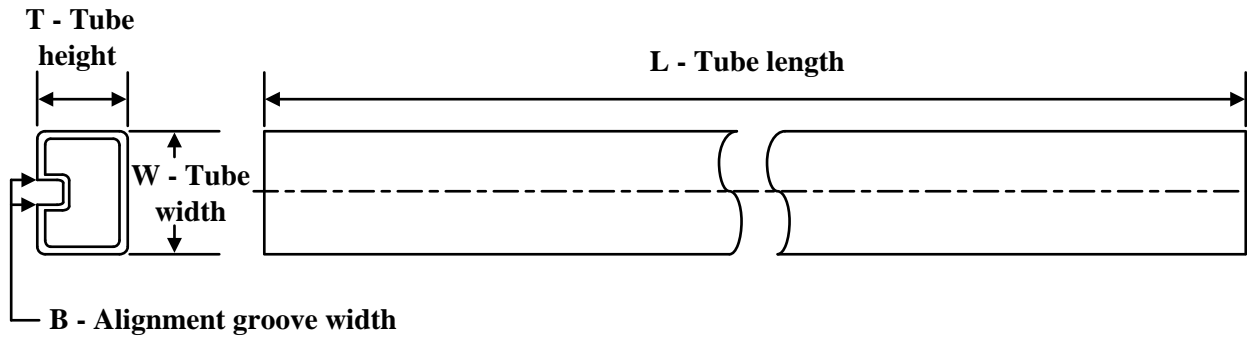
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD40110BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40110BE	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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