# TPS84259 4.5-V to 40-V Input, 15-W, Negative Output, Integrated Power Solution

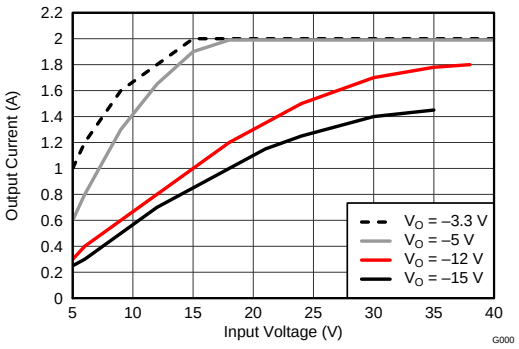
## 1 FEATURES

- Complete Integrated Power Solution Allows Small Footprint, Low-Profile Design
- Wide Input-Voltage Range from 4.5 V to 40 V
- Output Adjustable from –3 V to –17 V
- Supplies up to 2-A of Output Current
- 45-V Surge Capability
- Synchronizes to an External Clock
- Adjustable Slow Start
- Programmable Undervoltage Lockout (UVLO)
- Output Overcurrent Protection
- Overtemperature Protection
- Operating Temperature Range: –40°C to +85°C
- Enhanced Thermal Performance: 14°C/W
- Meets EN55022 Class B Emissions
- For Design Help visit http://www.ti.com/TPS84259

## 2 APPLICATIONS

- Industrial and Motor Controls
- Automated Test Equipment
- Bipolar Amplifiers in Audio/Video
- High Density Power Systems

**Safe Operating Current**

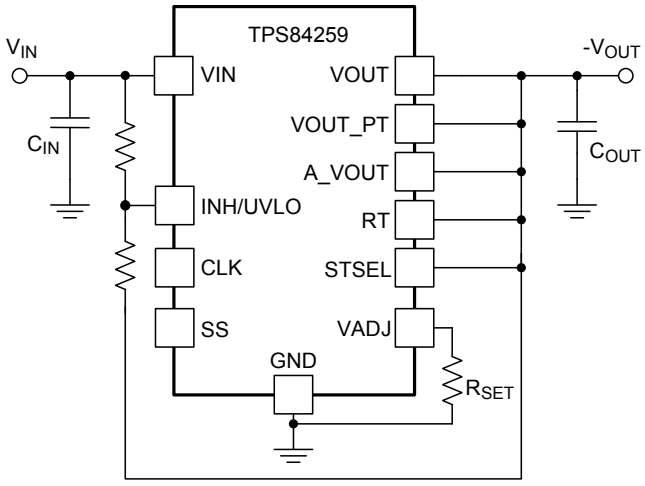



## 3 DESCRIPTION

The TPS84259 is an easy-to-use negative output voltage power module that combines a 15-W DC/DC converter with an inductor, and passives into a low-profile QFN package. This total power solution allows as few as five external components and eliminates the loop compensation and magnetics part selection process.

The 9 × 11 × 2.8 mm QFN package is easy to solder onto a printed circuit board. Its compact design also contains fewer components and possesses excellent power dissipation capability. The TPS84259 offers the flexibility and the feature-set of a discrete design and is ideal for powering a wide range of ICs and analog circuits requiring a negative output voltage. Advanced packaging technology affords a robust and reliable power solution, compatible with standard QFN mounting and testing techniques.

**SIMPLIFIED APPLICATION**





9 mm × 11 mm × 2.8 mm

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

**Table 1. ORDERING INFORMATION**

| |
|---|
| **For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at** www.ti.com. |

# 4 Specifications

## 4.1 ABSOLUTE MAXIMUM RATINGS(1)

| Over Operating Temperature Range (Unless Otherwise Noted) | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input Voltage | VIN | –0.3 | 45 | V |
| | INH/UVLO | –0.3 | 5(2) | V |
| | VADJ | –0.3 | 3(2) | V |
| | SS | –0.3 | 3(2) | V |
| | STSEL | –0.3 | 3(2) | V |
| | RT | –0.3 | 3.6(2) | V |
| | CLK | –0.3 | 3.6(2) | V |
| Output Voltage | PH | –0.6 | 45 | V |
| | PH 10ns Transient | –2 | 45 | V |
| | VOUT | –0.6 | VIN(2) | V |
| $V_{DIFF}$ (VOUT to exposed thermal pad) | | | ±200 | mV |
| Source Current | INH/UVLO | | 100 | µA |
| Sink Current | SS | | 200 | µA |
| Operating Junction Temperature | | –40 | 105(3) | °C |
| Storage Temperature | | –65 | 150 | °C |
| Peak Reflow Case Temperature(4)(5) | | | 250 | °C |
| Maximum Number of Reflows Allowed(4)(5) | | | 3 | |
| Mechanical Shock | Mil-STD-883D, Method 2002.3, 1 ms, 1/2 sine, mounted | | 1500 | G |
| Mechanical Vibration | Mil-STD-883D, Method 2007.2, 20-2000Hz | | 20 | |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This voltage rating is referenced to A_VOUT, not GND.
(3) See the temperature derating curves in the Typical Characteristics section for thermal information.
(4) For soldering specifications, refer to the *Soldering Requirements for BQFN Packages* application note.
(5) Devices with a date code prior to week 14 2018 (1814) have a peak reflow case temperature of 240°C with a maximum of one reflow.

## 4.2 RECOMMENDED OPERATING CONDITIONS

| Over Operating Free-Air Temperature Range (Unless Otherwise Noted) | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input Voltage | 4.5 | 40 | V |
| $V_{OUT}$ | Output Voltage | –3.0 | –17 | V |

## 4.3 PACKAGE SPECIFICATIONS

| TPS84259 | | UNIT |
|---|---|---|
| Weight | | 0.9 grams |
| Flammability | Meets UL 94 V-O | |
| MTBF Calculated reliability | Per Bellcore TR-332, 50% stress, $T_A$ = 40°C, ground benign | 31.7 MHrs |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## 4.4 ELECTRICAL CHARACTERISTICS

-40°C ≤ $T_A$ ≤ +85°C, $V_{IN}$ = 12 V, $V_{OUT}$ = –5.0 V, $I_{OUT}$ = 2.0A
$C_{IN}$ = 2 x 2.2 µF ceramic, $C_{OUT}$ = 2 x 47 µF ceramic (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{OUT}$ | Output current | Over input voltage and output voltage range | | 0 (1) | | 2.0 (2) | A |
| $V_{IN}$ | Input voltage range | Over output current range | | 4.5 | | 40 (3) | V |
| UVLO | $V_{IN}$ Undervoltage lockout | Rising only, $R_{UVLO1}$ = 174 kΩ, $R_{UVLO2}$ = 63.4 kΩ | | | 4.5 | | V |
| $V_{OUT(adj)}$ | Output voltage adjust range | Over output current range | | –3.0 | | –17 (3) | V |
| $V_{OUT}$ | Set-point voltage tolerance | $T_A$ = 25°C, $I_{OUT}$ = 100 mA | | | | 2.0% (4) | |
| | Temperature variation | –40°C ≤ $T_A$ ≤ +85°C | | | ±0.5% | ±1.0% | |
| | Line regulation | Over input voltage range | | | ±0.1% | | |
| | Load regulation | From 100 mA to $I_{OUT(max)}$ | | | ±0.4% | | |
| | Total output voltage variation | Includes set-point, line, load, and temperature variation | | | | 3.0% (4) | |
| η | Efficiency | $V_{IN}$ = 24 V | $V_{OUT}$ = –12 V, $I_{OUT}$ = 1.0 A | | 85 % | | |
| | | | $V_{OUT}$ = –5.0 V, $I_{OUT}$ = 1.0 A | | 81 % | | |
| | | | $V_{OUT}$ = –3.3 V, $I_{OUT}$ = 1.0 A | | 77 % | | |
| | | $V_{IN}$ = 12 V | $V_{OUT}$ = –12 V, $I_{OUT}$ = 0.6 A | | 86 % | | |
| | | | $V_{OUT}$ = –5.0 V, $I_{OUT}$ = 1.0 A | | 81 % | | |
| | | | $V_{OUT}$ = –3.3 V, $I_{OUT}$ = 1.0 A | | 78 % | | |
| | Output voltage ripple | 20 MHz bandwith, 100 mA ≤ $I_{OUT}$ ≤ $I_{OUT(max)}$ | | | 1% | | $V_{OUT}$ |
| $I_{LIM}$ | Current limit threshold | | | | 3.0 (5) | | A |
| | Transient response | 1.0 A/µs load step from 25 to 75% $I_{OUT(max)}$ | Recovery time | | 500 | | µs |
| | | | $V_{OUT}$ over/undershoot | | 80 | | mV |
| $V_{INH}$ | Inhibit threshold voltage | INH with respect to A_VOUT | | 1.15 | 1.25 | 1.36 (6) | V |
| $I_{INH}$ | INH Input current | $V_{INH}$ < 1.15 V | | | –0.9 | | µA |
| | | $V_{INH}$ > 1.36 V | | | –3.8 | | µA |
| $I_{I(stby)}$ | Input standby current | INH pin to A_VOUT | | | 1.3 | 4 | µA |
| $f_{SW}$ | Switching frequency | RT pin to A_VOUT | | 700 | 800 | 900 | kHz |
| $f_{CLK}$ | Synchronization frequency | | $R_{RT}$ = 0 Ω | 700 (7) | | 900 (7) | kHz |
| | | | $R_{RT}$ = 93.1 kΩ | 400 (7) | | 600 (7) | kHz |
| $V_{CLK-H}$ | CLK High-Level Threshold | With respect to A_VOUT | | | 1.9 | 2.2 | V |
| $V_{CLK-L}$ | CLK Low-Level Threshold | With respect to A_VOUT | | 0.5 | 0.7 | | V |
| $D_{CLK}$ | CLK Duty cycle | | | 25% | 50% | 75% | |
| | Thermal Shutdown | Thermal shutdown | | | 180 | | °C |
| | | Thermal shutdown hysteresis | | | 15 | | °C |
| $C_{IN}$ | External input capacitance | | Ceramic | 4.7 (8) | 10 | | µF |
| | | | Non-ceramic | | 22 | | |
| $C_{OUT}$ | External output capacitance | | | 100 (9) | | 430 (9) | µF |

(1) This device can regulate $V_{OUT}$ down to 0 A, however the ripple may increase due to pulse-skipping at light loads. See Light-Load Behavior for more information. See No-Load Operation when operating at 0 A.
(2) The maximum current is dependant on $V_{IN}$ and $V_{OUT}$, see Figure 33.
(3) The sum of $V_{IN}$ + |$V_{OUT}$| must not exceed 50 V.
(4) The stated limit of the set-point voltage tolerance includes the tolerance of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external $R_{SET}$ resistor.
(5) This product is not designed to endure a sustained (> 5 sec) over-current condition.
(6) If this pin is left open circuit, the device operates when input power is applied. An external level-shifter is required to interface with this pin. See Output On/Off Inhibit (INH) for further guidance.
(7) The synchronization frequency is dependant on $V_{IN}$ and $V_{OUT}$ as shown in Switching Frequency. $R_{RT}$ must be either 0 Ω or 93.1kΩ.
(8) A minimum of 4.7 µF of ceramic external capacitance is required across the input (VIN and PGND connected) for proper operation. Locate the capacitor close to the device. See Table 3 for more details.
(9) The amount of required capacitance must include at least 2 x 47 µF ceramic capacitor (or 4 x 22 µF). Locate the capacitance close to the device. Adding additional capacitance close to the load improves the response of the regulator to load transients. See Table 3 for more details. See Inrush Current section when adding additional output capacitance.

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## 4.5 THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS84259 RKG 41 PINS | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(2) | 14 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter(3) | 3.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(4) | 6.8 | |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, literature number SPRA953.
(2) The junction-to-ambient thermal resistance, $\theta_{JA}$, applies to devices soldered directly to a 100 mm x 100 mm double-sided PCB with 1 oz. copper and natural convection cooling. Additional airflow reduces $\theta_{JA}$.
(3) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JT} * Pdis + T_T$; where Pdis is the power dissipated in the device and $T_T$ is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature, $T_J$, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} * Pdis + T_B$; where Pdis is the power dissipated in the device and $T_B$ is the temperature of the board 1mm from the device.


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# 5 DEVICE INFORMATION

## FUNCTIONAL BLOCK DIAGRAM

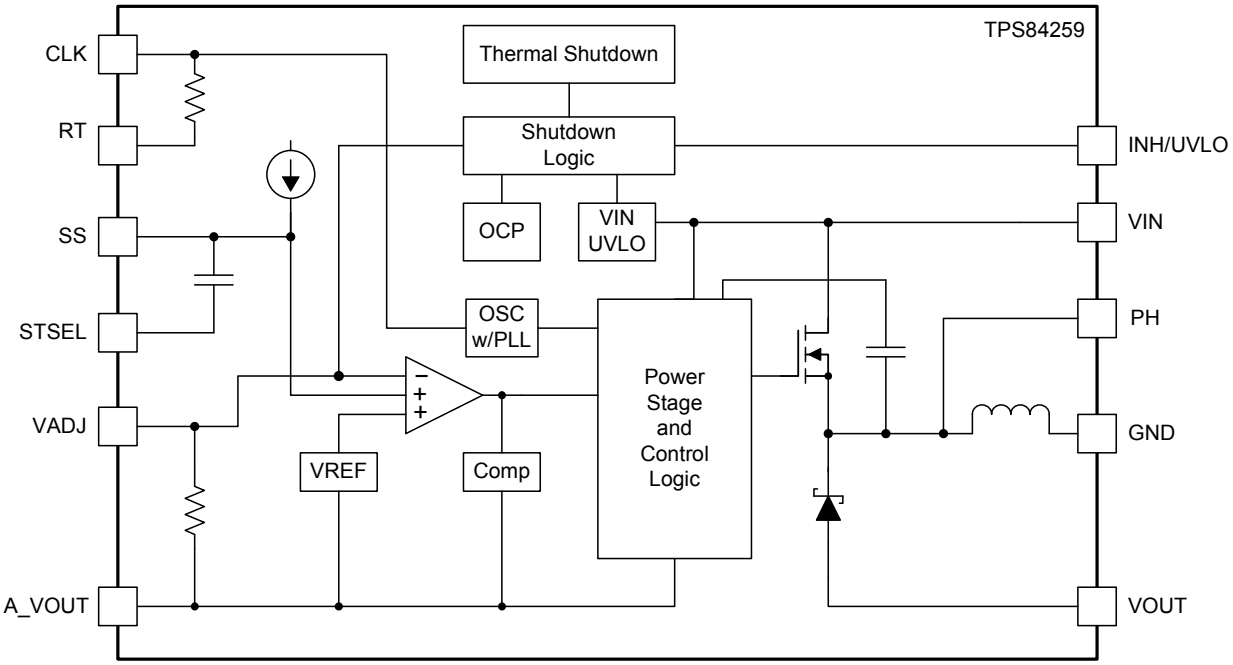

**Table 2. PIN DESCRIPTIONS**

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| VIN | 26 | Input voltage. This pin supplies all power to the converter. Connect this pin to the input supply and connect bypass capacitors between this pin and GND. |
| VOUT | 16 | Negative output voltage with respect to GND. Connect these pins to the output load and connect external bypass capacitors between these pins and GND. Pad 40 should be connected to PCB VOUT planes using multiple vias for good thermal performance. |
| | 17 | |
| | 18 | |
| | 19 | |
| | 20 | |
| | 40 | |
| GND | 10 | This is the return current path for the power stage of the device. These pins are connected to the internal output inductor. Connect these pins to the load and to the bypass capacitors associated with VIN and VOUT. |
| | 11 | |
| | 12 | |
| | 13 | |
| | 14 | |
| | 15 | |
| | 39 | |
| PH | 6 | Phase switch node. Do not place any external component on these pins or tie them to a pin of another function. |
| | 7 | |
| | 21 | |
| | 22 | |
| | 23 | |
| | 24 | |
| | 38 | |
| | 41 | |
| VOUT_PT | 8 | VOUT and A_VOUT Connection Point. Connect VOUT to A_VOUT at these pins as shown in the Layout Considerations section. These pins are not connected to internal circuitry, and are not connected to one another. |
| | 9 | |
| DNC | 2 | Do Not Connect. Do not connect these pins to GND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad. |
| | 3 | |
| | 25 | |
| | 35 | |
| A_VOUT | 1 | These pins are connected to the internal analog reference (A_VOUT) of the device. This node should be treated as the negative voltage reference for the analog control circuitry. Pad 37 should be connected to the PCB A_VOUT plane using multiple vias for good thermal performance. Not all pins are connected together internally. All pins must be connected together externally with a copper plane or pour directly under the module. Connect A_VOUT to VOUT at a single point (VOUT_PT; pins 8 & 9). See Layout Recommendations. |
| | 4 | |
| | 5 | |
| | 32 | |
| | 33 | |
| | 34 | |
| | 37 | |
| RT | 30 | Switching frequency adjust pin. To operate at the recommended free-running frequency, connect this pin to A_VOUT. Connecting a resistor between this pin and A_VOUT will reduce the switching frequency. See Switching Frequency section. |
| CLK | 31 | Use this pin to synchronize to an external clock. If unused, isolate this pin from any other signal. |
| INH/UVLO | 27 | Inhibit and UVLO adjust pin. Use an external level-shifter device to ground this pin to control the INH function. A resistor divider between this pin, A_VOUT, and VIN sets the UVLO voltage. |
| SS | 28 | Slow-start pin. Connecting an external capacitor between this pin and A_VOUT adjusts the output voltage rise time. |
| STSEL | 29 | Slow-start select. Connect this pin to A_VOUT to enable the internal SS capacitor. |
| VADJ | 36 | Connecting a resistor between this pin and GND sets the output voltage. A dedicated GND sense line connected at the load will improve regulation at the load. See Figure 48 in the Layout Considerations section. |


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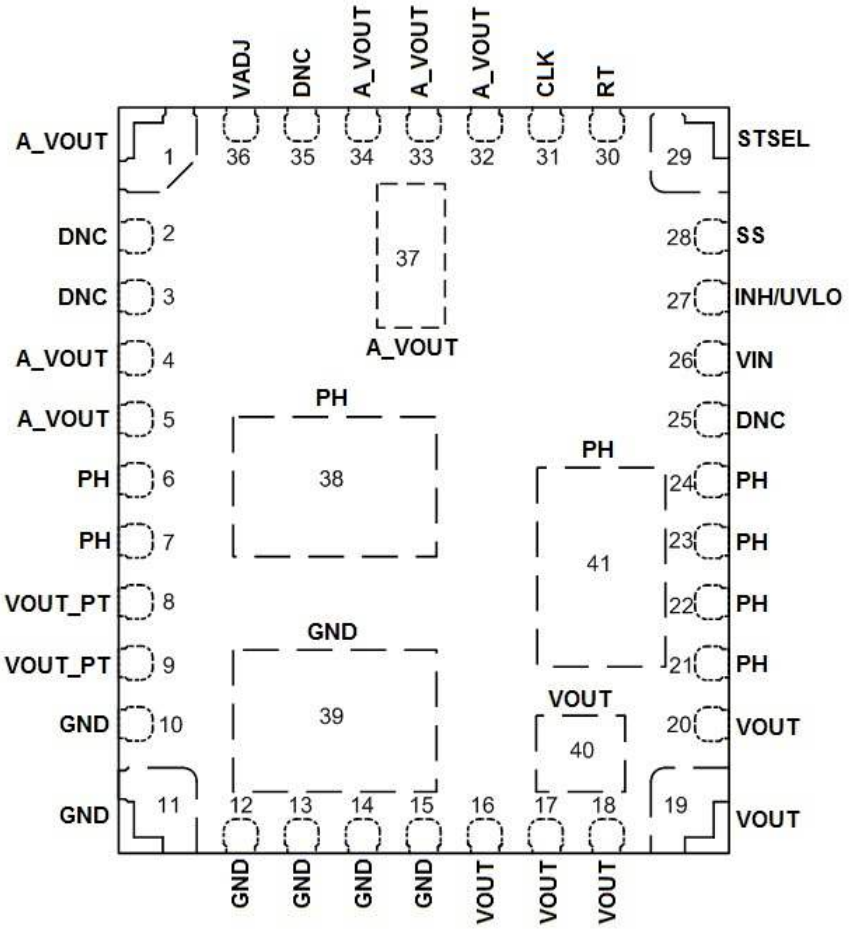
**RKG PACKAGE**
**(TOP VIEW)**



# 6 TYPICAL CHARACTERISTICS (VIN = 5 V) (1) (2)

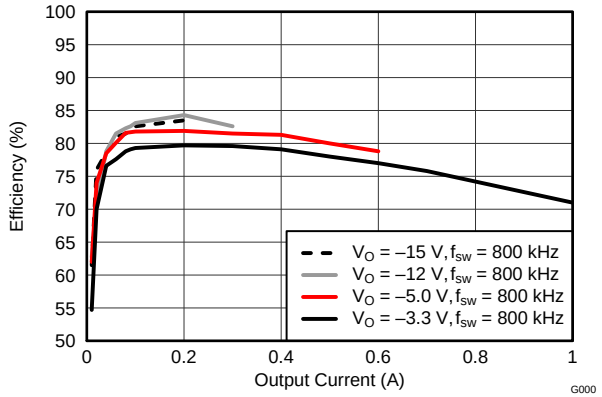



**Figure 1. Efficiency vs. Output Current**

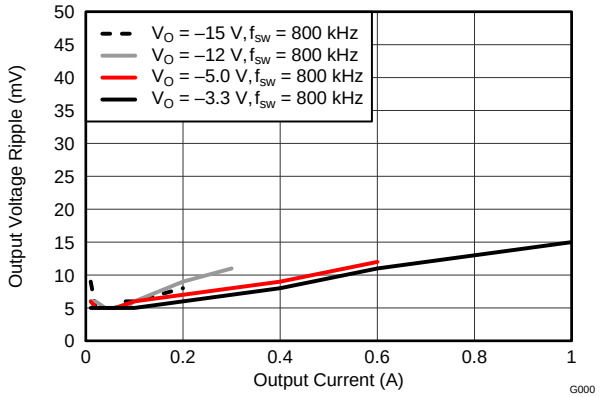



**Figure 2. Voltage Ripple vs. Output Current**

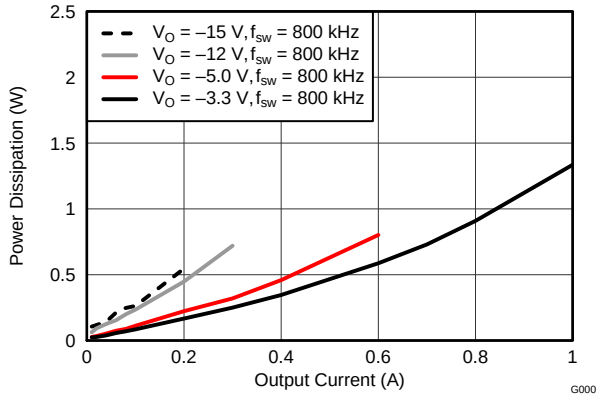



**Figure 3. Power Dissipation vs. Output Current**

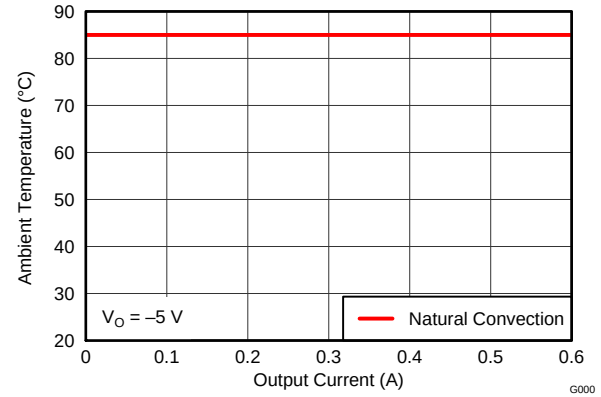



**Figure 4. Safe Operating Area**

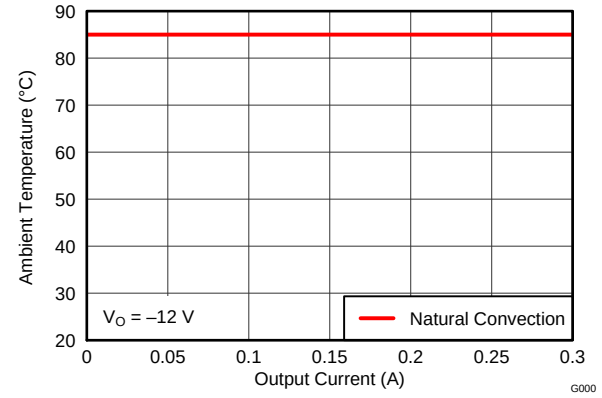



**Figure 5. Safe Operating Area**

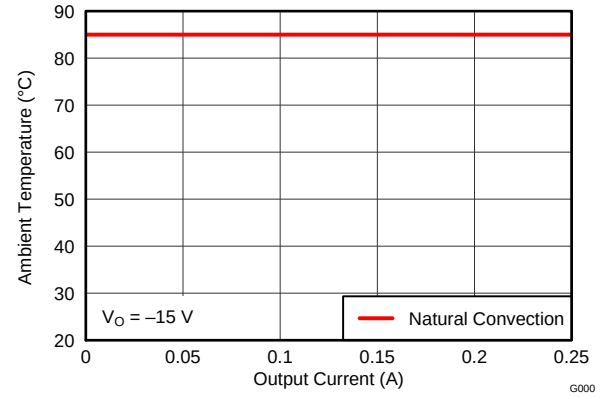



**Figure 6. Safe Operating Area**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to Figure 4, Figure 5, and Figure 6.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# 7 TYPICAL CHARACTERISTICS (VIN = 12 V) (1) (2)

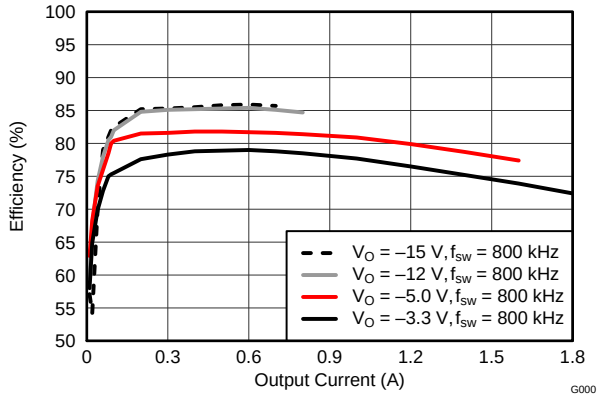


**Figure 7. Efficiency vs. Output Current**

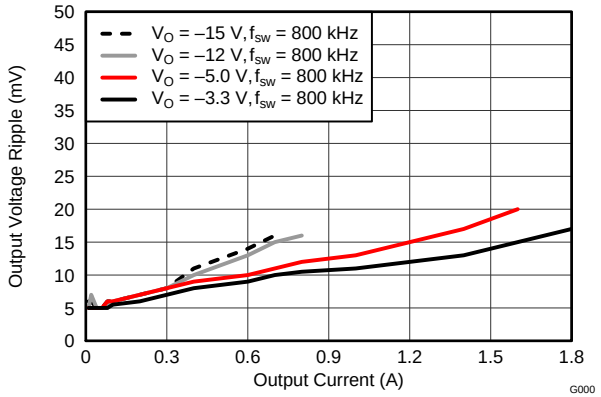


**Figure 8. Voltage Ripple vs. Output Current**

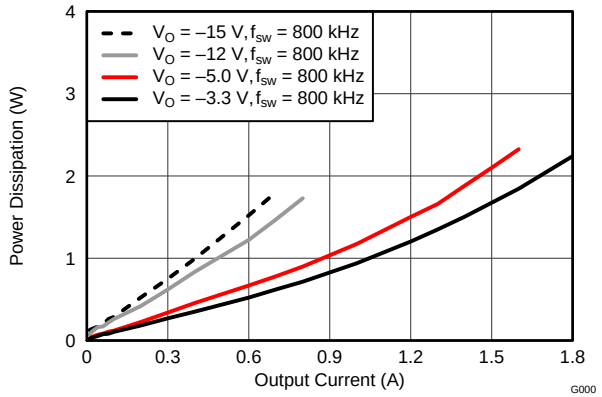


**Figure 9. Power Dissipation vs. Output Current**

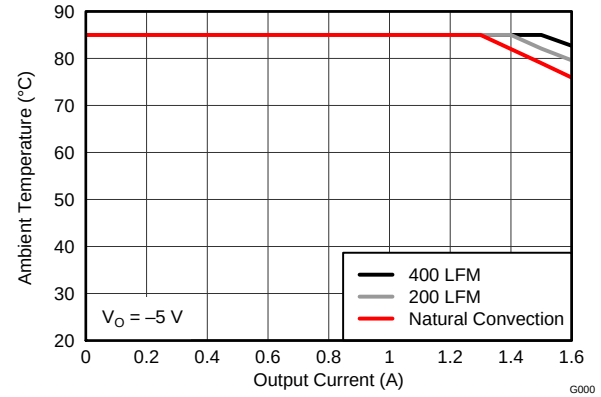


**Figure 10. Safe Operating Area**

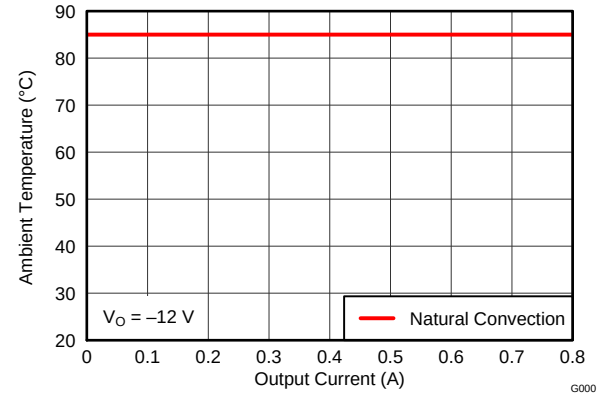


**Figure 11. Safe Operating Area**

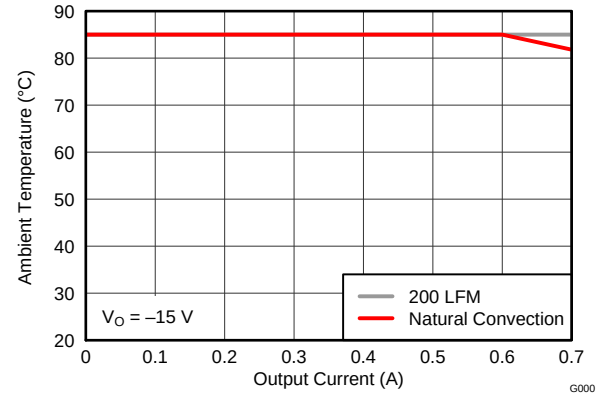


**Figure 12. Safe Operating Area**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 7, Figure 8, and Figure 9.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to Figure 10, Figure 11, and Figure 12.

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# 8 TYPICAL CHARACTERISTICS (VIN = 24 V) (1) (2) (3)

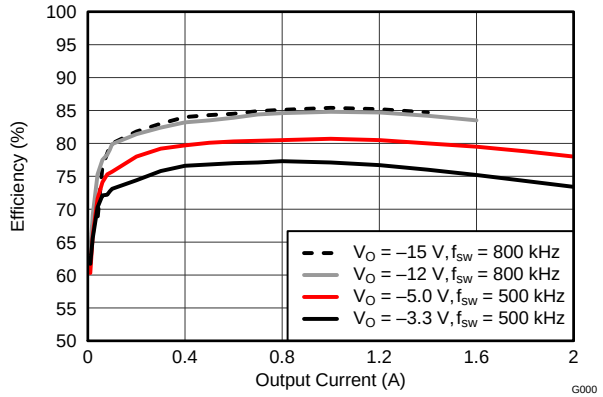


**Figure 13. Efficiency vs. Output Current**

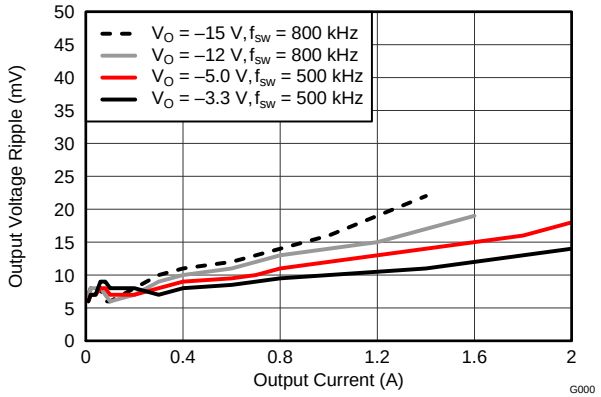


**Figure 14. Voltage Ripple vs. Output Current**

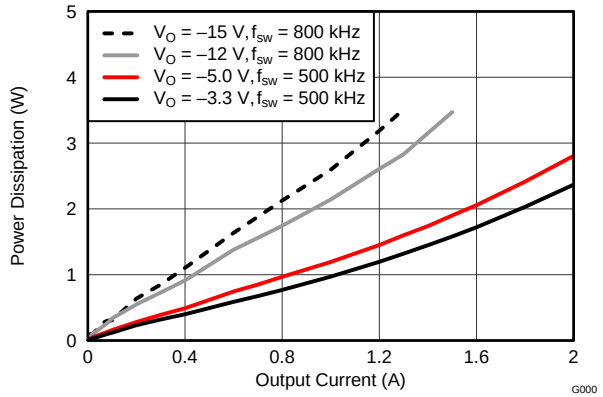


**Figure 15. Power Dissipation vs. Output Current**

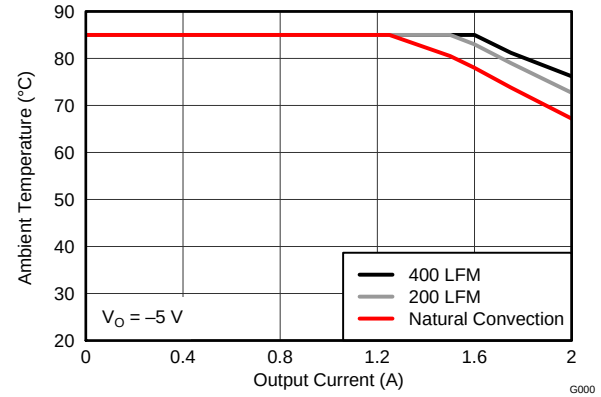


**Figure 16. Safe Operating Area**

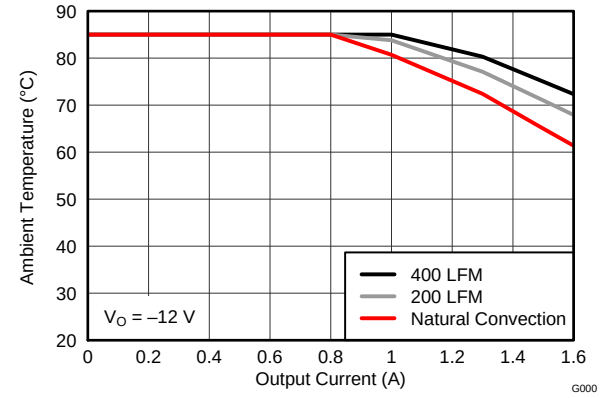


**Figure 17. Safe Operating Area**

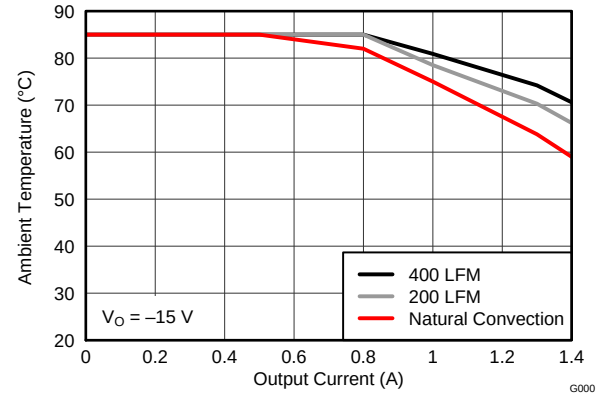


**Figure 18. Safe Operating Area**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 13, Figure 14, and Figure 15.

(2) At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. Applies to Figure 14.

(3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to Figure 16, Figure 17, and Figure 18.


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# 9 TYPICAL CHARACTERISTICS (VIN = 36 V) (1) (2) (3)

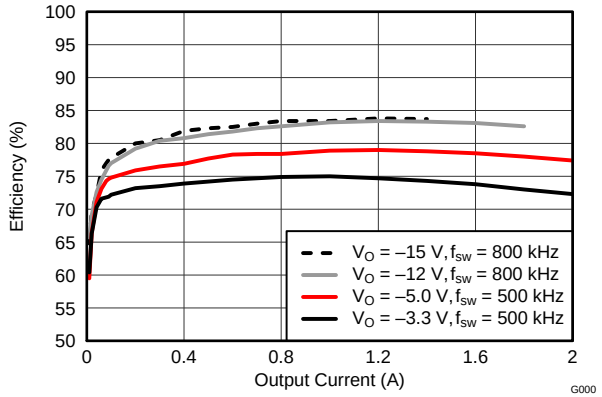


**Figure 19. Efficiency vs. Output Current**

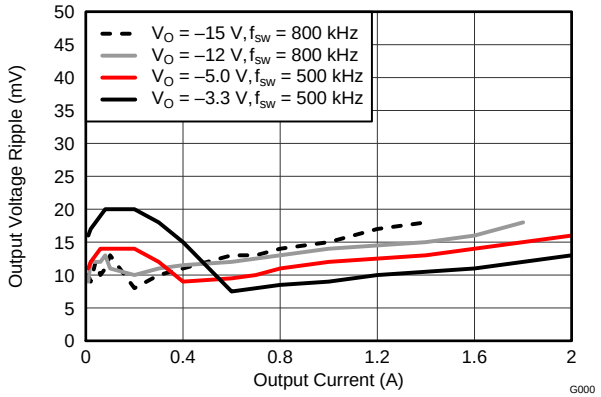


**Figure 20. Voltage Ripple vs. Output Current**

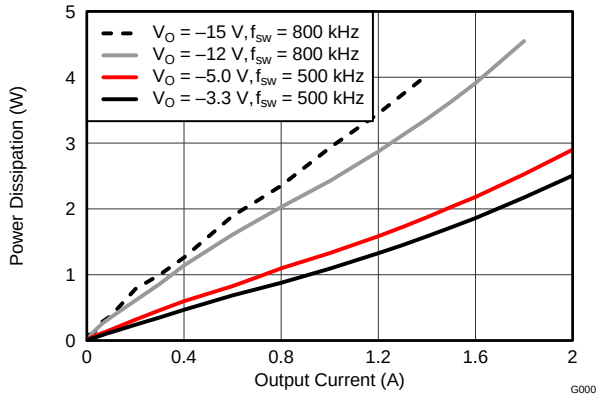


**Figure 21. Power Dissipation vs. Output Current**

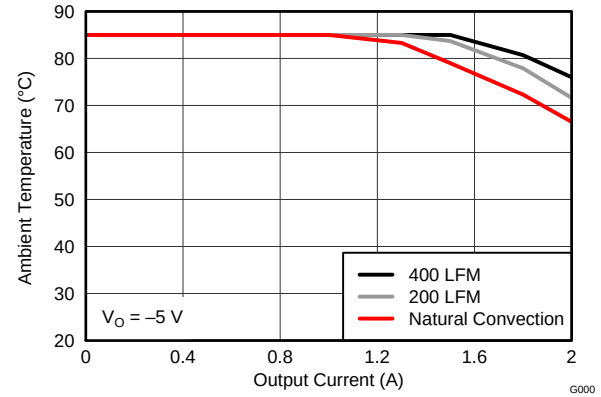


**Figure 22. Safe Operating Area**

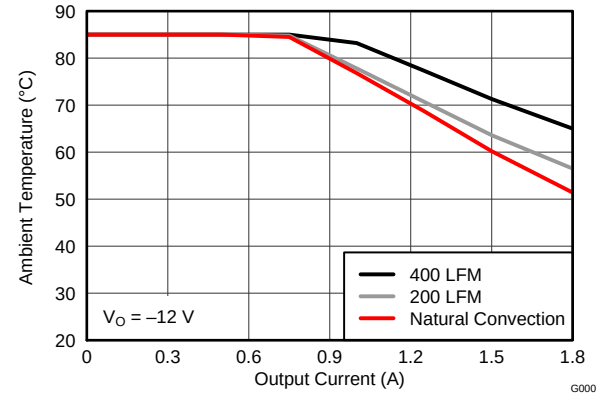


**Figure 23. Safe Operating Area**

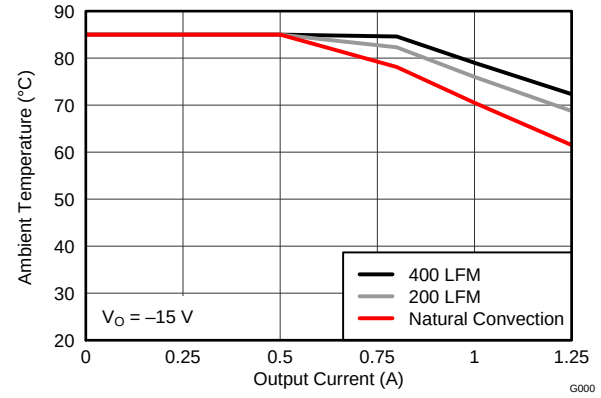


**Figure 24. Safe Operating Area**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 19, Figure 20, and Figure 21.

(2) At light load the output voltage ripple may increase due to pulse skipping. See Light-Load Behavior for more information. Applies to Figure 20.

(3) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to devices soldered directly to a 100 mm × 100 mm, 4-layer, double-sided PCB with 1 oz. copper. Applies to Figure 22, Figure 23, and Figure 24.

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## 10 TYPICAL CHARACTERISTICS (BODE PLOTS) (1)

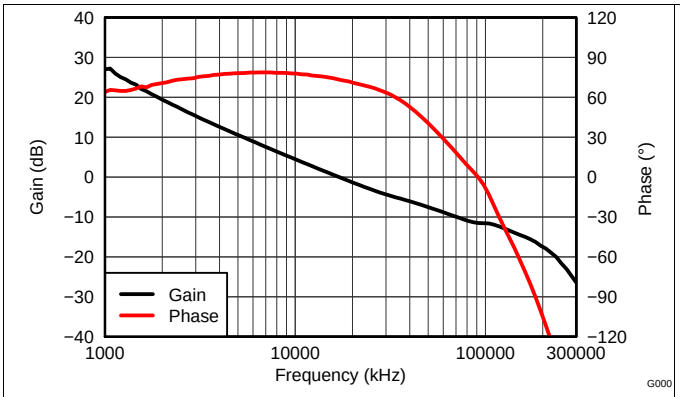


**Figure 25. $V_{IN}$= 5 V, $V_{OUT}$= –5 V, $I_{OUT}$= 0.6 A, $C_{OUT}$= 4 x 22µF ceramic, $f_{SW}$= 800 kHz**

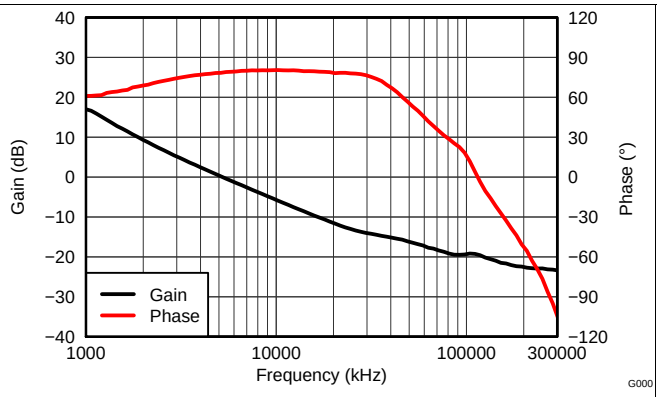


**Figure 26. $V_{IN}$= 5 V, $V_{OUT}$= –12 V, $I_{OUT}$= 0.3 A, $C_{OUT}$= 4 x 22 µF ceramic, $f_{SW}$= 800 kHz**

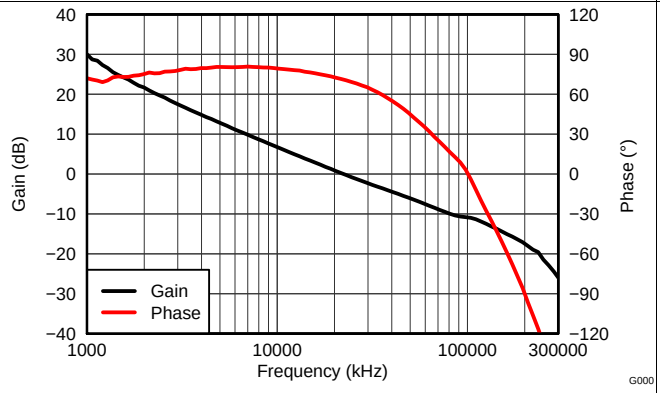


**Figure 27. $V_{IN}$= 12 V, $V_{OUT}$= –5 V, $I_{OUT}$= 1.6 A, $C_{OUT}$= 4 x 22 µF ceramic, $f_{SW}$= 800 kHz**

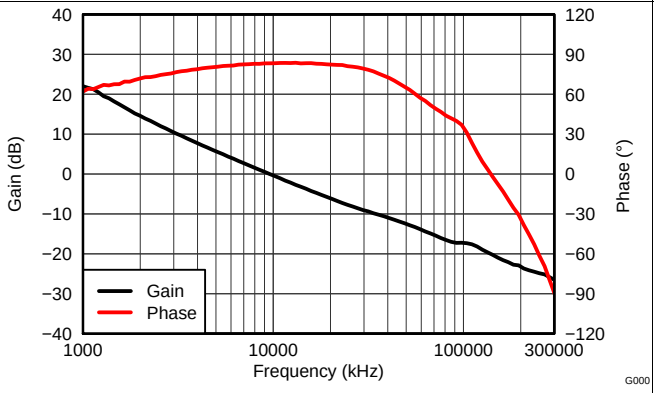


**Figure 28. $V_{IN}$= 12 V, $V_{OUT}$= –12 V, $I_{OUT}$= 0.8 A, $C_{OUT}$= 4 x 22 µF ceramic, $f_{SW}$= 800 kHz**

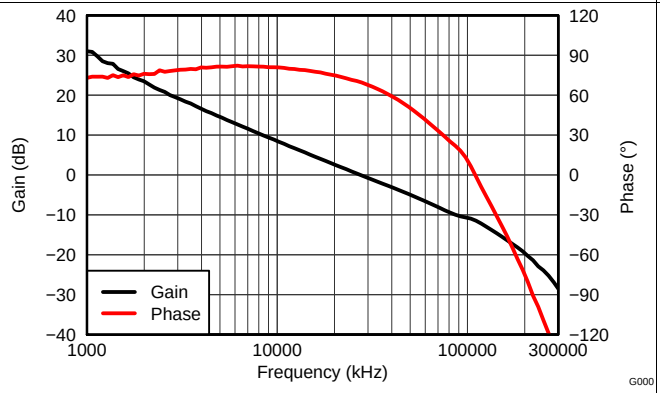


**Figure 29. $V_{IN}$= 24 V, $V_{OUT}$= –5 V, $I_{OUT}$= 2.0 A, $C_{OUT}$= 4 x 22 µF ceramic, $f_{SW}$= 500 kHz**

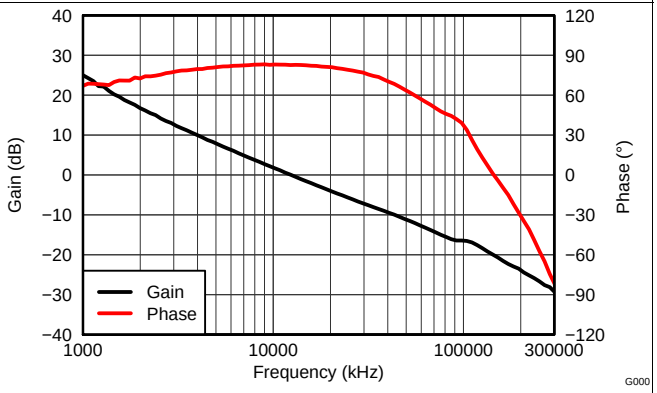


**Figure 30. $V_{IN}$= 24 V, $V_{OUT}$= –12 V, $I_{OUT}$= 1.5 A, $C_{OUT}$= 4 x 22 µF ceramic, $f_{SW}$= 800 kHz**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter.


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## TYPICAL CHARACTERISTICS (BODE PLOTS) (1) (continued)

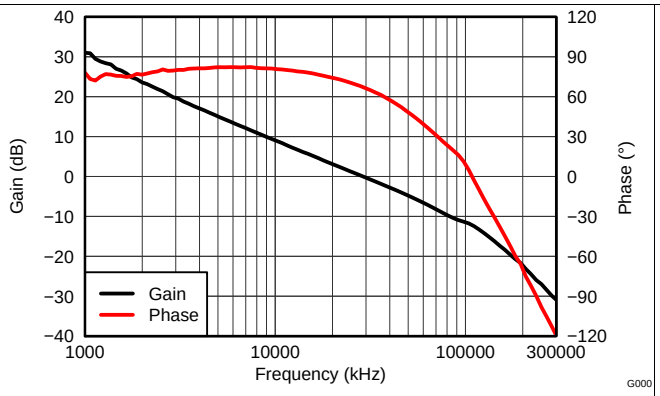


**Figure 31. $V_{IN}$= 36 V, $V_{OUT}$= –5 V, $I_{OUT}$= 2.0 A, $C_{OUT}$= 4 x 22 µF ceramic, $f_{SW}$= 500 kHz**

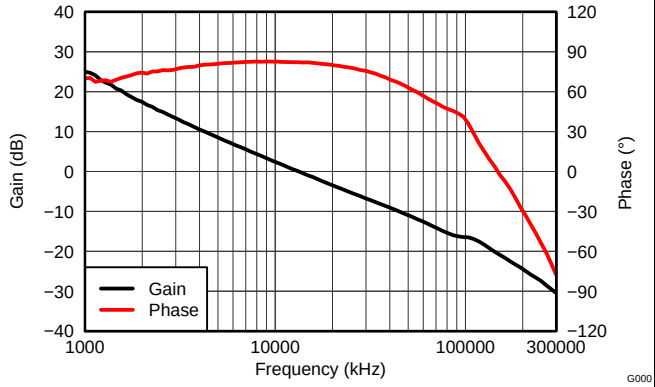


**Figure 32. $V_{IN}$= 36 V, $V_{OUT}$= –12 V, $I_{OUT}$= 1.8 A, $C_{OUT}$= 4 x 22 µF ceramic, $f_{SW}$= 800 kHz**

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# 11 CAPACITOR RECOMMENDATIONS FOR THE TPS84259 POWER SUPPLY

## 11.1 Capacitor Technologies

### 11.1.1 Electrolytic, Polymer-Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Polymer-electrolytic type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo OS-CON capacitor series is suggested due to the lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0°C.

### 11.1.2 Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective than ceramic capacitors above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

### 11.1.3 Tantalum, Polymer-Tantalum Capacitors

Polymer-tantalum type capacitors are recommended for applications where the ambient operating temperature is less than 0°C. The Sanyo POSCAP series and Kemet T530 capacitor series are recommended rather than many other tantalum types due to their lower ESR, higher rated surge, power dissipation, ripple current capability, and small package size. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

## 11.2 Input Capacitor

The TPS84259 requires a minimum input capacitance of 4.7 µF of ceramic type. The voltage rating of input capacitors must be greater than the maximum input voltage. The ripple current rating of the capacitor must be at least 450 mArms. Table 3 includes a preferred list of capacitors by vendor.

## 11.3 Output Capacitor

The required output capacitance of the TPS84259 can be comprised of either all ceramic capacitors, or a combination of ceramic and bulk capacitors. The required output capacitance must include at least 2 × 47 µF of ceramic type (or 4 × 22 µF). The voltage rating of output capacitors must be greater than the output voltage. When adding additional non-ceramic bulk capacitors, low-ESR devices like the ones recommended in Table 3 are required. Additional capacitance above the required minimum is determined by actual transient deviation requirements. Table 3 includes a preferred list of capacitors by vendor.

**Table 3. Recommended Input/Output Capacitors(1)**

| VENDOR | SERIES | PART NUMBER | CAPACITOR CHARACTERISTICS | | |
|---|---|---|---|---|---|
| | | | WORKING VOLTAGE (V) | CAPACITANCE (µF) | ESR (2) (mΩ) |
| Murata | X5R | GRM31CR61H225KA88L | 50 | 2.2 | 2 |
| TDK | X5R | C3216X5R1H475K | 50 | 4.7 | 2 |
| Murata | X5R | GRM32ER61E226K | 16 | 22 | 2 |
| TDK | X5R | C3225X5R0J476K | 6.3 | 47 | 2 |
| Murata | X5R | GRM32ER60J476M | 6.3 | 47 | 2 |
| Sanyo | POSCAP | 16TQC68M | 16 | 68 | 50 |
| Sanyo | POSCAP | 6TPE100MI | 6.3 | 100 | 25 |
| Kemet | T530 | T530D227M006ATE006 | 6.3 | 220 | 6 |

(1) **Capacitor Supplier Verification, RoHS, Lead-free and Material Details**
Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Maximum ESR @ 100 kHz, 25°C.


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# 12 APPLICATION INFORMATION

## 12.1 Adjusting the Output Voltage

The TPS84259 is designed to provide output voltages from –3 V to –17 V. The output voltage is determined by the value of $R_{SET}$, which must be connected between the VADJ pin (Pin 36) and GND. Table 4 gives the standard external $R_{SET}$ resistor for a number of common bus voltages.

**Table 4. Standard $R_{SET}$ Resistor Values for Common Output Voltages**

| OUTPUT VOLTAGE $V_{OUT}$ (V) | –3.3 | –5.0 | –8.0 | –12.0 | –15.0 |
|---|---|---|---|---|---|
| $R_{SET}$ (kΩ) | 31.6 | 52.3 | 90.9 | 140 | 178 |

For other output voltages the value of $R_{SET}$ can be calculated using the following formula, or simply selected from the range of values given in Table 5.

$$R_{SET} = 10 \times \left( \frac{|V_{OUT}|}{0.798} - 1 \right) \ (k\Omega) \quad (1)$$

**Table 5. Standard $R_{SET}$ Resistor Values**

| $V_{OUT}$ (V) | $R_{SET}$ (kΩ) | | $V_{OUT}$ (V) | $R_{SET}$ (kΩ) | | $V_{OUT}$ (V) | $R_{SET}$ (kΩ) |
|---|---|---|---|---|---|---|---|
| –3.0 | 27.4 | | –7.5 | 84.5 | | –12.5 | 147 |
| –3.3 | 31.6 | | –8.0 | 90.9 | | –13.0 | 154 |
| –3.5 | 34.0 | | –8.5 | 97.6 | | –13.5 | 158 |
| –4.0 | 40.2 | | –9.0 | 102 | | –14.0 | 165 |
| –4.5 | 46.4 | | –9.5 | 110 | | –14.5 | 174 |
| –5.0 | 52.3 | | –10.0 | 115 | | –15.0 | 178 |
| –5.5 | 59.0 | | –10.5 | 121 | | –15.5 | 187 |
| –6.0 | 64.9 | | –11.0 | 127 | | –16.0 | 191 |
| –6.5 | 71.5 | | –11.5 | 133 | | –16.5 | 196 |
| –7.0 | 78.7 | | –12.0 | 140 | | –17.0 | 205 |

## 12.2 Safe Operating Current

The amount of output current that can safely be delivered by the TPS84259 depends on the input voltage and the output voltage. Figure 33 shows the maximum output current for four standard output voltages over input voltage.

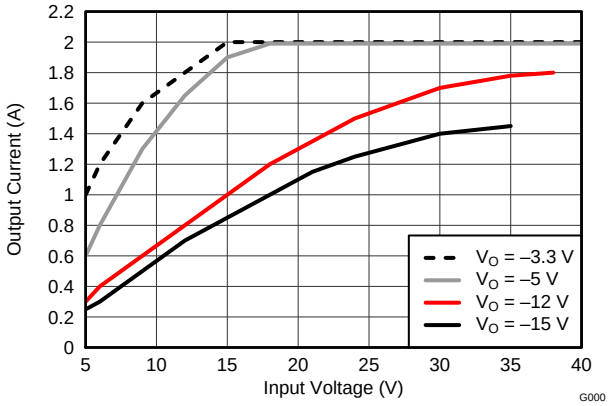


**Figure 33. Safe Operating Current**

## 12.3 Application Schematics

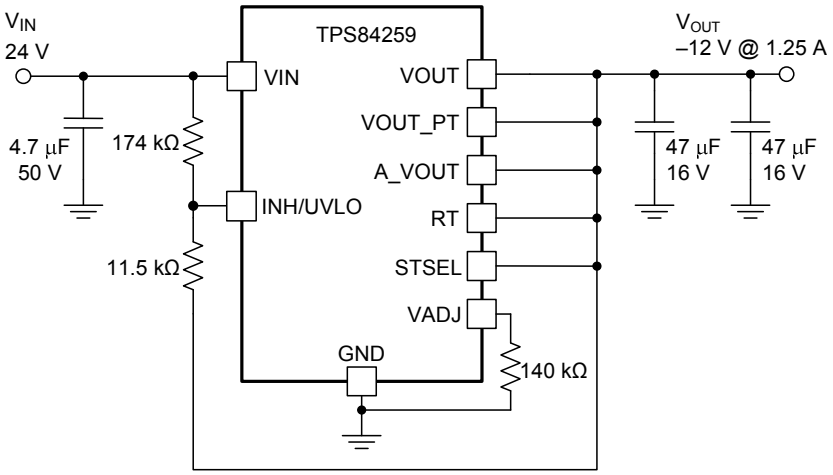


**Figure 34. Typical Schematic**
**$V_{IN}$ = 24 V, $V_{OUT}$ = –12 V**

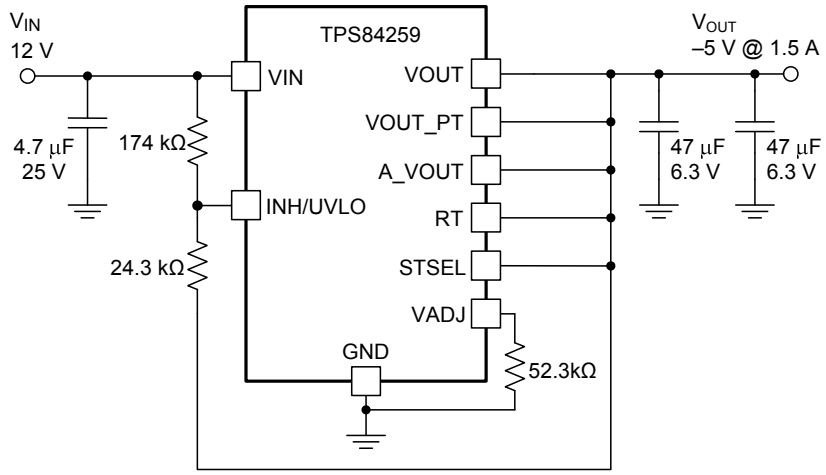


**Figure 35. Typical Schematic**
**$V_{IN}$ = 12 V, $V_{OUT}$ = –5 V**


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## 12.4 Input Voltage

The TPS84259 operates over the input voltage range of 4.5 V to 40 V. The maximum input voltage is 40 V, however, the sum of $V_{IN}$ + $|V_{OUT}|$ must not exceed 50 V.

See the Undervoltage Lockout (UVLO) Threshold section of this datasheet for more information.

## 12.5 Undervoltage Lockout (UVLO) Threshold

At turn-on, the $V_{ON}$ UVLO threshold determines the input voltage level where the device begins power conversion. $R_{UVLO1}$ and $R_{UVLO2}$ set the turn-on threshold as shown in Figure 36. The UVLO threshold is not present during the power-down sequence. Applications requiring a turn-off threshold must monitor the input voltage with external circuitry and shut-down using the INH control (see Output On/Off Inhibit (INH)).

The $V_{ON}$ UVLO threshold must be set to at least 4.5 V to insure proper start-up and reduce current surges on the host input supply as the voltage rises. If possible, it is recommended to set the UVLO threshold to appproximantely 80 to 85% of the minimum expected input voltage.

Use Equation 2 and Equation 3 to calculate the values of $R_{UVLO1}$ and $R_{UVLO2}$. $V_{ON}$ is the voltage threshold during power-up when the input voltage is rising. Table 6 lists standard resistor values for $R_{UVLO1}$ and $R_{UVLO2}$ for adjusting the $V_{ON}$ UVLO threshold for several input voltages.

$$R_{UVLO1} = \frac{0.5}{2.9 \times 10^{-3}} \left(k\Omega\right) \tag{2}$$

$$R_{UVLO2} = \frac{1.25}{\left(\frac{\left(V_{ON} - 1.25\right)}{R_{UVLO1}}\right) + 0.9 \times 10^{-3}} \left(k\Omega\right) \tag{3}$$

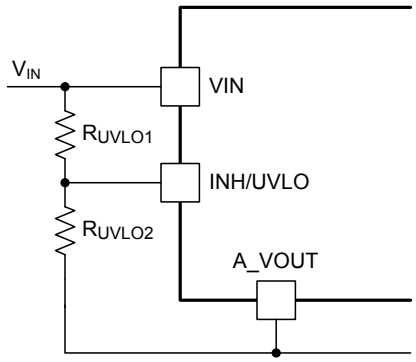


**Figure 36. Adjustable VIN UVLO**

**Table 6. Standard Resistor Values to set $V_{ON}$ UVLO Threshold**

| $V_{ON}$ THRESHOLD (V) | 4.5 | 5.0 | 6.5 | 8.0 | 9.0 | 10.0 | 15.0 | 20.0 | 30.0 |
|---|---|---|---|---|---|---|---|---|---|
| $R_{UVLO1}$ (kΩ) | 174 | 174 | 174 | 174 | 174 | 174 | 174 | 174 | 174 |
| $R_{UVLO2}$ (kΩ) | 63.4 | 56.2 | 40.2 | 31.6 | 27.4 | 24.3 | 15.8 | 11.5 | 7.50 |

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## 12.6 Power-Up Characteristics

When configured as shown in the application schematics, the TPS84259 produces a regulated output voltage following the application of a valid input voltage. During the power-up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay from the point that a valid input voltage is recognized. Figure 37 shows the start-up waveforms for a TPS84259, operating from a 12 V input and the output voltage adjusted to –5 V. The waveform were measured with a 1.5-A constant current load.

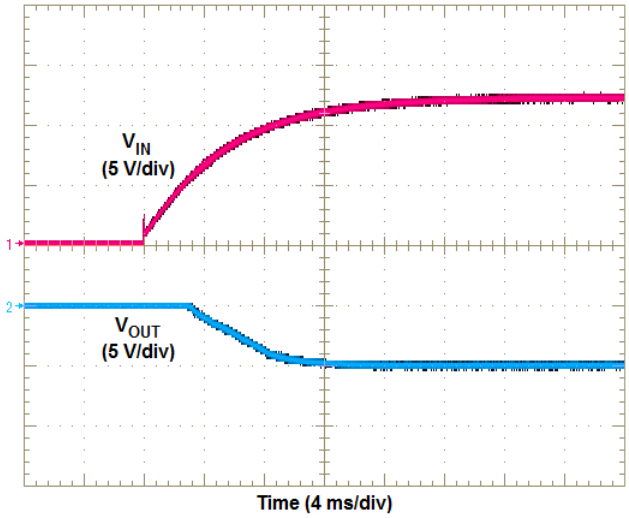


**Figure 37. Start-Up Sequence**

## 12.7 Light-Load Behavior

The TPS84259 is a non-synchronous converter. One of the characteristics of non-synchronous operation is that as the output load current decreases, a point is reached where the energy delivered by a single switching pulse is more than the load can absorb. This energy causes the output voltage to rise slightly. This rise in output voltage is sensed by the feedback loop and the device responds by skipping one or more switching cycles until the output voltages falls back to the set point. At very light loads or no load, many switching cycles are skipped. The observed effect during this pulse skipping mode of operation is an increase in the peak to peak ripple voltage, and a decrease in the ripple frequency. The amount of load current when pulse skipping begins is a function of the input voltage, the output voltage, and the switching frequency.

## 12.8 No-Load Operation

When operating at no load or very light load and the input voltage is removed, the output voltage discharges very slowly. If the input voltage is re-applied before the output voltage discharges, the slow-start circuit does not activate and the amount of inrush current is extremely large and may cause an over-current condition. To avoid this condition the output voltage must be allowed to discharge before re-applying the input voltage. Applying a 50-mA to 100-mA minimum load helps discharge the output voltage. Additionally, monitoring the input voltage with a supervisor and shuting-down using the INH control (see Output On/Off Inhibit (INH)) activates the internal slow-start circuit.


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## 12.9 Switching Frequency

The recommended switching frequency of the TPS84259 is 800 kHz. To operate at the recommended switching frequency, connect the RT pin (Pin 30) to A_VOUT (at pin 32).

It is recommended to adjust the switching frequency in applications with both, higher input voltage (> 18V) and lower output voltage (< –8V). For these applications, improved operating performance can be obtained by decreasing the operating frequency to 500 kHz by adding a resistor, $R_{RT}$ of 93.1 kΩ between the RT pin and A_VOUT as shown in Figure 38. Figure 39 shows the recommended switching frequency over input voltage and output voltage.

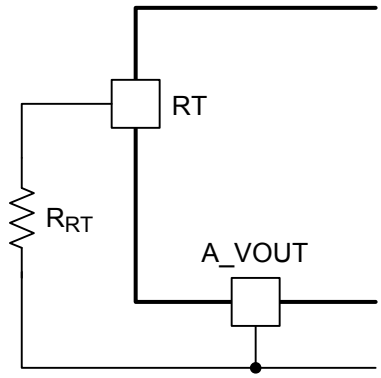


**Figure 38. $R_{RT}$ Resistor Placement**

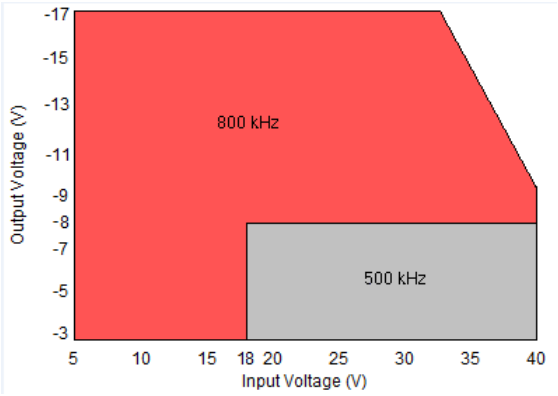


**Figure 39. Recommended Switching Frequency**

**Table 7. Standard Resistor Values For Setting Switching Frequency**

| $f_{SW}$ (kHz) | 500 | 800 |
|---|---|---|
| $R_{RT}$(kΩ) | 93.1 | 0 (short) |

## 12.10 Synchronization (CLK)

An internal phase locked loop (PLL) allows synchronization from 700 kHz to 900 kHz for 800 kHz applications, or 400 kHz to 600 kHz for 500 kHz applications. See Figure 39 to determine switching frequency based on input voltage and output voltage. To implement the synchronization feature, connect a square wave clock signal to the RT/CLK pin with a duty cycle between 25% to 75%. The clock signal amplitude must transition lower than 0.5 V and higher than 2.2 V. The start of the switching cycle is synchronized to the falling edge of RT/CLK pin. In applications requiring CLK mode, configure the device as shown in Figure 40 (800 kHz) and Figure 41 (500kHz).

Before the external clock is present, the device works in RT mode where the switching frequency is set by the $R_{RT}$ resistor. When the external clock is present, the CLK mode overrides the RT mode. The first time the CLK pin is pulled above the RT/CLK high threshold (2.2 V), the device switches from RT mode to CLK mode and the CLK pin becomes high impedance as the PLL starts to lock onto the frequency of the external clock. It is not recommended to switch from CLK mode back to RT mode because the internal switching frequency drops to 100 kHz first before returning to the switching frequency set by the RT resistor.

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## Synchronization (CLK) (continued)

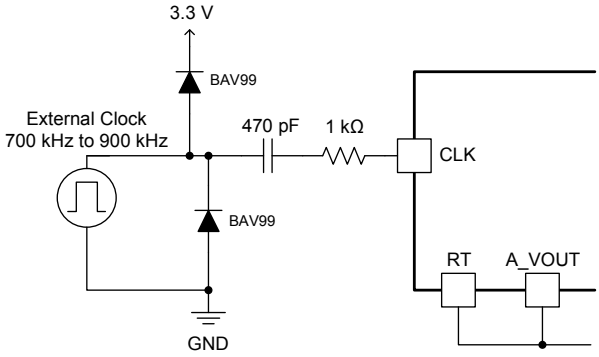


**Figure 40. CLK Configuration (800 kHz Typ)**

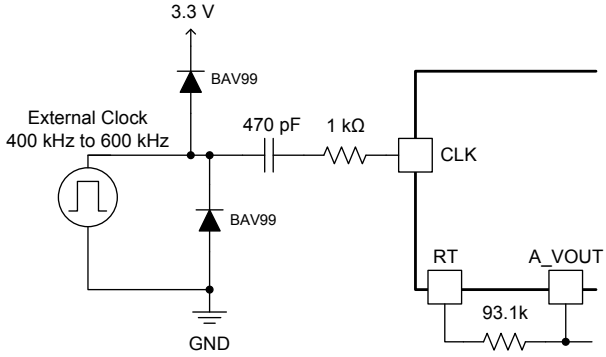


**Figure 41. CLK Configuration (500 kHz Typ)**


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## 12.11 Output On/Off Inhibit (INH)

The INH pin provides electrical on/off control of the device. Once the INH pin voltage exceeds the threshold voltage, the device starts operation. If the INH pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The INH pin has an internal pull-up current source, allowing the user to float the INH pin for enabling the device. If an application requires controlling the INH pin, an external level-shifter is required to interface with the pin because in a positive-to-negative buck-boost supply, the INH pin is referenced to VOUT, not GND. Adding a level-shifter (U1) as shown in Figure 42, allows the INH control to be refernced to GND. A recommended level-shifter part # is DCX144EH-7 from Diodes Inc.

Pulling the input of U1 to GND applies a low voltage to the inhibit control pin and disables the output of the supply, shown in . Releasing the input of U1 enables the device, which executes a soft-start power-up sequence, as shown in Figure 44. The device produces a regulated output vFigure 43oltage within 10 ms. The waveforms were measured with a 1.5-A constant current load.

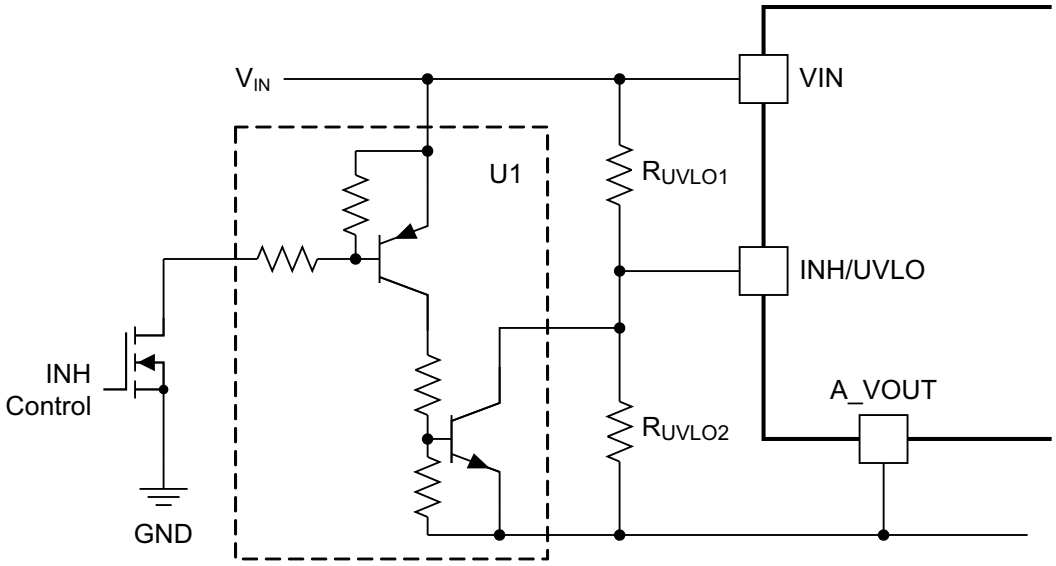


**Figure 42. Typical Inhibit Control**

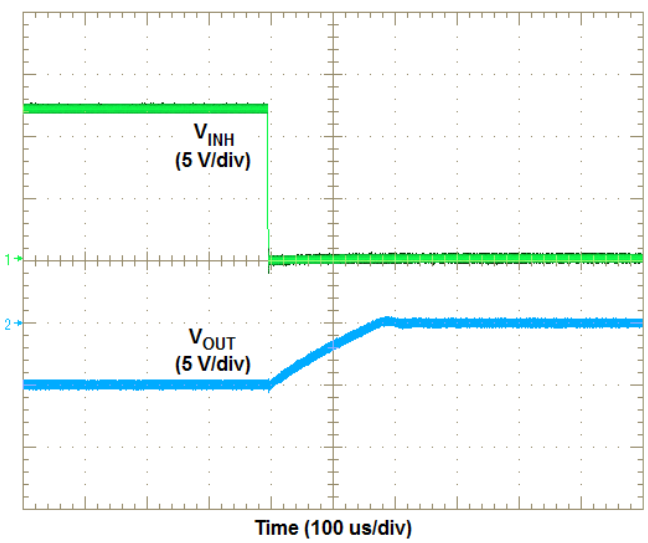


**Figure 43. Inhibit Turn-Off**

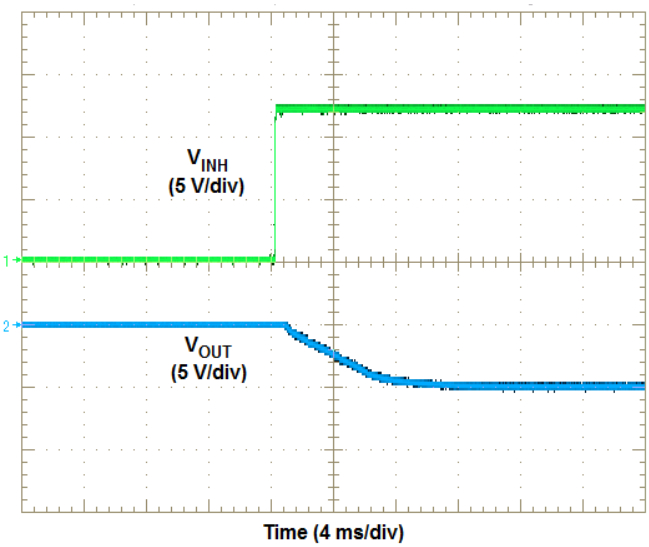


**Figure 44. Inhibit Turn-On**

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## 12.12 Slow-Start Circuit (SS)

Connecting the STSEL pin (Pin 29) to A_VOUT while leaving SS pin (Pin 28) open, enables the internal SS capacitor with a slow-start interval of approximately 10 ms. Adding additional capacitance between the SS pin and A_VOUT increases the slow-start time. Figure 45 shows an additional SS capacitor connected to the SS pin and the STSEL pin connected to A_VOUT. See Table 8 below for SS capacitor values and timing interval.

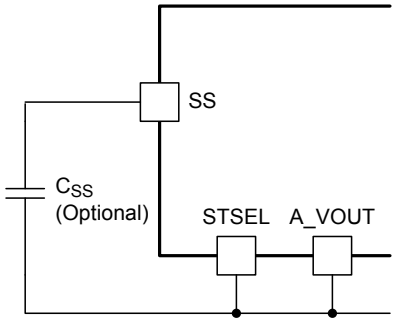


**Figure 45. Slow-Start Capacitor ($C_{SS}$) and STSEL Connection**

**Table 8. Slow-Start Capacitor Values and Slow-Start Time**

| $C_{SS}$ (nF) | Open | 10 | 15 | 22 |
|---|---|---|---|---|
| SS Time (ms) | 10 | 15 | 17 | 20 |

## 12.13 Inrush Current

During turn-on, as the TPS84259 performs a slow-start sequence, an inrush current is induced as the output capacitors charge up. The inrush current is in addition to the DC input current. The amount of inrush current depends on the input voltage, output voltage and amount of output capacitance. Table 9 shows the typical inrush current for the input voltage, output voltage and the amount of output capacitance. Increasing the slow-start capacitor reduces the inrush current by slowing down the ramp of the output voltage. See Slow-Start Circuit (SS).

**Table 9. Typical Inrush Current**

| Output Capacitance → | | 100 µF Ceramic | 200 µF (1) | 320 µF (1) | 430 µF (1) |
|---|---|---|---|---|---|
| VIN (V) | VOUT (V) | Inrush Current (A) | | | |
| 5 | –3.3 | 0.1 | 0.1 | 0.1 | 0.1 |
| | –5 | 0.1 | 0.2 | 0.2 | 0.3 |
| | –12 | 0.3 | 0.8 | 1.2 | 1.8 |
| | –15 | 0.4 | 1.3 | 2.5 | 3.6 |
| 12 | –3.3 | 0.1 | 0.1 | 0.1 | 0.1 |
| | –5 | 0.1 | 0.1 | 0.1 | 0.2 |
| | –12 | 0.2 | 0.4 | 0.6 | 0.8 |
| | –15 | 0.3 | 0.5 | 0.9 | 1.3 |
| 24 | –3.3 | 0.1 | 0.1 | 0.1 | 0.1 |
| | –5 | 0.1 | 0.1 | 0.2 | 0.2 |
| | –12 | 0.2 | 0.2 | 0.3 | 0.5 |
| | –15 | 0.3 | 0.3 | 0.5 | 0.7 |
| 36 | –3.3 | 0.2 | 0.2 | 0.2 | 0.2 |
| | –5 | 0.2 | 0.2 | 0.2 | 0.2 |
| | –12 | 0.2 | 0.3 | 0.4 | 0.4 |

(1) This amount of capacitance includes the required 100 µF of ceramic capacitance with additional bulk capacitance.


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## 12.14 Input to Output Coupling Capacitor

Adding an input to output coupling capacitor ($C_{IO}$) across VIN to VOUT as shown in Figure 46 can help reduce output voltage ripple and improve transient response. A typical value for $C_{IO}$ is 2.2 µF ceramic with a voltage rating greater than the sum of VIN + |VOUT|.

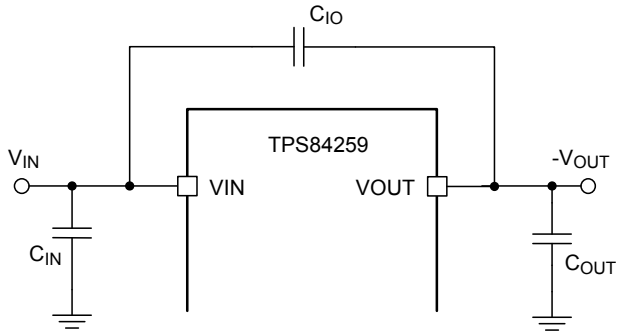


**Figure 46. Input to Output Coupling Capacitor**

## 12.15 Overcurrent Protection

For protection against load faults, the TPS84259 incorporates cycle-by-cycle current limiting. During an overcurrent condition the output current is limited and the output voltage is reduced. If the output voltage drops more than 25%, the switching frequency is lowered to reduce power dissipation within the device. When the overcurrent condition is removed, the output voltage returns to the established voltage.

The TPS84259 is not designed to endure a sustained short circuit condition. The use of an output fuse, voltage supervisor circuit, or other overcurrent protection circuit is recommended.

## 12.16 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 180°C typically. The device reinitiates the power up sequence when the junction temperature drops below 165°C typically.

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## 12.17 Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 47 through Figure 50 show a typical four layer PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and GND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Place a dedicated A_VOUT copper area beneath the TPS84259.
- Isolate the PH copper area from the GND copper area using the VOUT copper area.
- Connect the VOUT and A_VOUT copper areas at one point; at pins 8 & 9.
- Place $R_{SET}$, $R_{RT}$, and $C_{SS}$ as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.
- Use a dedicated sense line to connect $R_{SET}$ to GND near the load for best regulation.

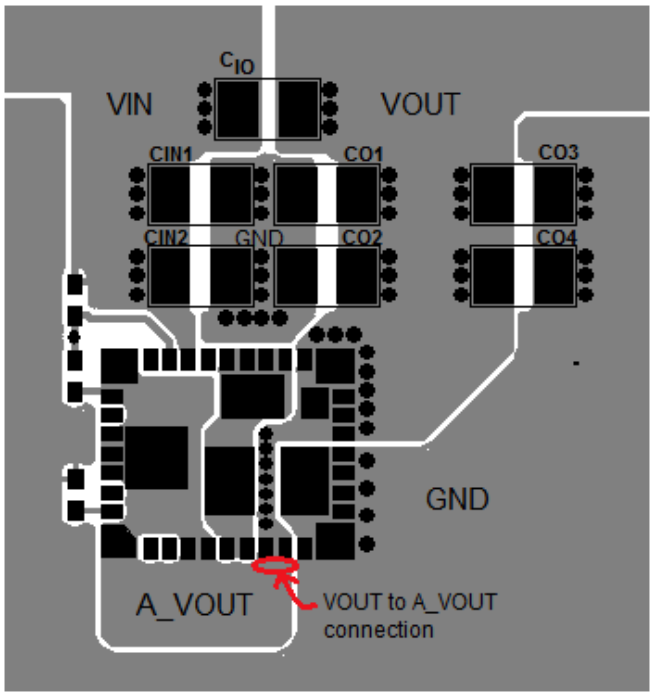


**Figure 47. Typical Top-Layer Recommended Layout**

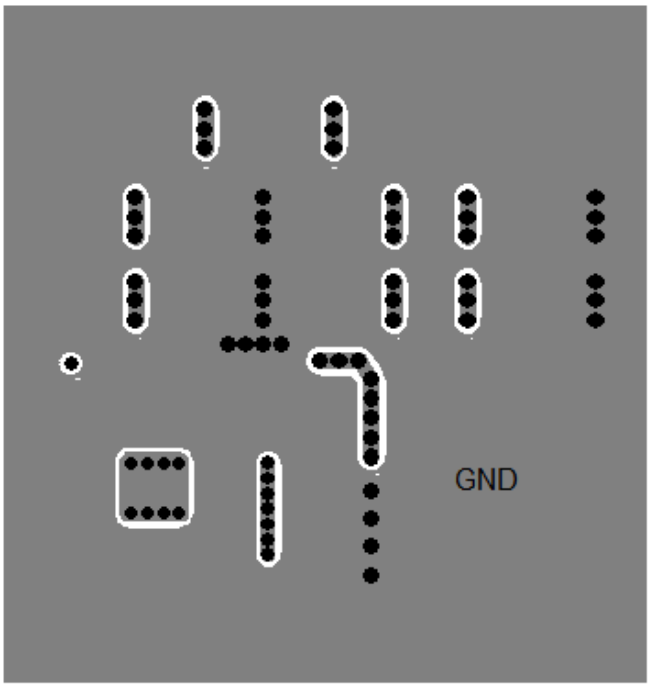


**Figure 48. Typical GND-Layer Recommended Layout**


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## Layout Considerations (continued)

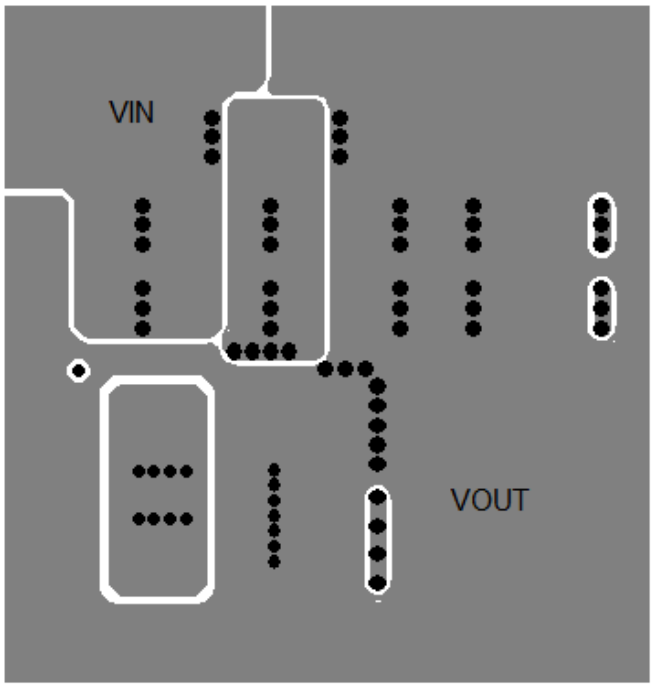


**Figure 49. Typical VOUT-Layer Recommended Layout**

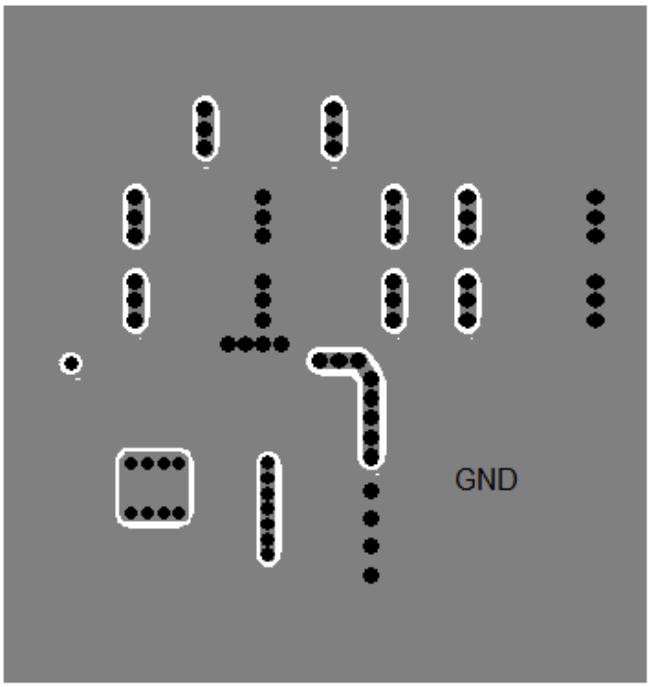


**Figure 50. Typical Bottom-Layer Recommended Layout**

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# 13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (June 2017) to Revision D** **Page**

- Added top navigator icon for TI reference design ..... 1
- Increased the peak reflow temperature and maximum number of reflows to JEDEC specification for improved manufacturability. ..... 2

**Changes from Revision B (September 2013) to Revision C** **Page**

- Added peak reflow and maximum number of reflows information ..... 2

**Changes from Revision A (June 2013) to Revision B** **Page**

- Changed incorrect $R_{SET}$ value for -5.5 $V_{OUT}$ in Table 5. ..... 15
- Added *Mechanical, Packaging, and Orderable Information* section..... 27

**Changes from Original (August 2012) to Revision A** **Page**

- Changed describing pins 8 & 9 not connected together internally. ..... 6
- Added multiple layout layers to the recommended layout. ..... 24


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# 14 Device and Documentation Support

## 14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 14.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 14.3 Trademarks

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## 14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 14.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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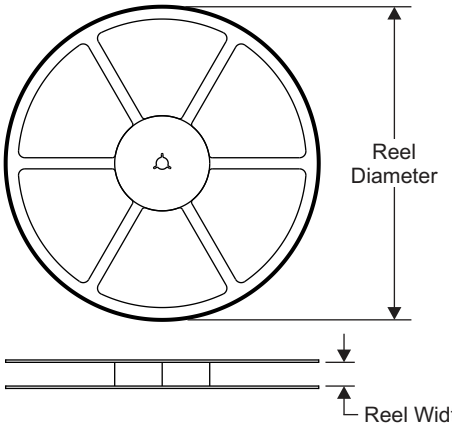
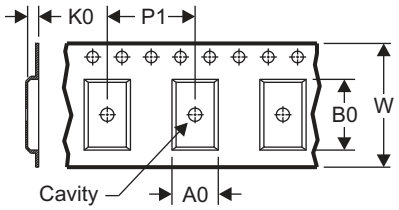
## 15.1 Tape and Reel Information

**REEL DIMENSIONS**

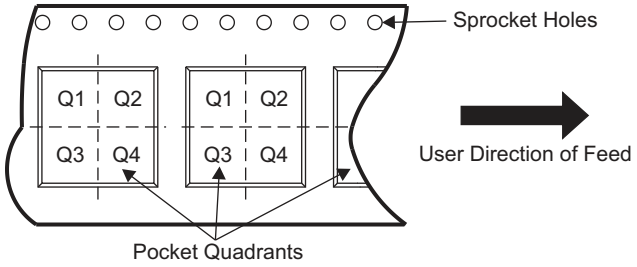



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS84259RKGR | B1QFN | RKG | 41 | 500 | 330.0 | 24.4 | 9.35 | 11.35 | 3.1 | 16.0 | 24.0 | Q1 |
| TPS84259RKGT | B1QFN | RKG | 41 | 250 | 330.0 | 24.4 | 9.35 | 11.35 | 3.1 | 16.0 | 24.0 | Q1 |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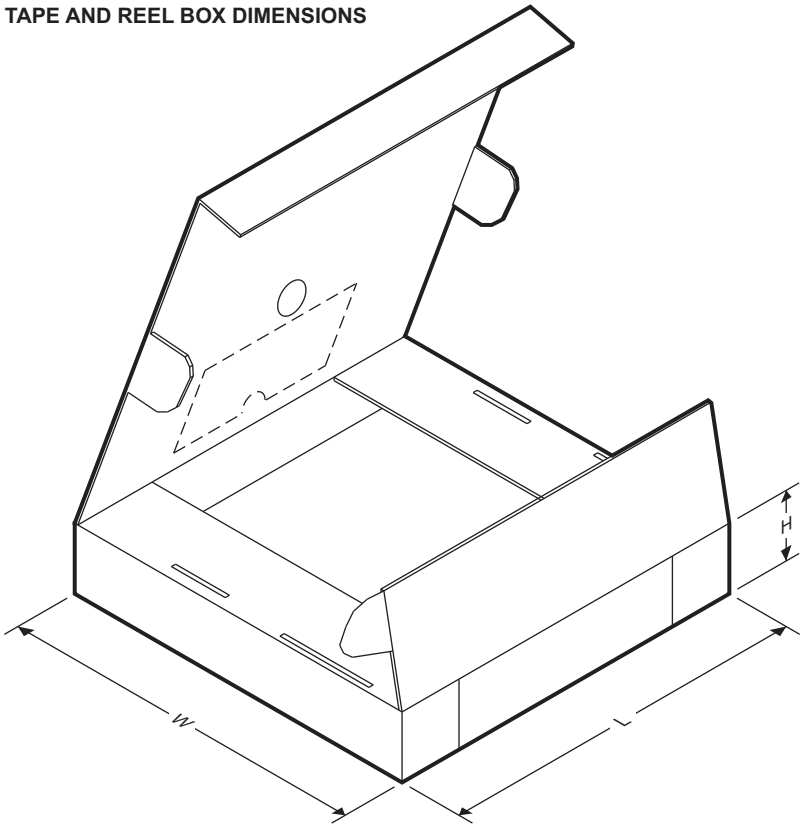
**TAPE AND REEL BOX DIMENSIONS**




| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS84259RKGR | B1QFN | RKG | 41 | 500 | 383.0 | 353.0 | 58.0 |
| TPS84259RKGT | B1QFN | RKG | 41 | 250 | 383.0 | 353.0 | 58.0 |

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS84259RKGR | ACTIVE | B1QFN | RKG | 41 | 500 | RoHS Exempt & Green | NIPDAU | Level-3-250C-168 HR | -40 to 85 | (54260, TPS84259) | Samples |
| TPS84259RKGT | ACTIVE | B1QFN | RKG | 41 | 250 | RoHS Exempt & Green | NIPDAU | Level-3-250C-168 HR | -40 to 85 | (54260, TPS84259) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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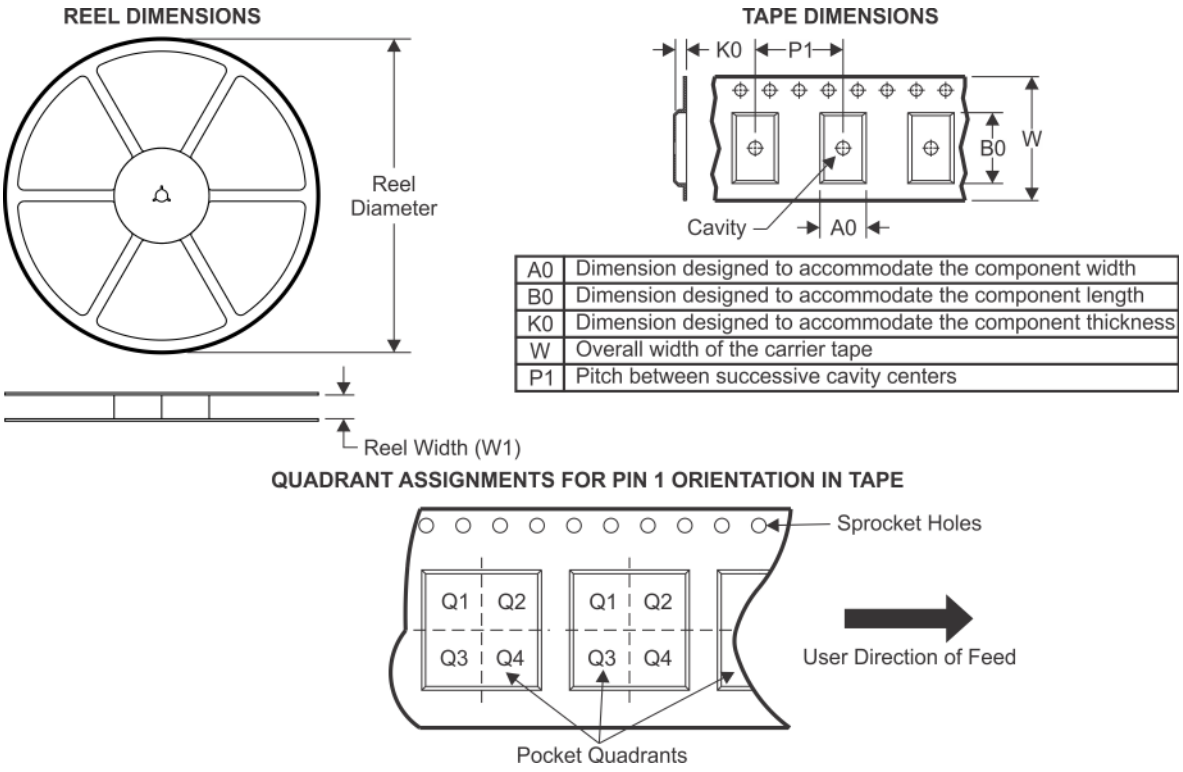
## TAPE AND REEL INFORMATION




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
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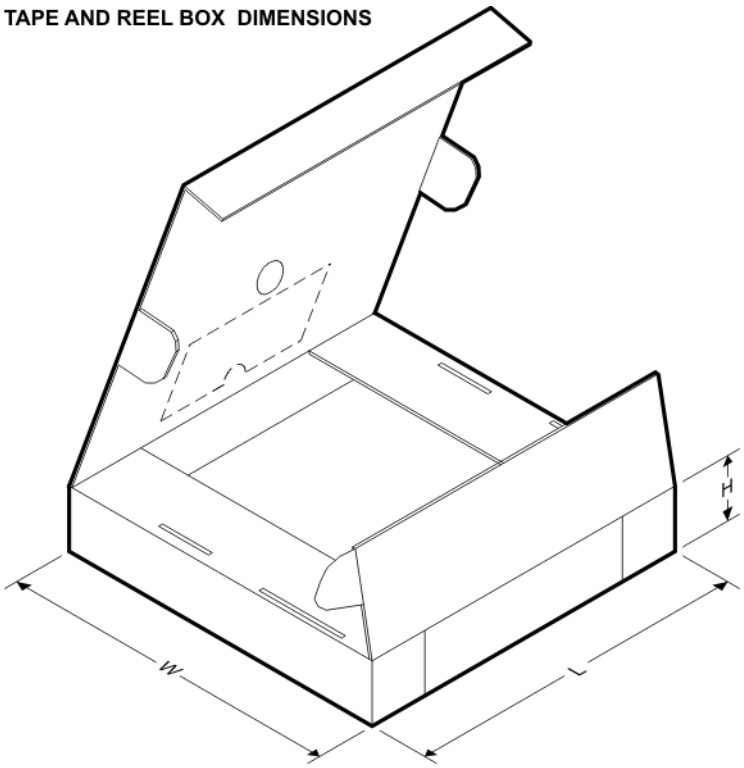
| TPS84259RKGT | B1QFN | RKG | 41 | 250 | 330.0 | 24.4 | 9.35 | 11.35 | 3.1 | 16.0 | 24.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

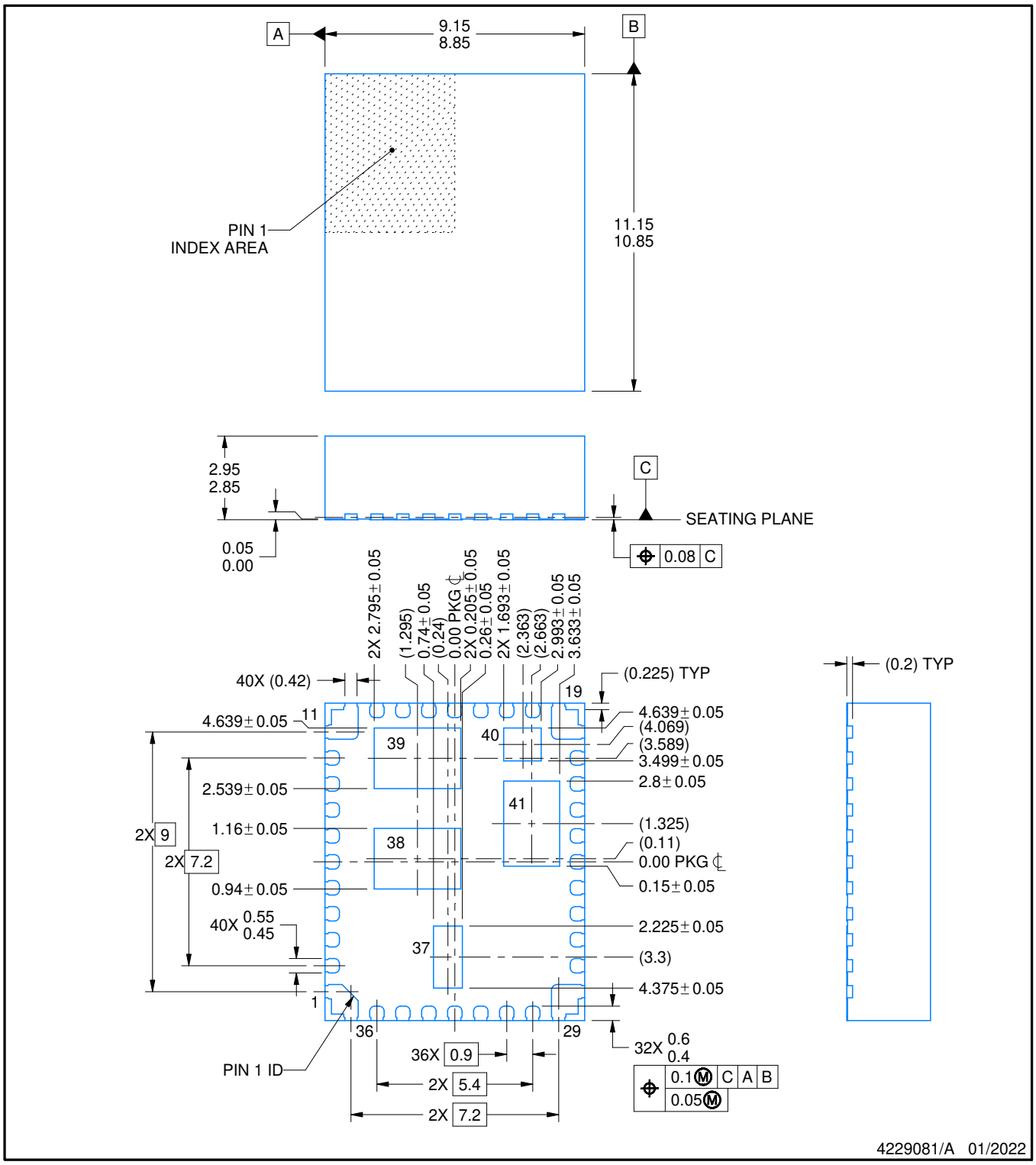
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS84259RKGR | B1QFN | RKG | 41 | 500 | 383.0 | 353.0 | 58.0 |
| TPS84259RKGT | B1QFN | RKG | 41 | 250 | 383.0 | 353.0 | 58.0 |

# RKG0041A

# PACKAGE OUTLINE

## B1QFN - 2.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

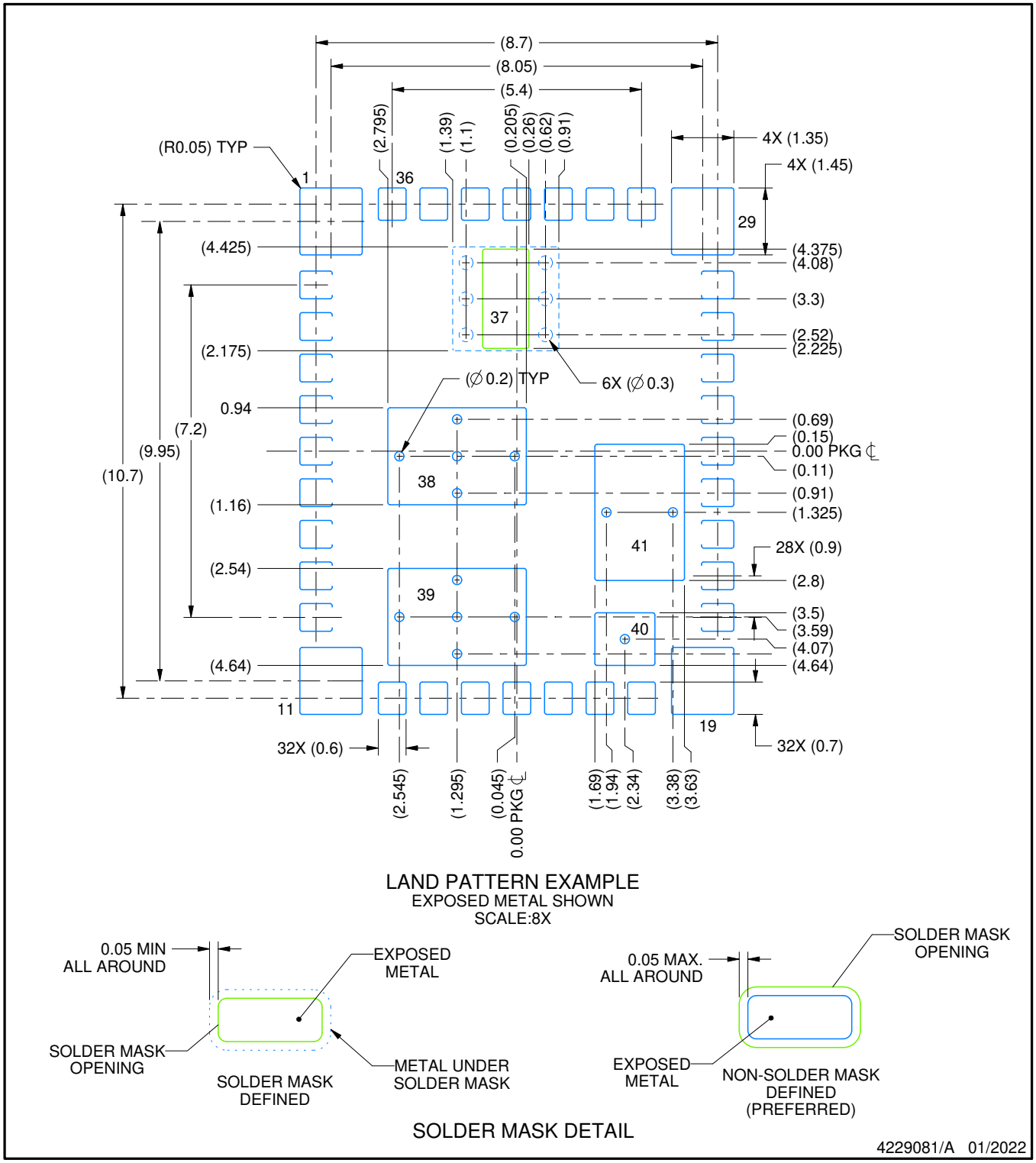
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

## RKG0041A

## B1QFN - 2.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

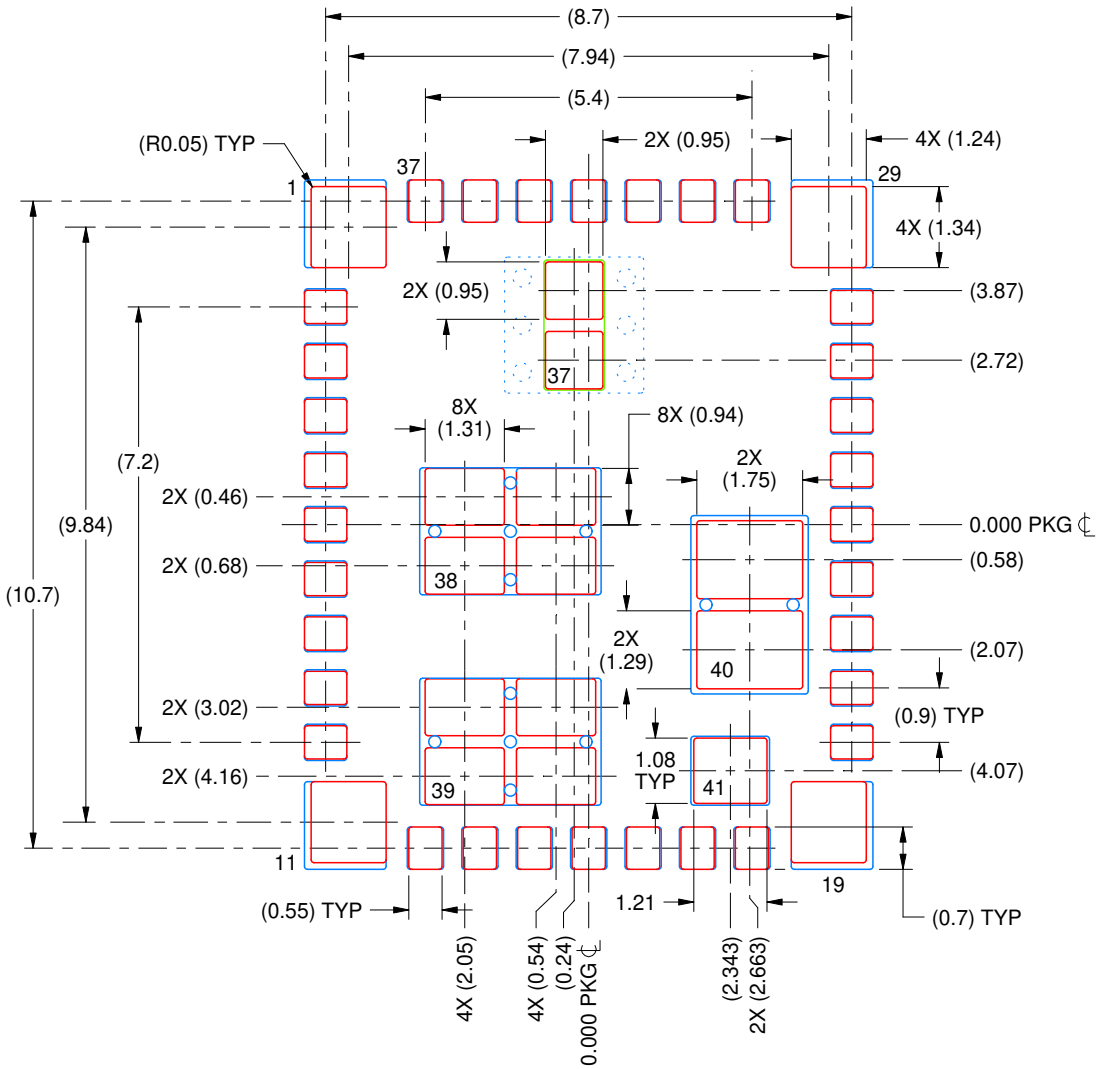



SOLDER MASK DETAIL

4229081/A 01/2022

NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE

BASED ON 0.1 mm STENCIL THICKNESS

4229081/A 01/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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