



# Micropower Secondary Regulation IC

## ISDN I.430 RELATED FEATURES

- Secondary-Side Voltage Sense for Improved Regulation
- Restricted Mode Status Output
- Precision Programmable Quiescent Current
- Very Low Quiescent Power for CCITT 25mW Restricted Mode

## GENERAL FEATURES

- Wide Supply Voltage Range
- Precision 2.0V Reference
- Low Offset, High Gain Error Amplifier
- Temperature Stable Oscillator
- Logic Level Oscillator Synchronization
- Low Line Status Output
- Under Voltage Lockout
- Programmable Secondary-Side Soft Start
- 5V V<sub>DD</sub> Logic Supply Regulator

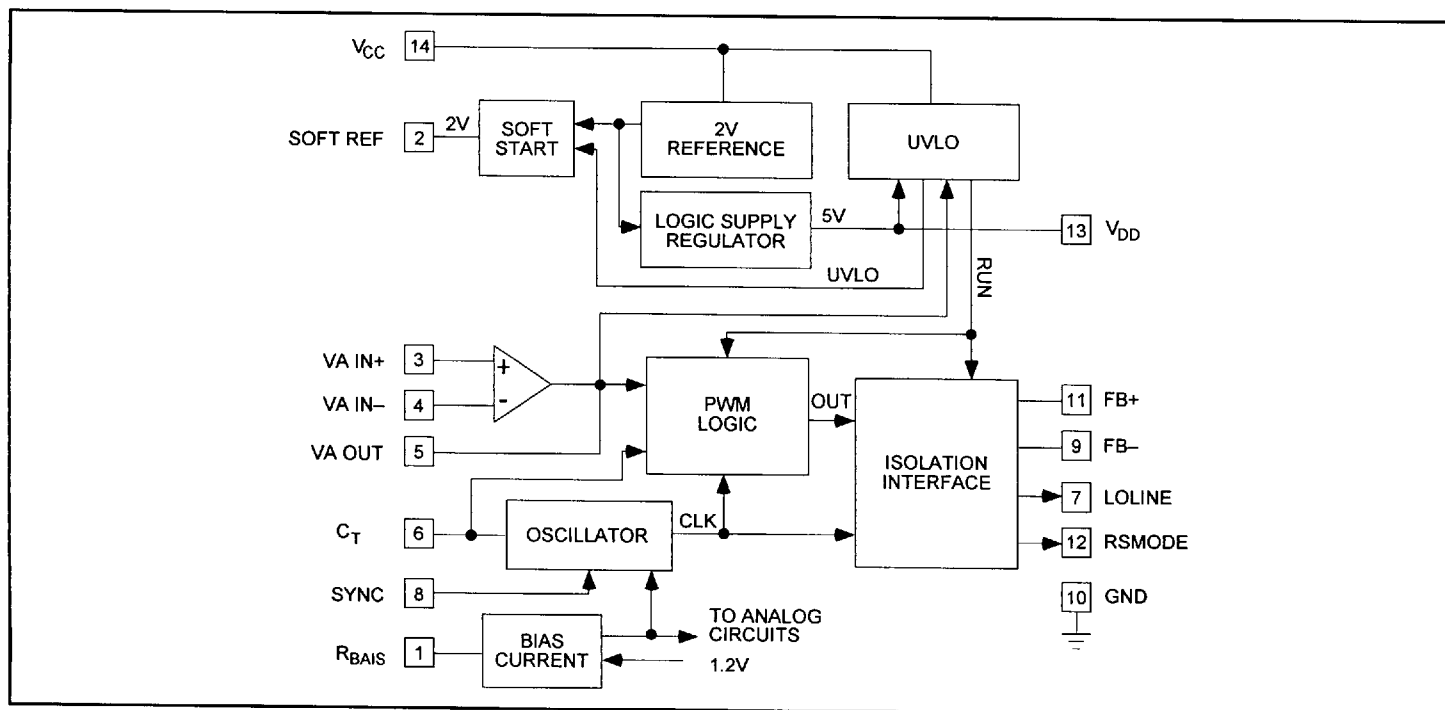
## DESCRIPTION

The UCC1885 supplies the necessary functions to implement a fully isolated, ISDN compatible SMPS meeting the guidelines of CCITT recommendation I.430, when used in conjunction with the UCC1883 primary-side PWM controller. The UCC1885 secondary-side regulation IC provides improved regulation by allowing direct sensing of the output voltage on the secondary side of the DC/DC converter. The UCC1885 contains a precision system reference and a complete error amplifier. The output of the amplifier serves as the PWM control voltage and is provided to the primary-side via an isolation pulse transformer. The UCC1885 also sends synchronization information to the primary-side with this transformer. Under voltage lockout circuitry operates in combination with the user programmable soft start function to prevent transmission of data across the isolation barrier until adequate secondary-side operating conditions are established.

ISDN specific features allow the UCC1883/UCC1885 combination to be compatible with CCITT recommendation I.430. The UCC1885 receives two digital bits of status information from the UCC1883 via the isolation pulse transformer. These bits, which indicate restricted power mode and low input line voltage, are output on the secondary-side at CMOS logic levels. Precision programming of the quiescent current used by the UCC1885 allows the system to meet the 25mW restricted mode power limit, or the current can be set to achieve higher operating frequencies at the cost of increased power consumption.

The UCC1885 is fabricated in Unitrode's 3 $\mu$ m BiCMOS process. Even though the device contains internal clamping diodes on all pins, the part should still be considered static sensitive. Normal ESD handling procedures for CMOS devices should be observed when using the UCC1885.

## BLOCK DIAGRAM

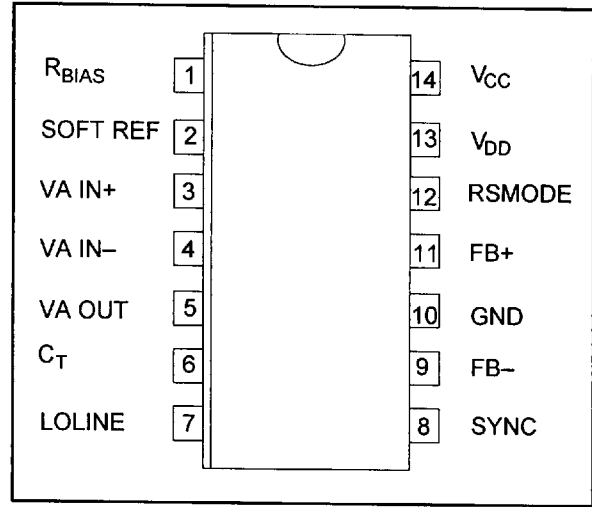


**ABSOLUTE MAXIMUM RATINGS**

Analog Supply Voltage ( $V_{CC}$ ) ..... 18V  
 Maximum  $V_{CC}$  Slew Rate ..... 3V/mS  
 Digital Supply Voltage ( $V_{DD}$ ) ..... 7V  
 Maximum Voltage, All Signal Pins .....  $V_{DD} + 0.3V$  to 7V  
 Minimum Voltage, All Pins ..... - 0.3V  
 Maximum DC Current, Any Pin, Source or Sink ..... 100mA  
 Maximum Peak Current, Any Pin, Source or Sink .... 500mA  
 Total Package Dissipation (N package) ..... 1W  
 Total Package Dissipation (D package) ..... 800mW  
 Storage Temperature ..... - 65°C to +150°C  
 Lead Temperature (Soldering, 10 seconds)..... +300°C

**CONNECTION DIAGRAM**

DIL-14, J or N Package, SOIC-14, D-Package



- Note 1:** All voltages expressed with respect to pin 10, currents are positive into the specified terminal.
- Note 2:** All maximum signal pin voltage limits apply for cases of zero source impedance. Higher or lower voltages may be impressed through a finite source impedance which causes the input current to be limited to the values specified, with total package power dissipation at or below specified limits.
- Note 3:** Consult Packaging Section of Databook for thermal limitations and considerations of package.

Pin Number	Pin Name	Pin Type	Function
1	$R_{BIAS}$	Analog Program	Quiescent Bias Current Set
2	SOFTREF	Analog Program & Output	Soft Start Timing Set and 2.0V Reference Output
3	VA IN +	Analog Input	Voltage Error Amplifier Non-Inverting Input
4	VA IN -	Analog Input	Voltage Error Amplifier Inverting Input
5	VA OUT	Analog Output	Voltage Error Amplifier Output
6	$C_T$	Analog Program	Oscillator Frequency Set
7	LOLINE	Digital Output	Low Primary-Side Line Voltage Status Bit (High = True)
8	SYNC	Digital Input	Oscillator SYNC (Positive-Edge Triggered)
9	FB -	Digital I/O	Differential Feedback Communication Signal (-)
10	GND	Supply Return	System Ground
11	FB +	Digital I/O	Differential Feedback Communication Signal (+)
12	RSMODE	Digital Output	CCITT Restricted Power Mode Status Bit (High = True)
13	$V_{DD}$	Logic Supply	5.0V Internal Regulator Output or Logic Supply Input
14	$V_{CC}$	Power Supply	Analog Power Supply Input



**ELECTRICAL CHARACTERISTICS** Unless otherwise noted, all specifications apply for  $T_A$  -55°C to +125°C for the UCC1885; -40°C to +85°C for the UCC2885; 0°C to +70°C for the UCC3885  $V_{CC} = V_{DD} = 5V$ , SYNC = 0V,  $R_{BIAS} = 200Kohms$ ,  $C_t = 100pF$ , and  $T_J = T_A$ (min) to  $T_A$ (max)

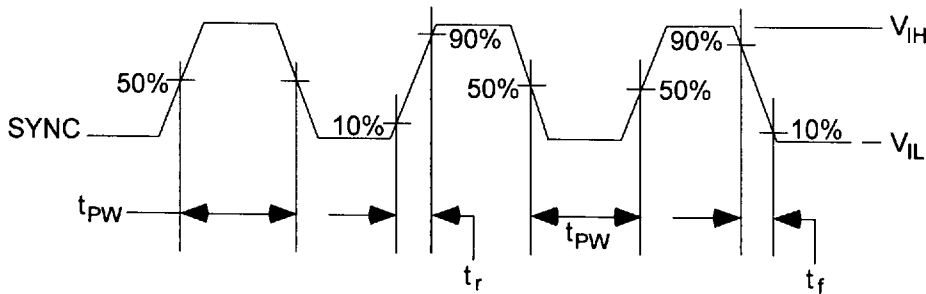
UCC1885  
UCC2885  
UCC3885

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
<b>UVLO Section</b>					
$V_{CC}$ Start Threshold	$V_{DD} = V_{CC}$	2.4	2.7	3.0	V
$V_{CC}$ Threshold Hysteresis	$V_{DD} = V_{CC}$	260	400	600	mV
$V_{DD}$ Start Threshold	$V_{DD} < V_{CC}$	2.0	2.4	2.9	V
VA OUT Run Threshold	VA OUT = VA IN(-)	1.0	1.15	1.3	V
<b>Reference Section</b>					
Reference Voltage	$T_J = 25^\circ C$ , $R_{load} > 50Mohm$	1.98	2	2.02	V
Line Regulation	$3V < V_{CC} < 16.5V$	-	2	10	mV
Load Regulation	$-500nA < I_{out} < 500nA$	-	12	35	mV
Total Reference Variation	Initial + Line + Temperature $R_{load} > 50Mohm$	1.96	-	2.04	V
Soft Start Current	SOFTREF = 0V	4	10	16	uA
External Override Threshold		-	-	2.45	V
Input Bias Current	SOFTREF = 5V	-	-	50	nA
<b>User Bias Section</b>					
$R_{BIAS}$ Voltage	$T_J = 25^\circ C$	1.17	1.2	1.23	V
$R_{BIAS}$ Pin Line Regulation	$3V < V_{CC} < 16.5V$	-	8	30	mV
Total $R_{BIAS}$ Pin Variation	Initial + Line + Temperature	1.15	-	1.25	V
<b>Error Amplifier Section</b>					
Input Common Mode Range	VA OUT = 1V	1	-	4.5	V
Input Offset Voltage	VA IN(+) = 2V, VA OUT = 1V	-8	-	8	mV
Input Bias Current	VA IN(+) = 2V, VA OUT = 1V	-100	-	100	nA
VA OUT Low Level	$V_{dm} = -10mV$ , $I_{out} = 700uA$	-	0.05	0.15	V
VA OUT High Level	$R_{BIAS} = 200K$ , $V_{dm} = 10mV$ , $I_{out} = -50uA$	2.0	2.6	-	V
	$R_{BIAS} = 39.2K$ , $V_{dm} = 10mV$ , $I_{out} = -250uA$	2.0	2.7	-	V
VA OUT Short Circuit Current	VA OUT = 0V, $R_{BIAS} = 39.2 Kohms$	-0.4	-1	-5	mA
Open Loop Voltage Gain	$V_{cm} = 2V$ , $0.1 < VA OUT = < 2.0V$ $R_{BIAS} = 39.2 Kohms$	80	110	-	dB
DC PSRR	$V_{cm} = 2V$ , $0.1 < VA OUT = 1V$ $R_{BIAS} = 39.2K$ , $3V < V_{CC} < 16.5V$	70	110	-	dB
DC CMRR	VA OUT = 1V, $R_{BIAS} = 39.2K$ $1V < V_{cm} < 4V$	70	100	-	dB
Unity Gain Bandwidth	$R_{BIAS} = 200 Kohms$ , $C_{out} = 25pF$ (Note 1)	375	500	-	KHz
	$R_{BIAS} = 39.2 Kohms$ , $C_{out} = 25pF$ (Note 1)	1.6	2.2	-	MHz
Open Loop Output Impedance	$R_{BIAS} = 200K$ (Note 1)	-	2.2	3.3	Kohms
	$R_{BIAS} = 39.2K$ (Note 1)		450	675	ohms
VA OUT Slew Rate	$R_{BIAS} = 200K$ , $C_{out} = 25pF$ (Note 1)	140	250	-	mV/us
	$R_{BIAS} = 39.2K$ , $C_{out} = 25pF$ (Note 1)	0.7	1.25	-	V/us
<b>Oscillator Section</b>					
Initial Accuracy	$T_J = 25^\circ C$	42	48	56	KHz
Voltage Stability	$3V < V_{CC} = V_{DD} < 7V$	-	1	3	%
Total Oscillator Variation	Initial + Line + Temperature	41.5	-	58	KHz
$C_T$ Ramp Amplitude		1.65	1.8	1.9	V
SYNC Input Low Voltage		-	-	1.5	V
SYNC Input High Voltage		3.5	-	-	V

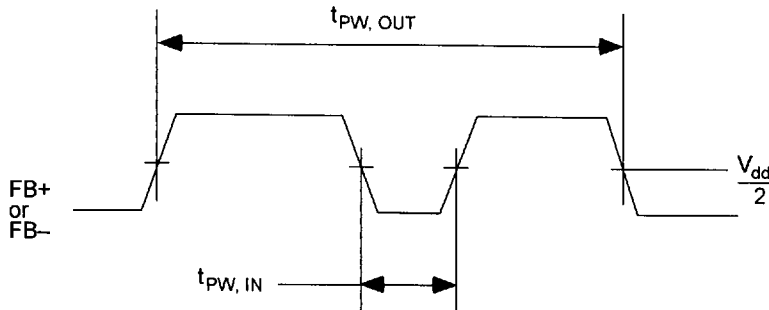
**ELECTRICAL CHARACTERISTICS** : Unless otherwise noted, all specifications apply for  $T_A$  -55°C to +125°C UCC1885  
 for the UCC1885; -40°C to +85°C for the UCC2885; 0°C to +70°C for the UCC3885  $V_{CC} = V_{DD} = 5V$ , SYNC UCC2885  
 $= 0V$ ,  $R_{BIAS} = 200Kohms$ ,  $C_t = 100pF$ , and  $T_J = T_A$ (min) to  $T_A$ (max) UCC3885

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
<b>Oscillator Section (Continued)</b>					
Maximum SYNC Rise, Fall Time	(See Figure 1 and Note 1)	500	–	–	nS
Minimum SYNC Pulse Width	(See Figure 1 and Note 1)	10	15	nS	
<b>Isolation Interface Section</b>					
FB Output High Voltage	$R_{load} = 500\text{ ohms}$	4.0	4.5	–	V
FB Output Low Voltage	$R_{load} = 50\text{ ohms to }5V$	–	0.5	0.85	V
FB Output Pulse Width	$R_{BIAS} = 200\text{ Kohms}$ (See Figure 2)	200	300	450	ns
	$R_{BIAS} = 39.2\text{ Kohms}$ (See Figure 2)	–	100	–	ns
FB Output PW Matching		–	15	–	ns
Minimum FB Input Pulse Width	(See Figure 2 and Note 1)	–	10	–	ns
Digital Status Output High	LOLINE, RSMODE, $I_{out} = -200\mu A$	4.85	4.95	–	V
Digital Status Output Low	LOLINE, RSMODE, $I_{out} = 800\mu A$	–	0.3	0.45	V
<b><math>V_{DD}</math> Regulator</b>					
$V_{DD}$ Output Voltage	$V_{DD} < V_{CC}$ , No External Load	4.75	5	5.25	V
$V_{DD}$ Line Regulation	$7V < V_{CC} < 16.5V$	–	10	50	mV
$V_{DD}$ Load Regulation	$-3mA < I_{out} < 0mA$	–	100	250	mV
$V_{DD}$ Regulator Dropout	No External Load	–	0.9	1.7	V
$V_{DD}$ Short Circuit Current	$V_{DD} = 0V$	8	30	70	mA
<b>Power Supplies</b>					
DC Supply Current		–	100	150	uA
Cpd	(Note 2)	–	150	–	pF

- Notes:** 1. This parameter not 100% tested in production, but guaranteed by design.  
 2. Total power dissipation will be determined by associated isolation pulse transformer characteristics. A pulse transformer with a low loss core and at least 50µH of magnetizing inductance is strongly recommended.



OSCILLATOR SYNC TIMING  
**FIGURE 1**



FEEDBACK I/O TIMING  
**FIGURE 2**

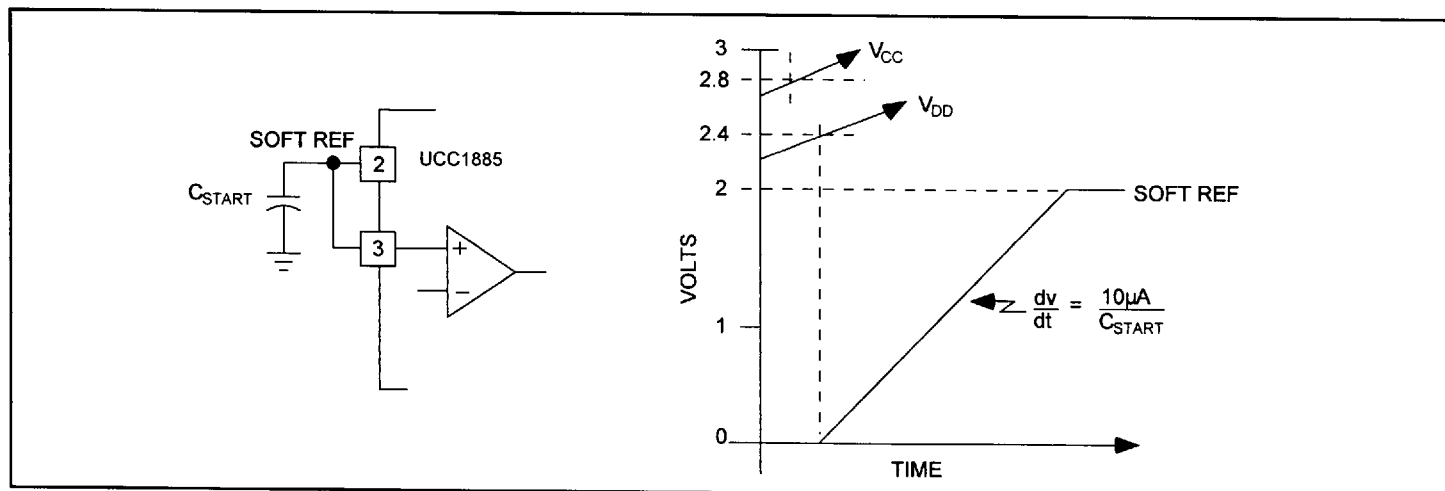
## APPLICATIONS INFORMATION

### UNDER VOLTAGE LOCKOUT

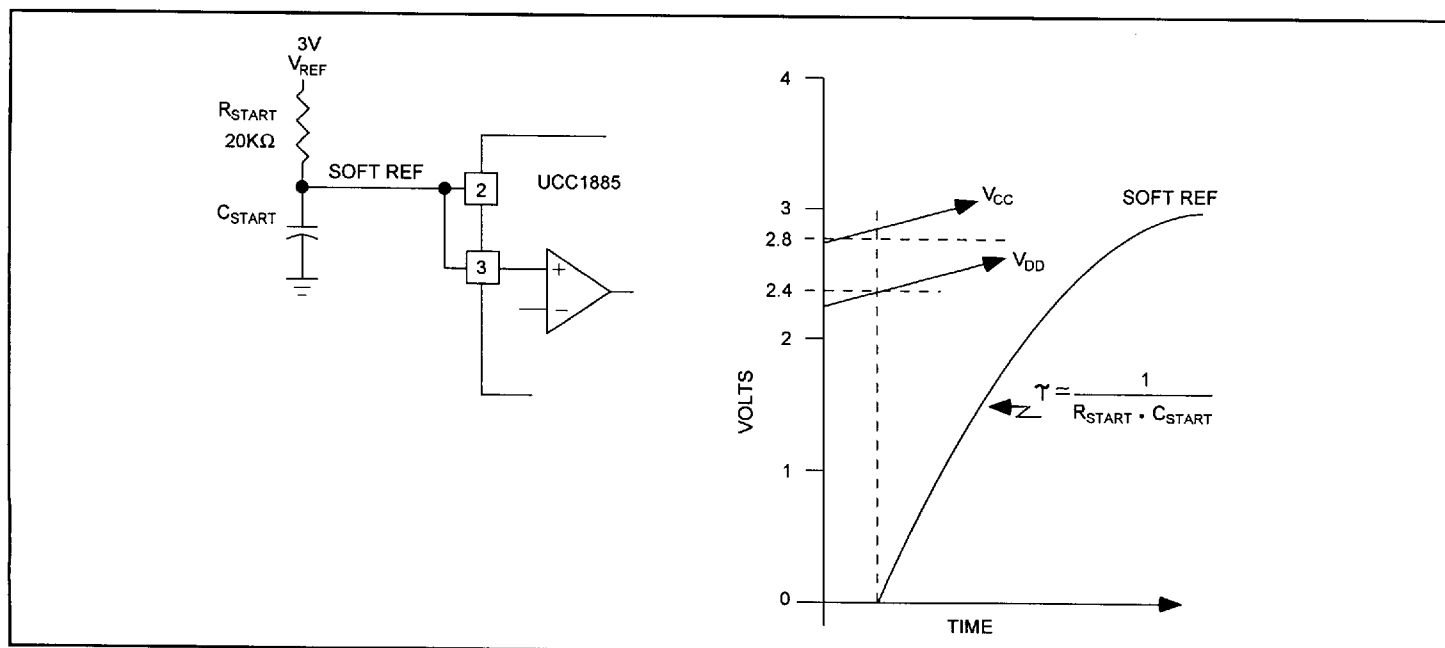
When power is first applied to the UCC1885, SOFTREF is held at ground until  $V_{CC}$  exceeds 2.8V and  $V_{DD}$  exceeds 2.4V. Once adequate operating voltages have been established, SOFTREF is released and allowed to charge from an internal 10 $\mu$ A current source. A capacitor from this pin to ground may be used to continue an output soft start after the UCC1885 takes control of the SMPS with feedback communication to the UCC1883. In this case, the  $dV/dt$  established on SOFTREF must exceed the  $dV/dt$  established on the regulated output by the blind soft start being provided by the UCC1883. Normally the SOFTREF pin will charge to 2.0V, the value of the internal precision reference. Once the internal reference voltage is reached, the current source is disabled and the SOFTREF pin maintains an output impedance of 30K $\Omega$ , which, acting with

any soft start capacitance, will then form a single-pole reference noise filter.

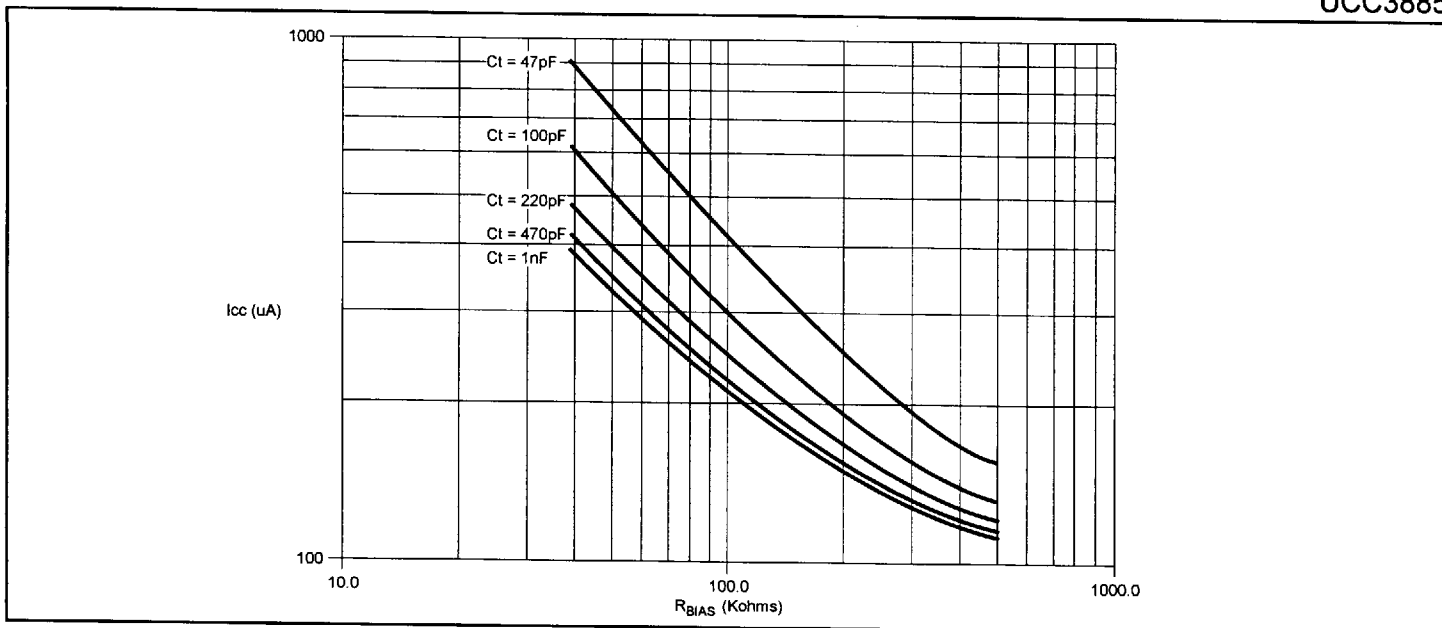
If the use of an external reference ( $V_{REF} > 2.5V$ ) is desired, the soft start function can still be maintained on SOFTREF. In this case, the user must also supply a soft start resistor between the external reference and SOFTREF. The value of this resistor should be chosen such that the current sourced into the SOFTREF pin when the voltage reaches 2.0V is at least 20 $\mu$ A, which will allow the UCC1885 to sense the presence of an external reference. Once the external reference is sensed, the internal reference is disconnected from SOFTREF, making it high impedance and eliminating any DC error across the soft start resistor. The minimum value of the soft start resistor



SOFT START WITH INTERNAL REFERENCE  
 FIGURE 3



SOFT START WITH EXTERNAL REFERENCE  
 FIGURE 4



AVERAGE DC CURRENT VERSUS  $R_{BIAS}$  (Not including Pulse Transformer Losses)  
**FIGURE 5**

should be limited to allow SOFTREF to pull low during UVLO. The output impedance of SOFTREF during this phase of operation is about 300 ohms to ground.

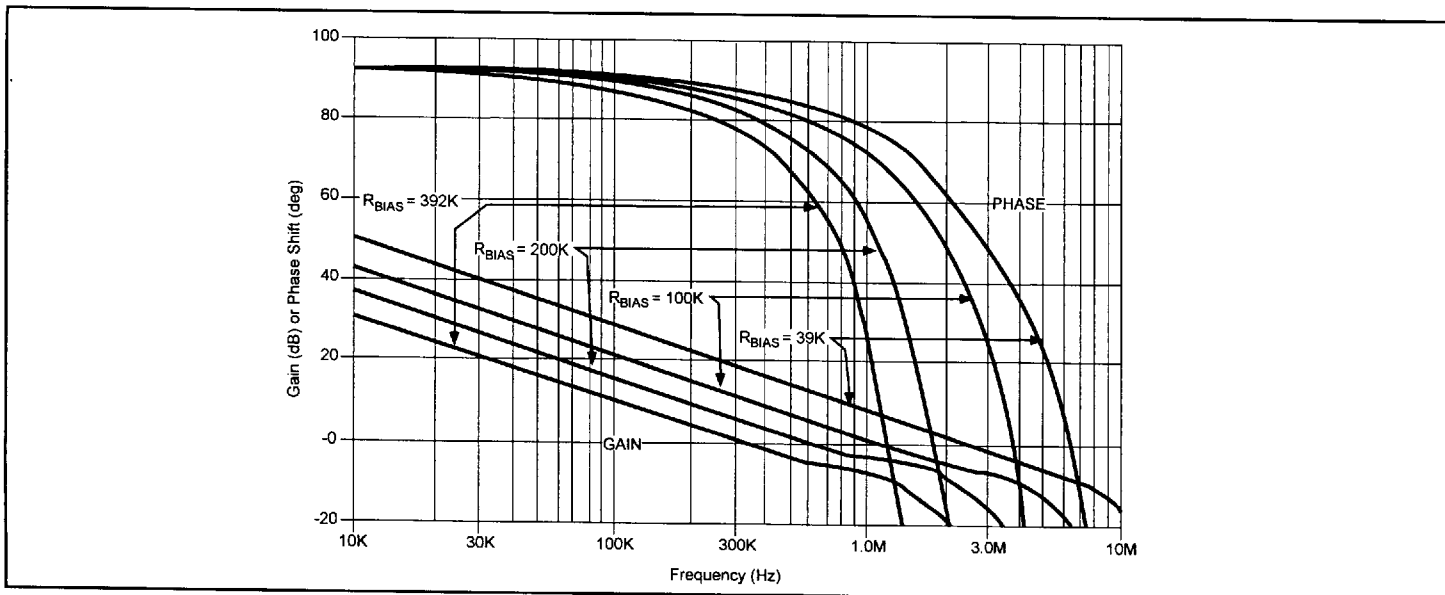
The final portion of the UCC1885 UVLO sequence occurs when the output of the error amplifier increases above 1.15V. Normally this will not occur until the system reference has charged to some intermediate value. Assuming that adequate operating voltage has also been established, then the isolation interface on the UCC1885 begins transmitting output pulse width control information to the UCC1883 via an isolation pulse transformer. The 1.15V required on the output of the error amplifier guarantees that the UCC1885 will initially begin transmitting information to the primary-side

PWM controller which keeps energy flowing to the secondary allowing the control loop to come into regulation. Once the isolation interface is enabled, the UVLO circuitry ignores all voltages appearing on the output of the error amplifier.

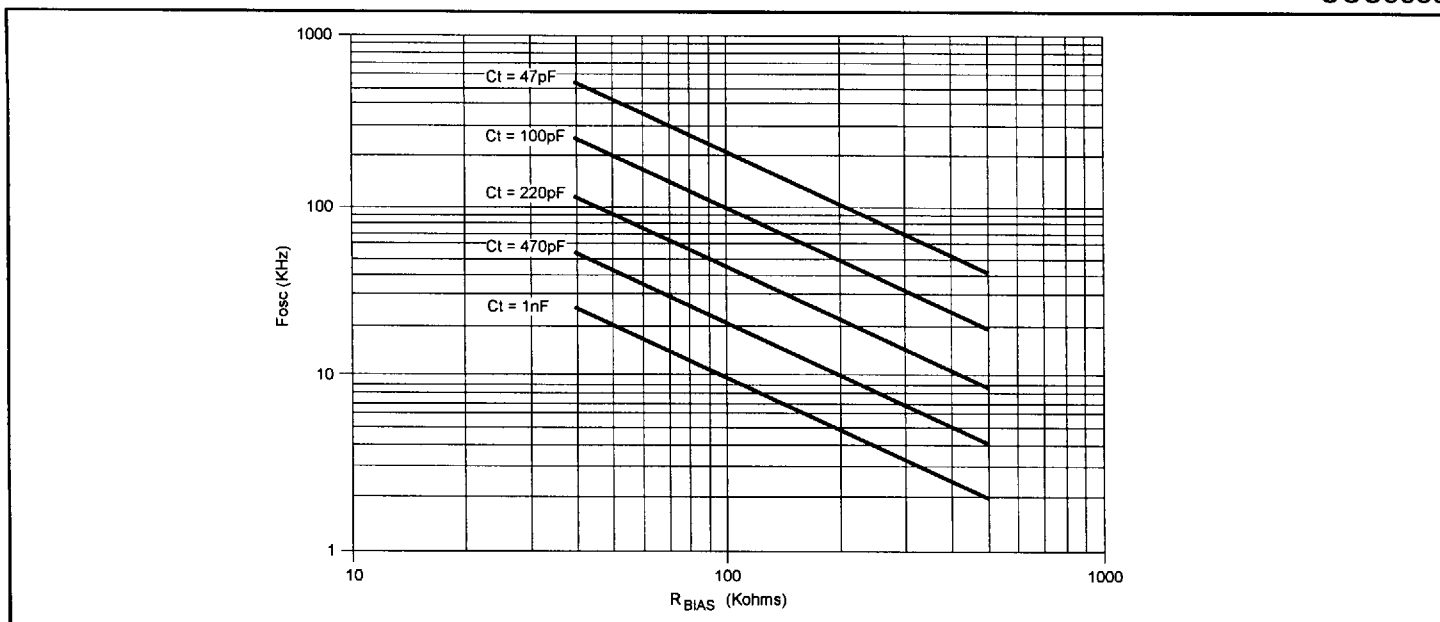
**USER BIAS PROGRAMMING**

The  $R_{BIAS}$  pin may be used to set the amount of quiescent current consumed by certain analog circuits within the UCC1885. A resistor from this pin to ground establishes a user bias current according to the equation

$$I_{BIAS} = \frac{1.2V}{R_{BIAS}}$$



ERROR AMPLIFIER GBW VERSUS  $R_{BIAS}$   
**FIGURE 6**



OSCILLATOR FREQUENCY VERSUS R<sub>BIAS</sub>  
**FIGURE 7**

Recommended range for R<sub>BIAS</sub> is 39.2 KΩ to 392 KΩ. Internal circuits on the UCC1885 consume a total quiescent current of  $9 \cdot I_{BIAS}$ , plus some fixed currents amounting to about 50uA at room temperature. Additional dynamic current consumption may be calculated with C<sub>PD</sub> (see specifications), given a certain oscillator frequency f<sub>OSC</sub>, from the equation

$$I_{DYNAMIC} = C_{PD} \cdot V_{DD} \cdot f_{OSC}$$

Also note from the specifications that the voltage on R<sub>BIAS</sub> is well controlled and thus may be effectively used as another reference voltage in the system.

### V<sub>DD</sub> LOGIC SUPPLY

The internal CMOS logic on the UCC1885 requires a supply limited to 7V. If the value of V<sub>CC</sub> is anticipated to be below 7V, then V<sub>DD</sub> should be wired directly to V<sub>CC</sub> and bypassed with at least 0.01uF. If V<sub>CC</sub> exceeds 7V, the UCC1885 provides an internal 5V regulator to the V<sub>DD</sub> pin for running the onboard CMOS logic. At these higher V<sub>CC</sub> voltages, the V<sub>DD</sub> pin should be disconnected and bypassed with at least 0.01uF. For this case of internal regulation, V<sub>DD</sub> bypass capacitance should not exceed 10uF.

### ERROR AMPLIFIER

The UCC1885 error amplifier is intended to be the control amplifier for the voltage loop of the ISDN SMPS. It is a low offset, high gain design. Output swing is typically limited to a maximum of 2.7V. The GBW of the amplifier is controlled by the value of R<sub>BIAS</sub> supplied by the user on pin 1. Input common mode range is between 1V and V<sub>CC</sub> - 0.5V. If both inputs are beneath the common mode range during soft start,

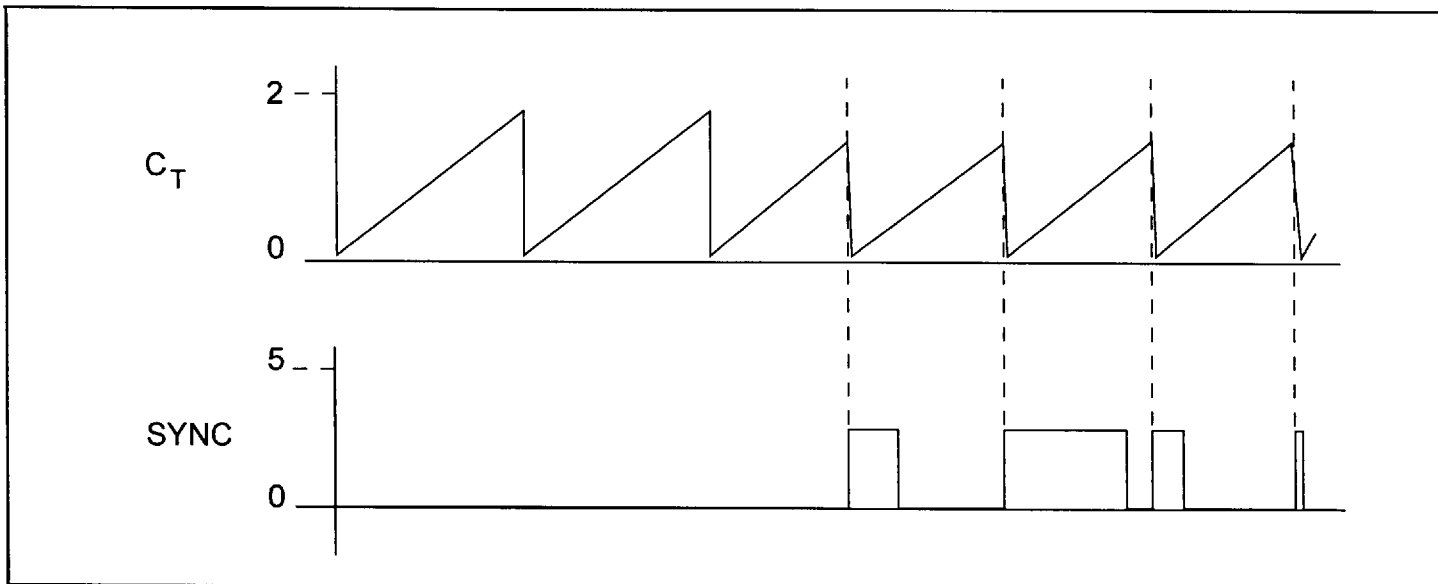
special circuitry on the UCC1885 guarantees VA out will be very near ground to insure proper startup.

### OSCILLATOR

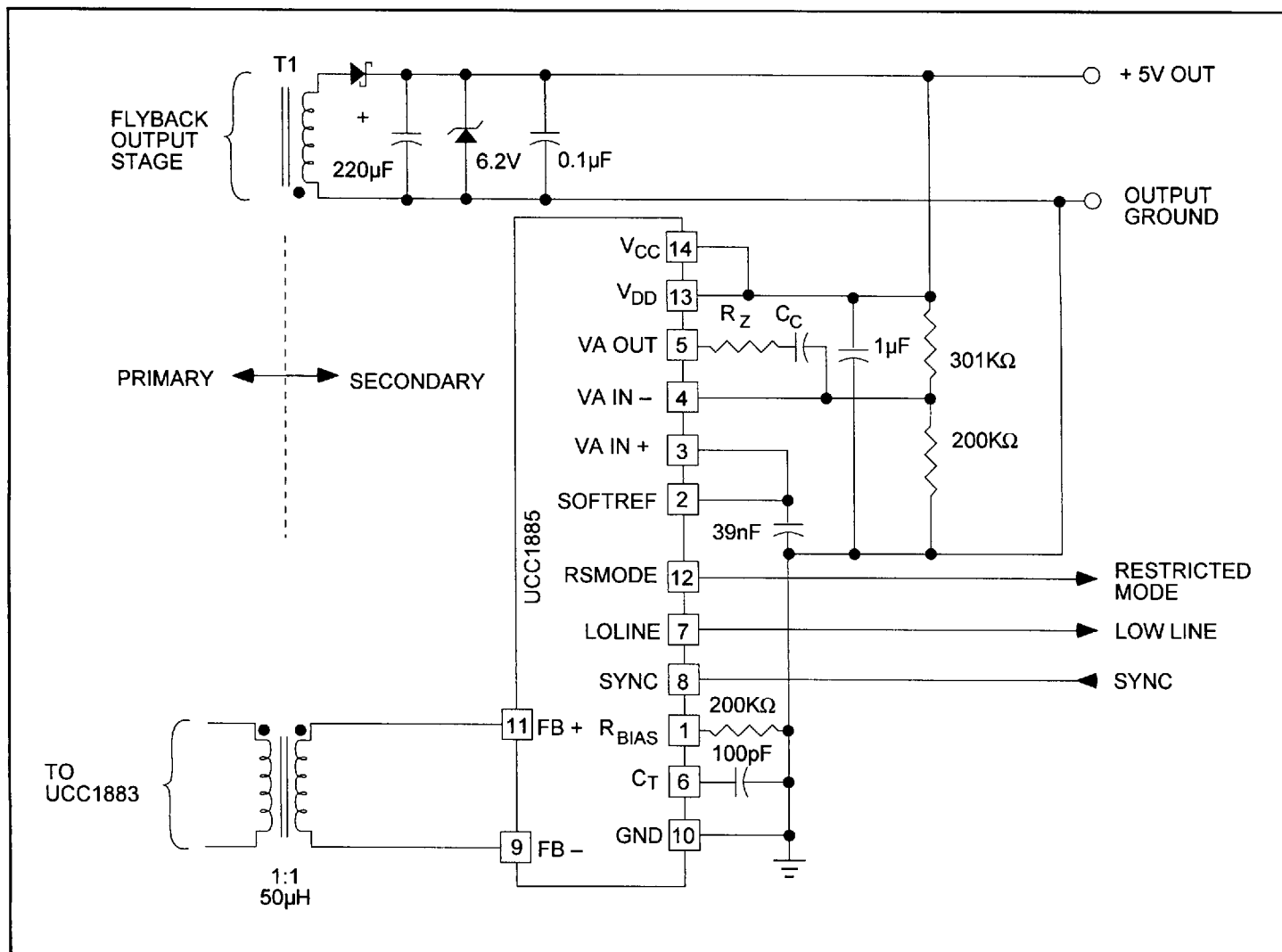
A timing capacitor is connected between C<sub>T</sub> and ground to program a natural oscillator frequency according to the equation

$$f_{OSC} = \frac{1}{C_T \cdot R_{BIAS}}$$

A ramp voltage running from ground to 1.8V is created on the C<sub>T</sub> pin. This oscillator may be synchronized to a system clock applied to SYNC. Proper synchronization will only occur if the frequency of the SYNC signal exceeds the natural frequency programmed into the oscillator. A new oscillator cycle (ramp returns to ground) will be initiated on each rising edge of SYNC, with a corresponding decrease in ramp amplitude. SYNC should be wired to ground if this feature is not used. The ramp amplitude represents the maximum value of error amplifier output voltage which may be passed over the isolation interface to the UCC1883. Thus a minimum synchronized ramp amplitude of 1.3V is recommended. The UCC1885 will accept a wide range of duty cycles on the SYNC pin, but rise and fall times of longer than 200ns are not recommended.



OSCILLATOR WAVEFORMS  
 FIGURE 8



TYPICAL APPLICATION  
 FIGURE 9