

**FEATURES****Supply voltage**

Single: 1.8 V to 5.5 V

Dual:  $\pm 2.5$  V**TTL-/CMOS-compatible control inputs****Switch control options**

On-board links

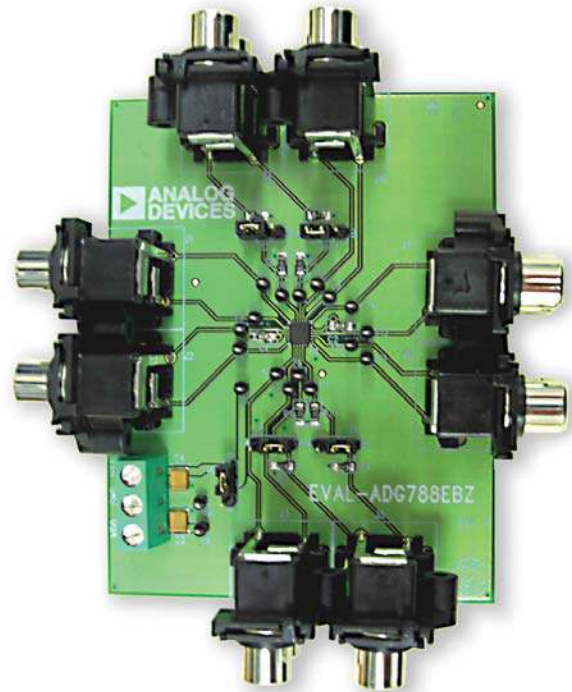
External control signals

**RoHS compliant****GENERAL DESCRIPTION**

This data sheet describes the evaluation board for the ADG788, a triple SPDT switch packaged in a compact 4 mm  $\times$  4 mm body, 20-lead LFCSP package. The switches are designed using an enhanced submicron CMOS process to provide optimal performance in terms of on resistance, bandwidth, and power dissipation. The excellent on resistance flatness makes the ADG788 ideal for a wide range of applications, including data and audio-video switching. Each SPDT switch can be individually controlled using a 1-wire parallel interface.

The evaluation board supports both single- and dual-supply operation and comes fitted with connectors that allow the user to evaluate the performance of the ADG788 with minimum effort. The operation of the switches is controlled using the on-board links or by applying external control signals to the appropriate connectors.

The data sheet for the ADG788 device is available from Analog Devices, Inc. It contains all the information regarding operation of the device, and it should be consulted in conjunction with this data sheet when using the evaluation board.

**EVALUATION BOARD***Figure 1.*

00756-001

**Rev. 0**

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**REVISION HISTORY**

6/07—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

The ADG788 evaluation board kit contains the following:

- A fully fitted printed circuit board
- A CD containing the ADG788 product data sheet and the evaluation board data sheet

The evaluation board allows the user to connect the signals that require switching to the ADG788 switch and control its operation by using the on-board links or by applying the correct control signals to the appropriate connectors. The signals present at the pins of the ADG788 can be monitored using the test point provided on the board.

The following sections describe the function of all connectors and links.

### POWER SUPPLY

To operate the ADG788 evaluation board, the user must provide an external power supply connected to Power Block P1. The supply voltage range is 1.8 V to 5.5 V for single-supply operation and  $\pm 2.5$  V for dual-supply operation. The user can select single-supply operation or dual-supply operation using Link J23, as shown in Table 1.

**Table 1. Link J23 Configuration**

Position	Operation Mode
A	Single-supply operation
B	Dual-supply operation (default configuration)

### SWITCH CONTROL

The four input pins, IN1, IN2, IN3, and IN4, control the operation of the ADG788. Link J8, Link J9, Link J12, and Link J13 control the logic levels applied to these pins and allow the user to drive these pins with external signals applied to Connector J5 and Connector J11 (the signals have 50  $\Omega$  on-board termination resistors to GND). Table 2 describes the configuration achieved for each position of these links.

**Table 2. Link J8, Link J9, Link J12, and Link J13 Settings**

Link	Position	ADG788 Switch Status	
J8	Removed	S2A to D2 = off, S2B to D2 = on	
	A	S2A to D2 = on, S2B to D2 = off	
	B (default configuration)	Controlled via signal applied to Connector J5_TOP	High: S2A to D2 = on, S2B to D2 = off Low: S2A to D2 = off, S2B to D2 = on
J9	Removed	S3A to D3 = off, S3B to D3 = on	
	A	S3A to D3 = on, S3B to D3 = off	
	B (default configuration)	Controlled via signal applied to Connector J5_BOTTOM	High: S3A to D3 = on, S3B to D3 = off Low: S3A to D3 = off, S3B to D3 = on
J12	Removed	S1A to D1 = off, S1B to D1 = on	
	A (default configuration)	Controlled via signal applied to Connector J11_BOTTOM	High: S1A to D1 = on, S1B to D1 = off Low: S1A to D1 = off, S1B to D1 = on
	B	S1A to D1 = on, S1B to D1 = off	
J13	Removed	S4A to D4 = off, S4B to D4 = on	
	A (default configuration)	Controlled via signal applied to Connector J11_TOP	High: S4A to D4 = on, S4B to D4 = off Low: S4A to D4 = off, S4B to D4 = on
	B	S4A to D4 = on, S4B to D4 = off	

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## CONNECTIONS AND TEST POINTS

Table 3.

Connector	Position	Test Point	Connection to ADG788 Pin
J1	Top	T19	S1A
	Bottom	T1	D1
J2	Top	T2	S1B
	Bottom	T3	S2B
J3	Top	T4	D2
	Bottom	T5	S2A
J4	V <sub>DD</sub>	T9	V <sub>DD</sub>
	GND	T10	GND
	V <sub>SS</sub>	T8	V <sub>SS</sub>
J5 <sup>1</sup>	Top	T6	IN2
	Bottom	T7	IN3
J6	Top	T11	S3A
	Bottom	T12	D3
J7	Top	T13	S3B
	Bottom	T14	S4B
J10	Top	T15	D4
	Bottom	T16	S4A
J11 <sup>1</sup>	Top	T17	IN4
	Bottom	T18	IN1

<sup>1</sup> This connector is tied to the ADG788 pins only when Link J8 and Link J9 are set in Position B, and J12 and J13 are in Position A.

# EVALUATION BOARD SCHEMATICS AND ARTWORK

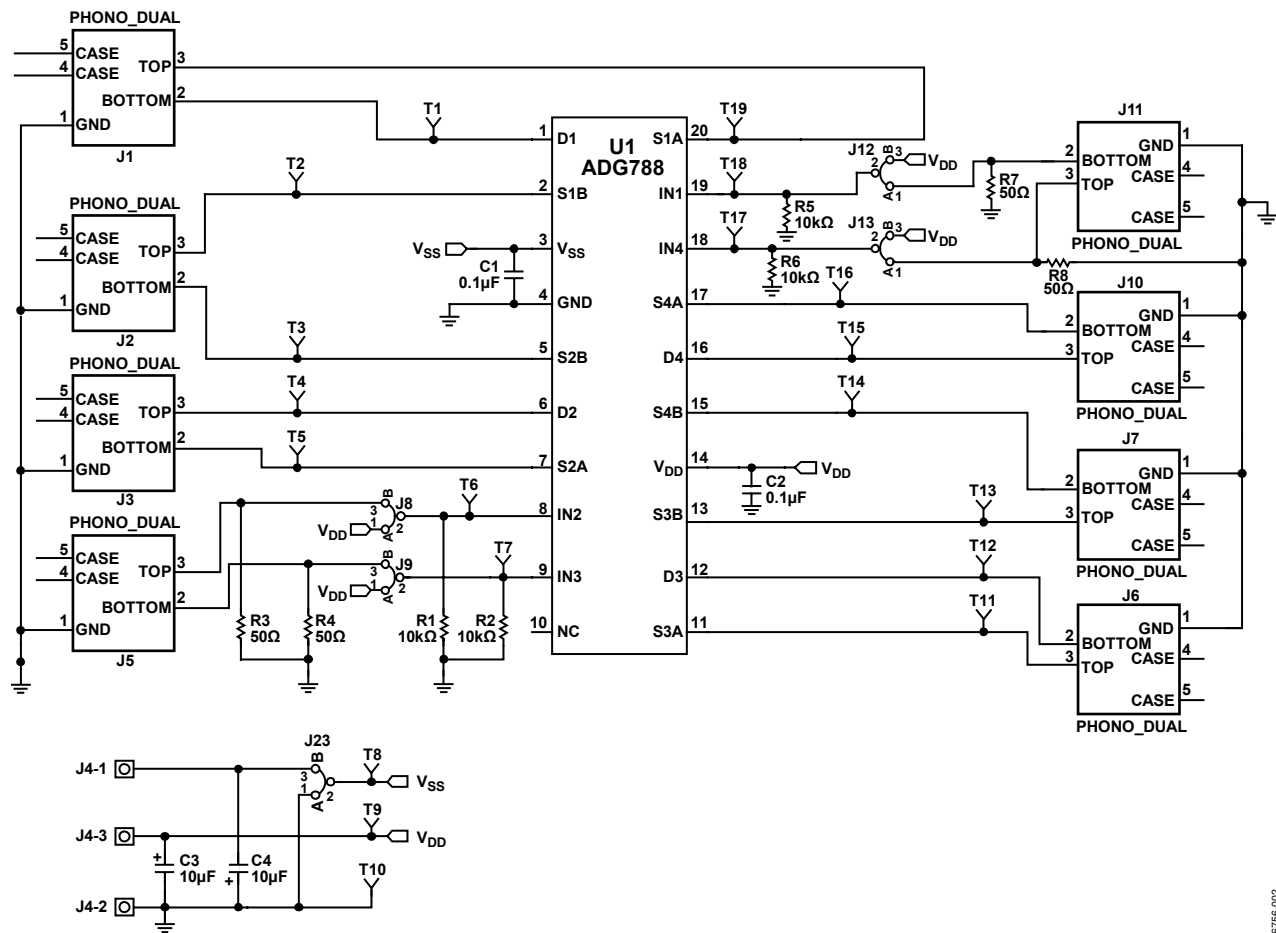
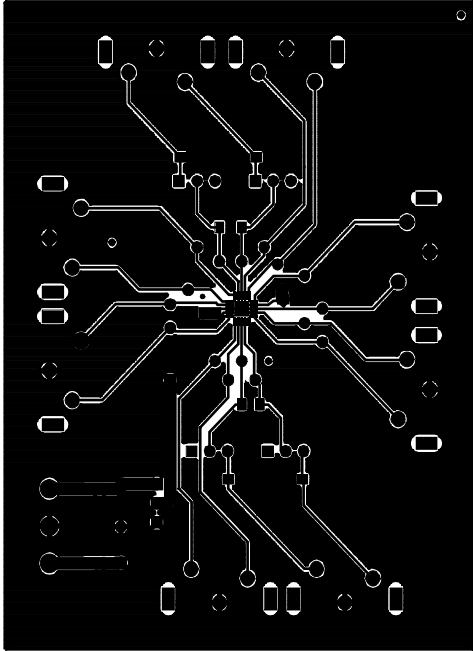


Figure 2. Evaluation Board Schematic

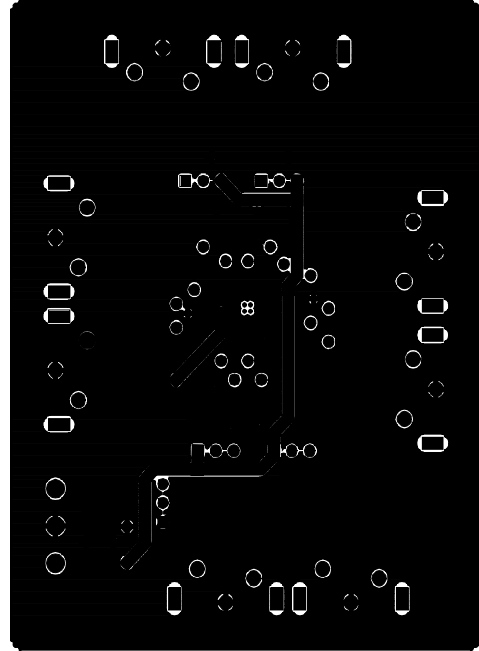
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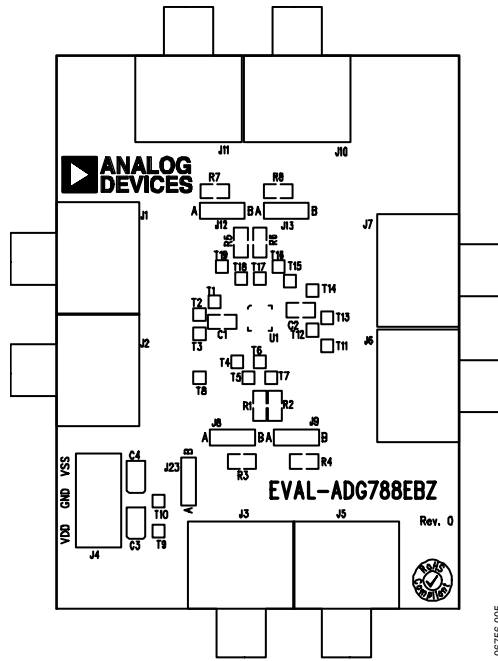
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Figure 3. Component Side PCB Drawing (Layer 1)



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Figure 4. Solder Side PCB Drawing (Layer2) Component Side View



06756-005

Figure 5. Component Side Silkscreen PCB Drawing

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 4.

Qty	Reference Designator	Description	Supplier/Number
2	C1, C2	0.1 $\mu$ F SMD ceramic capacitor	FEC 301-9482
2	C3, C4	10 $\mu$ F (0805 package) 10 V X5R SMD ceramic capacitor	FEC 498-737
8	J1, J2, J3, J5, J6, J7, J10, J11	Dual phono connector	FEC 128-0670
1	J4	3-pin power block	FEC 963-2980
5	J8, J9, J12, J13, J23	3-pin SIL header and shorting link	FEC 486-1220 and FEC 148-029
4	R1, R2, R5, R6	10 k $\Omega$ SMD resistor	FEC 933-0399
4	R3, R4, R7, R8	50 $\Omega$ SMD resistor	FEC 933-1336
19	T1 to T19	Test point	FEC 873-1128
1	U1	ADG788BCPZ	Analog Devices, Inc.

### ORDERING GUIDE

Model	Package Description
EVAL-ADG788EBZ <sup>1</sup>	ADG788 Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**EVAL-ADG788EBZ**

**NOTES**