9P750CGLF

Category: Zero Delay Buffers

Generic Part: 9P750

Market Group: PC CLOCK

Description: PC BUFFER
Recommended Application: DDR Zero Delay Clock Buffer Product Description/Features: â€¢ Low skew, low jitter PLL clock driver â€¢ 12 pairs of differential outputs support up to DDR400 â€¢ Outputs divided into 3 groups - Group A is reference - Groups B and C have default offsets from Group A, but also have skew programmable in steps relative to Group A. - Skew step (unit) set via RSTEP resistor â€¢ Static Phase Offset (SPO) of entire device can be programmed - RSPO sets overall SPO (analog delay) - I2C register settings allow fine tuning in steps defined by RSTEP â€¢ Spread spectrum tolerant inputs â€¢ 2.5 V differential reference clock input Switching Characteristics: â€¢ PEAK - PEAK jitter (>100MHz): <75ps â€¢ CYCLE - CYCLE jitter (>100MHz):<65ps â€¢ OUTPUT - OUTPUT skew: <50ps â€¢ DUTY CYCLE: 49% - 51% â€¢ Slew rate: 1V/ns - 2V/ns â€¢ Input clock duty cycle: 40% - 60%

Parameters

Package	TSSOP 48 (PAG48)
Voltage	3.3 V
Package	TSSOP 48
Speed	NA
Temperature	C
Status	Active
Sample	Yes
Minimum Order Quantity	76
Factory Order Increment	38

Distributor Inventory

No Pricing information is available from our Distributors at this time.

Documents

Type	Title	Size	Revision Date
Misc	PC Clocks Contact Info	61 KB	05/29/2007

Package

Description	TSSOP 6.10 MM
Class	PLASTIC
Moisture Sensitivity Level (MSL)	1
Category	Green
Moisture Exposure Floor Life	Unlimited @ <30°C/85% RH
Peak Reflow Temprature	260°C
Rebake Conditions	N/A
Length	12.5
Mark	G
Width	6.1
Pitch	0.5
Thickness	1.0
Status	Active