CY62167ESL MoBL®

16-Mbit (1 M × 16) Static RAM

Features

- High speed: 45 ns/55 ns
- Temperature range:
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 1.65 V to 1.95 V, 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra-low standby power
  - Typical standby current at 25 °C = 1.5 µA
  - Typical standby current at 40 °C = 2.5 µA
- Ultra-low active power
  - Active current: I_{CC} = 2.2 mA (typical) at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Pb-free 60-pin WLCSP packages

Functional Description

The CY62167ESL is a high-performance CMOS Static RAM organized as 1M words by 16 bits. This device features an advanced circuit design that provides an ultra low active current. Ultra low active current is ideal for providing More Battery Life™ (MoBL®) in portable applications such as hand-held devices. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH).

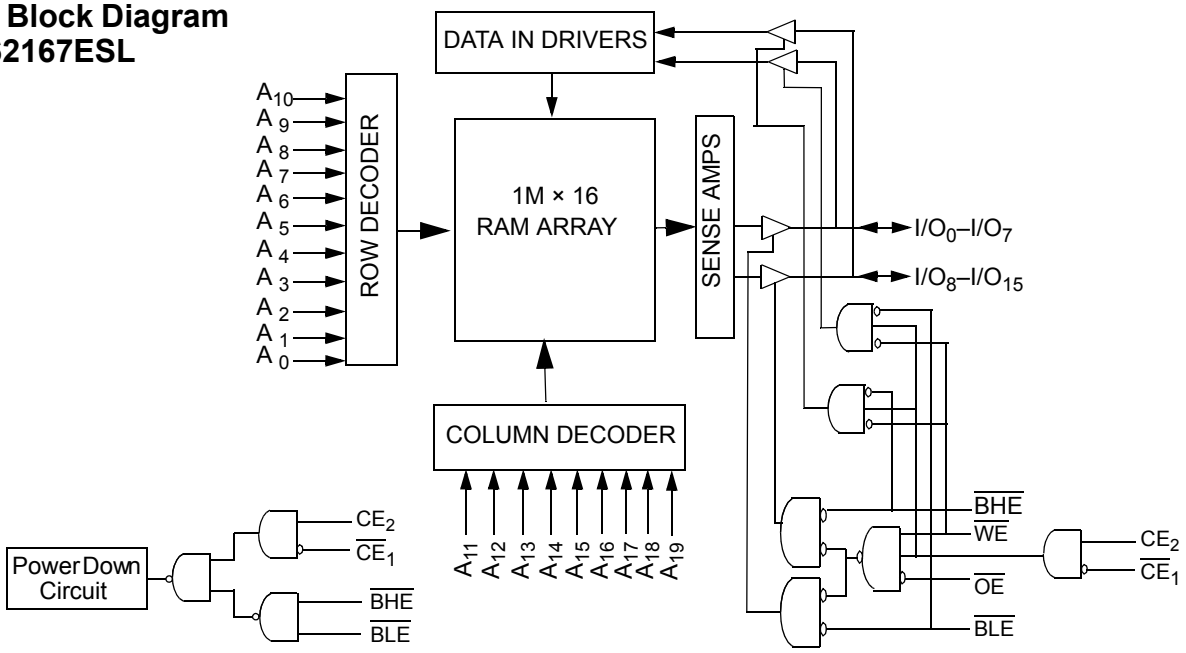
The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state during the following events:

- The device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW)

Write to the device by taking Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from the I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

Read from the device by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 12 for a complete description of read and write modes.

Logic Block Diagram – CY62167ESL



Contents

Pin Configurations

Figure 1. 60-Pin WLCSP Pinout (Ball Up View)[1]

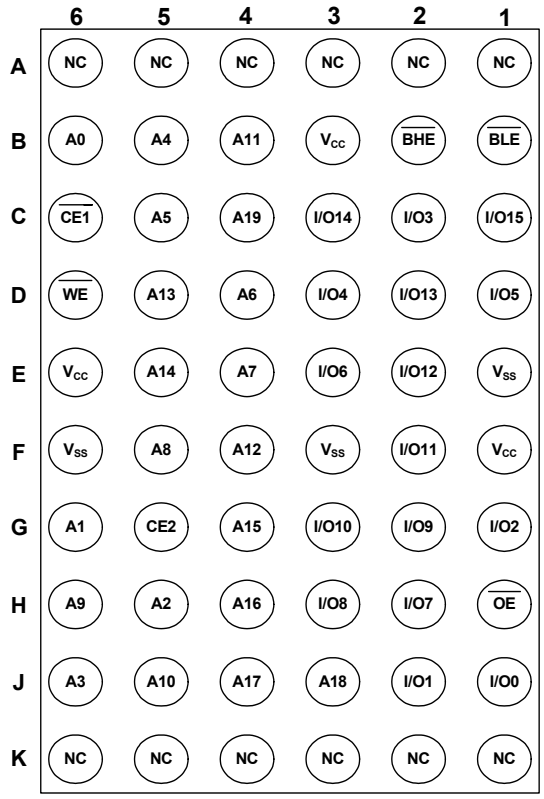
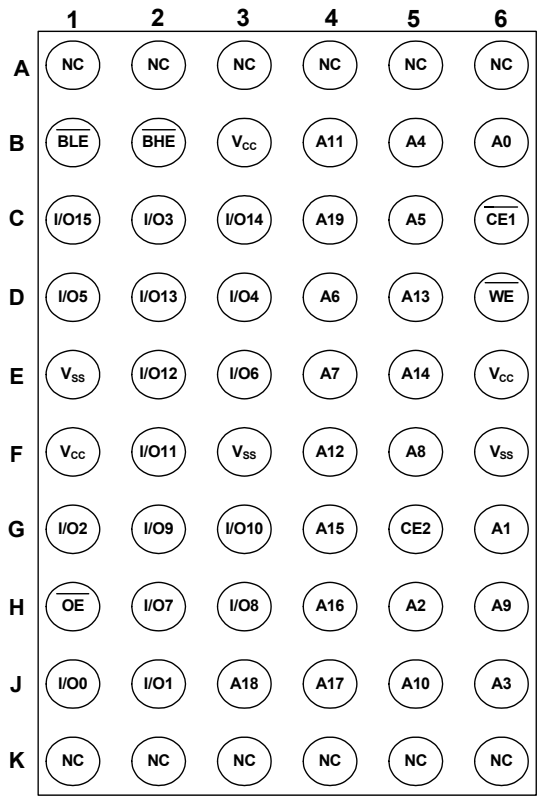


Figure 2. 60-Pin WLCSP Pinout (Ball Down View)[1]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ	Max		Typ	Max	Typ	Max	Typ	Max
CY62167ESL	Industrial	4.5	5.0	5.5	45	2.2	4.0	25	30	1.5	12
		2.2	3.0	3.6							
		1.65	1.8	1.95	55						

Notes
1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential [2, 3] .....–0.5 V to 6.0 V

DC voltage applied to outputs in High Z state [2, 3] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [2, 3] ..... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [4]
CY62167ESL	Industrial	–40 °C to +85 °C	1.65 V to 1.95 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Test Conditions		45/55 ns			Unit
				Min	Typ [5]	Max	
V_{OH}	Output HIGH Voltage	$1.65 \le V_{CC} \le 1.95$	I_{OH} = –0.1 mA	1.4	–	–	V
		$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	
		$4.5 \le V_{CC} \le 5.5$	I_{OH} = –1.0 mA	2.4	–	–	
V_{OL}	Output LOW Voltage	$1.65 \le V_{CC} \le 1.95$	I_{OL} = 0.1 mA	–	–	0.2	
		$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	
		$2.7 \le V_{CC} \le 3.6$	I_{OL} = 2.1 mA	–	–	0.4	
		$4.5 \le V_{CC} \le 5.5$	I_{OL} = 2.1 mA	–	–	0.4	
V_{IH}	Input HIGH Voltage	$1.65 \le V_{CC} \le 1.95$		1.4	–	V_{CC} + 0.2	
		$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	
		$4.5 \le V_{CC} \le 5.5$		2.2	–	V_{CC} + 0.5	
V_{IL}	Input LOW Voltage	$1.65 \le V_{CC} \le 1.95$		–0.2	–	0.4	
		$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.8	
		$4.5 \le V_{CC} \le 5.5$		–0.5	–	0.8	
I_{IX}	Input Leakage Current	$GND \le V_I \le V_{CC}$		–1.0	–	+1.0	µA
I_{OZ}	Output Leakage Current	$GND \le V_O \le V_{CC}$, Output disabled		–1.0	–	+1.0	
I_{CC}	V_{CC} Operating Supply Current	f = f_{max} = $1/t_{RC}$	V_{CC} = Vcc Max. I_{OUT} = 0 mA, CMOS levels	–	25.0	30.0	mA
		f = 1 MHz		–	2.2	4.0	
I_{SB1} [6]	Automatic CE Power-down Current – CMOS Inputs	$\overline{CE}_1 \ge V_{CC}$ – 0.2 V or $CE_2 \le$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V, $V_{IN} \le$ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(max)}$		–	–	12.0	µA
I_{SB2} [6]	Automatic CE Power-down Current – CMOS Inputs	$\overline{CE}_1 \ge V_{CC}$ – 0.2V or $CE_2 \le$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) $\ge V_{CC}$ – 0.2 V, $V_{IN} \ge V_{CC}$ – 0.2 V or $V_{IN} \le$ 0.2 V, f = 0, $V_{CC} = V_{CC(max)}$	25 °C [5]	–	1.5	4.0	
			40 °C [5]	–	2.5	7.0	
			85 °C	–	–	12.0	

Notes

2. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
3. $V_{IH(max)} = V_{CC}$ + 0.75 V for pulse durations less than 20 ns.
4. Full Device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
5. These values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
6. Chip enables ($\overline{CE}_1$ and CE_2) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be tied to CMOS levels to meet the I_{SB1}/I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

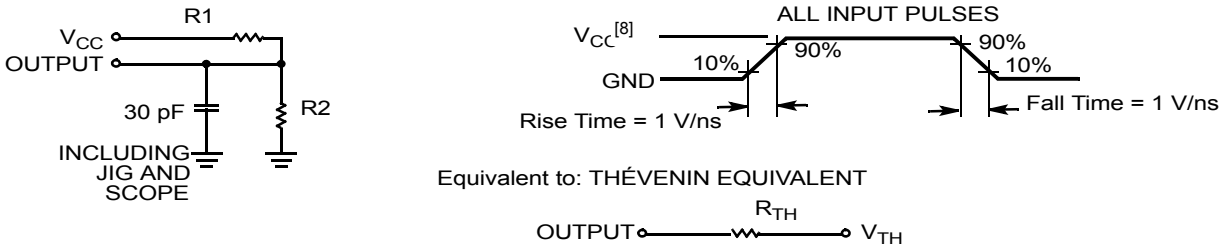
Parameter [7]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10.0	pF
C_{OUT}	Output Capacitance		10.0	pF

Thermal Resistance

Parameter [7]	Description	Test Conditions	WLCSP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	26.54	°C/W
Θ_{JC}	Thermal resistance (junction to case)		0.11	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	1.65 V to 1.95 V	2.2 V to 2.7 V	2.7 V to 3.6 V	4.5 V to 5.5 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V

Notes
7. Tested initially and after any design or process changes that may affect these parameters.
8. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference level of 1.5V (for V_{CC} > 3V) and V_{CC}/2 (for V_{CC} < 3V), and input pulse levels of 0 to 3V (for V_{CC} > 3V) and 0 to V_{CC} (V_{CC} < 3V) and output loading of the specified I_{OL}/I_{OH} as shown.

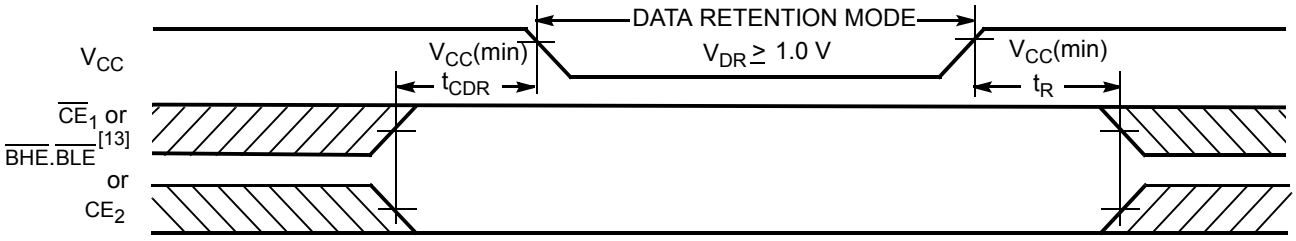
Data Retention Characteristics

Over the operating range of –40 °C to 85 °C

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for Data Retention	–	1.0	–	–	V
I_{CCDR}[10]	Data Retention Current	V_{CC} = 1.0 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V or ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	10.0	µA
t_{CDR}[11]	Chip Deselect to Data Retention Time	–	0.0	–	–	–
t_R[12]	Operation Recovery Time	–	45/55	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes
9. Typical values are included for reference only, and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enables ($\overline{CE_1}$ and CE_2) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

AC Switching Characteristics

Over the operating range of –40 °C to 85 °C

Parameter [14, 15]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [15]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [15, 16]	–	18	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z [15]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z [15, 16]	–	18	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down	–	45	–	55	ns
t_{DBE}	BLE / BHE LOW to data valid	–	45	–	55	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z [15]	10	–	10	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z [15, 16]	–	18	–	18	ns
Write Cycle [17, 18]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [15, 16]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [15]	10	–	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference level of 1.5V (for V_{CC} > 3V) and V_{CC}/2 (for V_{CC} < 3V), and input pulse levels of 0 to 3V (for V_{CC} > 3V) and 0 to V_{CC} (V_{CC} < 3V) and output loading of the specified I_{OL}/I_{OH} as shown in Figure 3 on page 5.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
18. The minimum pulse width for write cycle 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [19, 20]

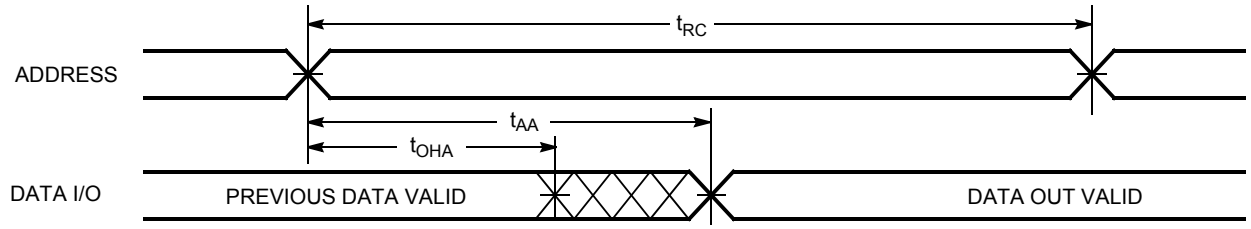
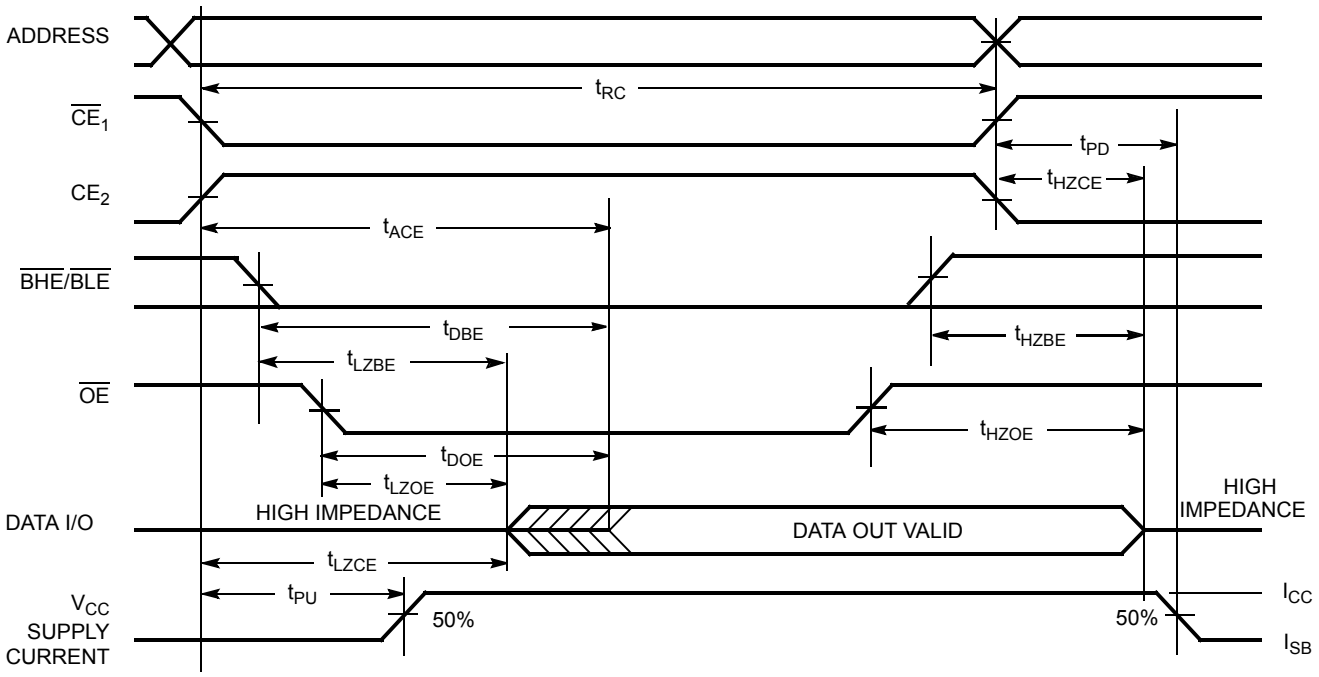


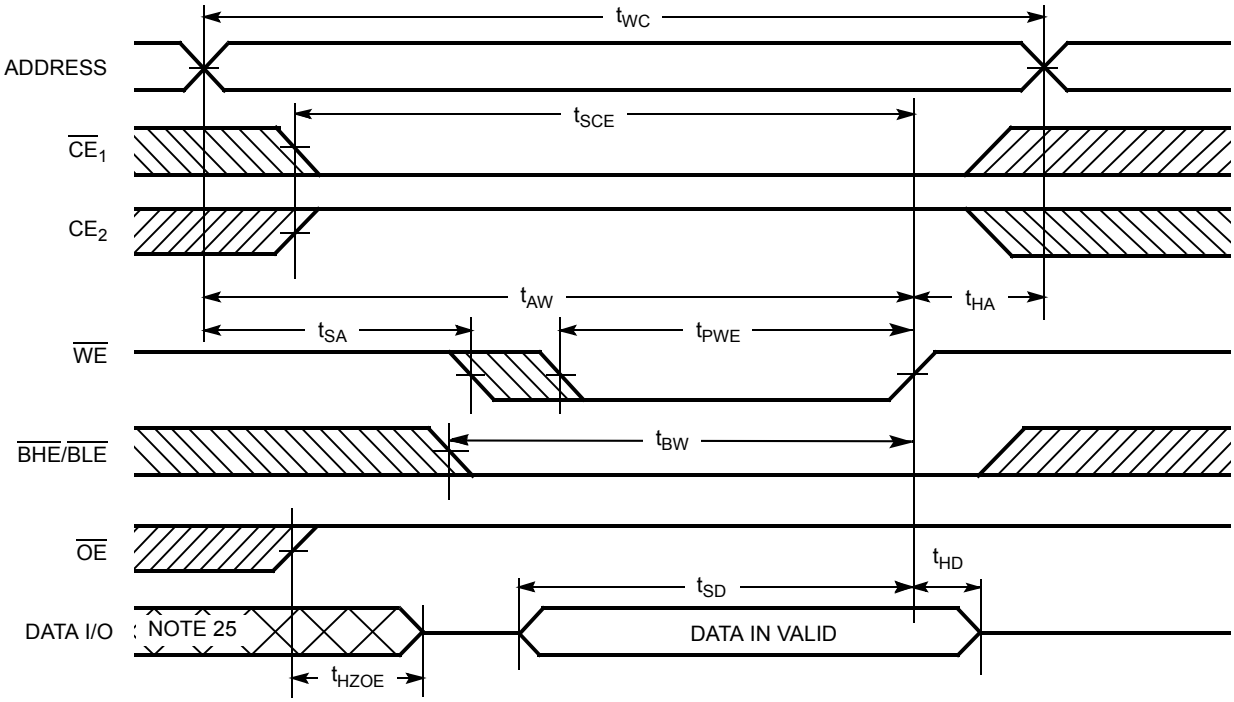
Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [20, 21]



Notes
19. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [22, 23, 24]

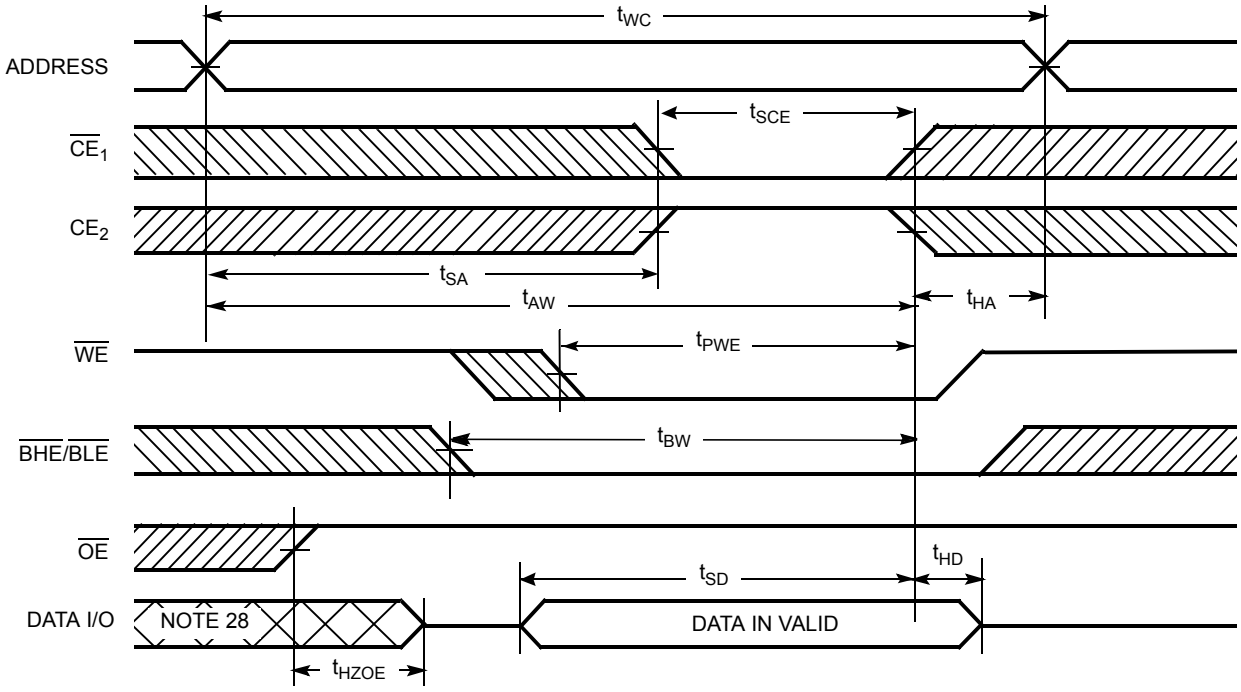


Notes

22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ($\overline{CE}_1$ or CE_2 Controlled) [26, 27]



Notes

26. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
28. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (WE Controlled, OE LOW) [29, 31]

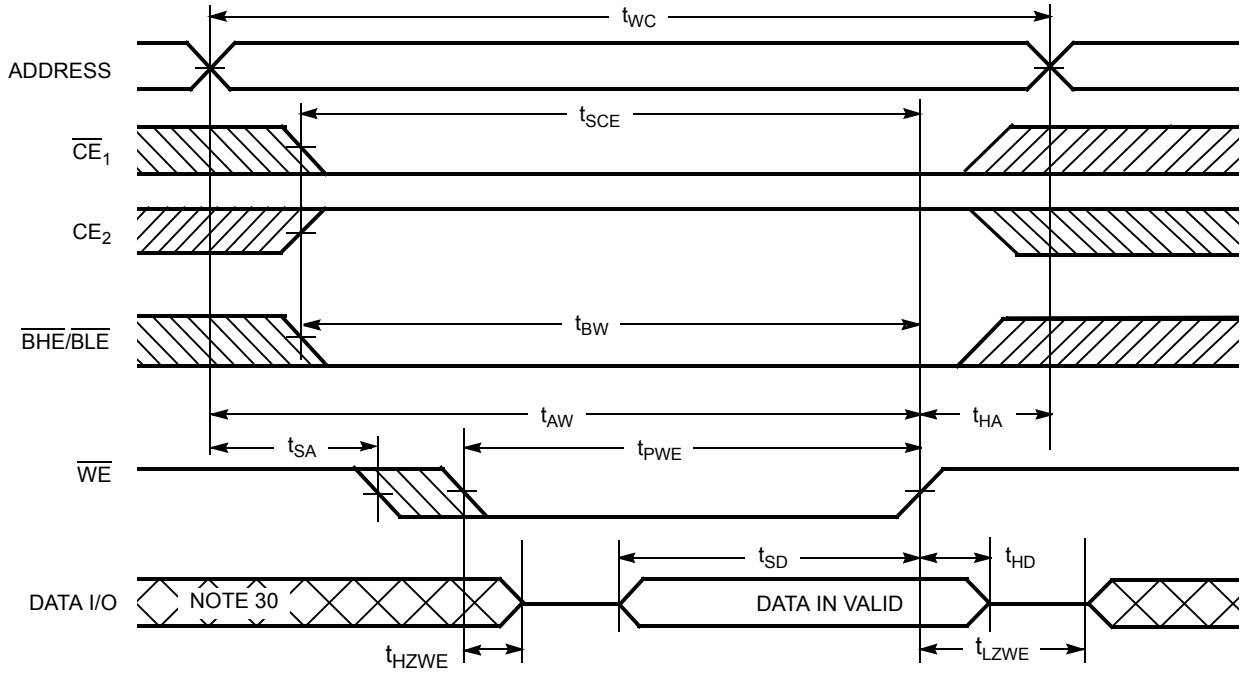
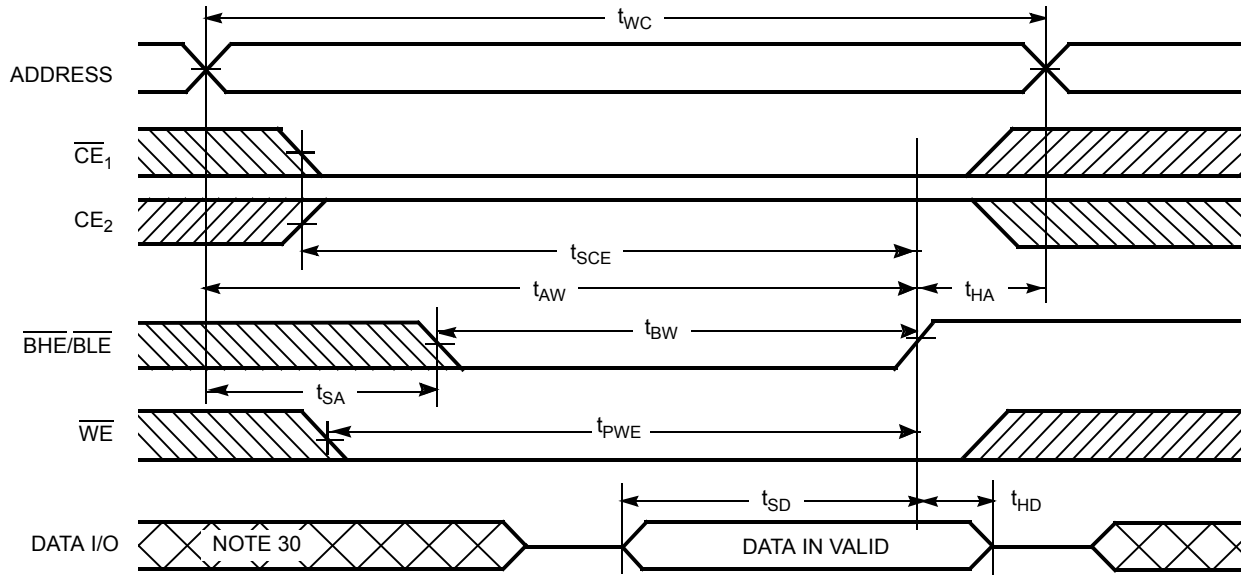


Figure 10. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [29]



Notes
29. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
30. During this period, the I/Os are in output state. Do not apply input signals.
31. The minimum pulse width for write cycle 3 (WE controlled, OE LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

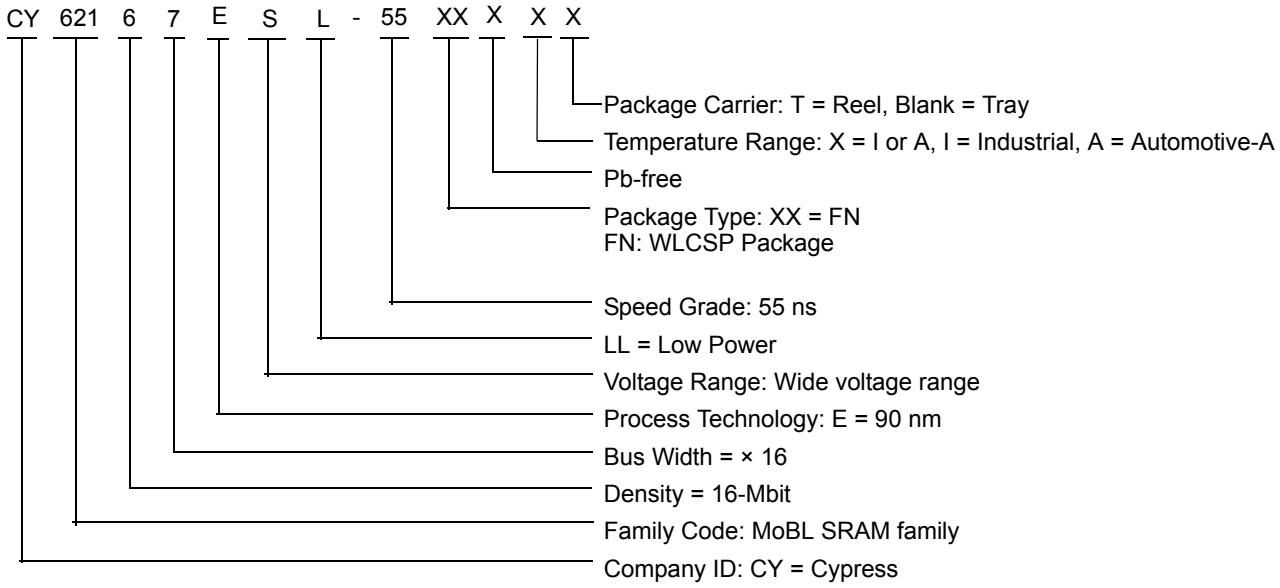
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[32]	X	X	X[32]	X[32]	High Z	Deselect/Power-down	Standby (I_{SB})
X[32]	L	X	X	X[32]	X[32]	High Z	Deselect/Power-down	Standby (I_{SB})
X[32]	X[32]	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7) High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7) Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7) High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7) Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Note
32. The 'X' (Don't care) state for the chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

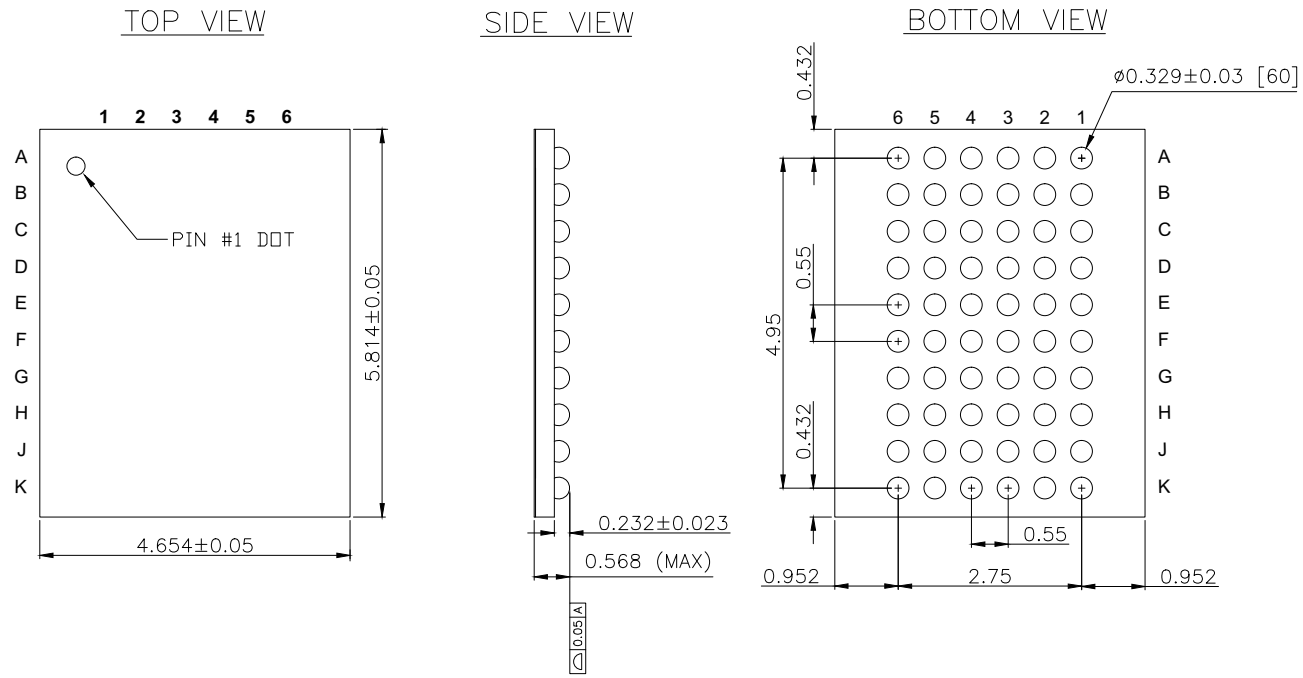
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62167ESL-55FNXI	001-96092	WLCSP	Industrial
	CY62167ESL-55FNXIT			

Ordering Code Definitions



Package Diagram

Figure 11. 60-Pin WLCSP Package Outline



NOTES:
1. Reference Jedec Publication 95; Design Guide 4.18
2. All dimensions are in millimeters

001-96092 **

Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4626678	VINI	02/03/2015	New datasheet.
*A	4664021	VINI	02/17/2015	Added Thermal Resistance. Updated the label “V” to “V_{TH}” in Figure 3.
*B	4841477	VINI	07/16/2015	Updated Ordering Information and Ordering Code Definitions to include Tape and Reel parts.
*C	6003255	AESATMP9	12/22/2017	Updated logo and copyright.

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