SLVL005

XILINXPWR-080 (HPA-080)
Dual Linear Regulator Power Management Solution Providing up to 850 mA from V_{IN} = 3.3 V

SUPPORTS:

- Spartan™-3 Design 2 (PR214) - http://focus.ti.com/lit/ml/slva175/slva175.pdf

FEATURES:

- Dual channel low-dropout (LDO) linear regulator in thermally enhanced PowerPAD™ package saves cost and space.
- Linear regulators start-up fast, allowing large in-rush currents for charging decoupling capacitors and FPGA start-up. The current draw on the input power supply is minimized by the use of the optional:
  - External SVS, U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
  - Soft-start circuit consisting of the external NMOS transistor Q1 and supporting passive components to provide 10 ms rise time for V_{CCINT}
    - Soft-start circuit (Q1) forces sequencing of V_{CCAUX}, then V_{CCINT}, with EN1 and EN2 tied together.
- The design meets Xilinx's V_{CCINT} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at http://www.ti.com/xilinxfpga for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/TPS70402.pdf and http://focus.ti.com/lit/ds/symlink/tlc7733.pdf.
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations when using linear regulators.
- Link to application note SLVA156 http://focus.ti.com/lit/an/slva156/slva156.pdf for more details on the soft-start circuit.
- Link to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf when using 3.3-V JTAG ports.

IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads.

- **Power Dissipation/Thermal Issues:** The dual regulator, U2, is limited to 2W @ $T_A = 55^o$ C and no airflow, due to power dissipation limitation of the PowerPAD™ package.
  - Refer to the application section of the datasheet for maximum power dissipation at different ambient conditions and guidance on sizing the ground plane area underneath the package for heatsinking.
  - The following equation can be used to solve for the maximum current on one rail if the other rail current is known:
    $P_{Dmax} = (V_{IN} - V_{CCINT}) * I_{CCINTmax} + (V_{IN} - V_{CCAUX}) * I_{CCAUXmax}$

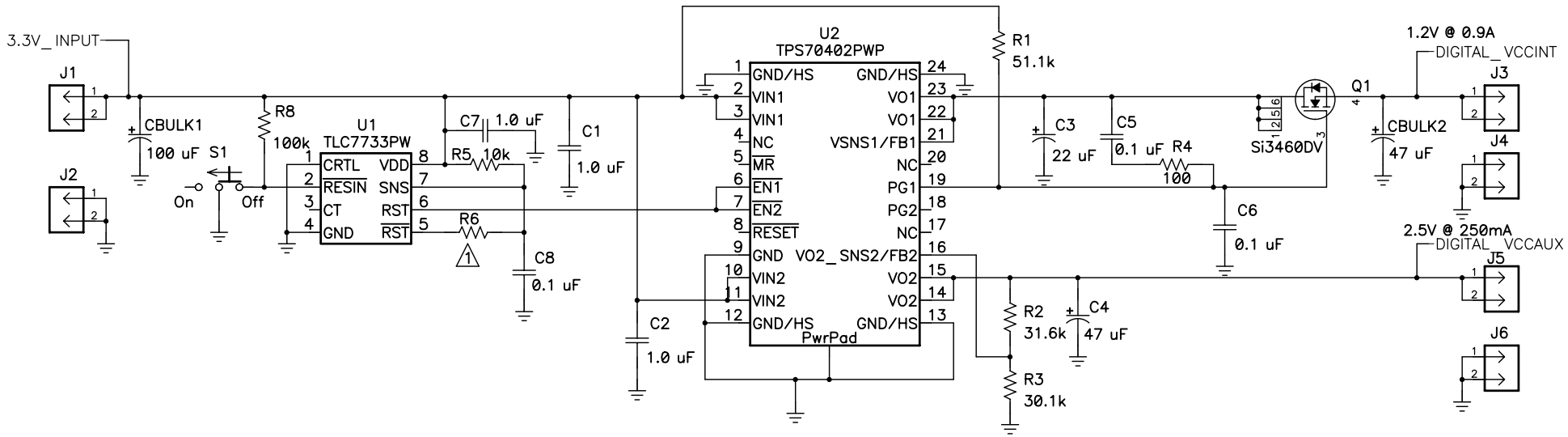
    As an example, with V_{IN} = 3.3 V, V_{CCINT} = 1.2V, V_{CCAUX} = 2.5 V, P_{Dmax} = 2 W and assuming that the $I_{CCAUXmax}$ = 250 mA:
    - I_{CCINT} max = $[P_{Dmax} - (V_{IN} - V_{CCAUX}) * I_{CCAUXmax}] / (V_{IN} - V_{CCINT})$
    - $I_{CCINTmax}$ = 857 mA
- **Soft Start Circuitry:**
  - NMOS transistor Q1 should be selected so that its threshold voltage, V_{TH}, is at least 0.9 V below V_{IN} or lower (e.g., $V_{TH} \leq 3.3\ V - 0.9\ V = 2.4\ V$). In addition, the transistor's R_{DSon} of Q1 should be low enough, when driven by V_{IN}, that the voltage drop across the transistor at maximum current (e.g., $I_{CCINTmax} * R_{DSon}$) does not cause V_{CCINT} to fall below its -5% tolerance.
  - The source of Q1 needs at least 10 uF of total capacitance in order for the soft-start circuit to work properly. The additional bulk bypass capacitance (not shown in the schematic) required for the V_{CCINT} rail of the FPGA will most likely meet this requirement.
- **Input Voltage Monitoring Circuit:**
  - The TLC770x SVS circuit is sensitive to the rise time and source impedance of the input power supply. If the input power supply rises slowly and has a high source impedance, the RESET and /RESET outputs may briefly toggle between high and low due to the point of load converter being enabled and pulling the input power supply down slightly, until the input voltage rises above the SVS's trip point. Therefore, the 1.0 uF capacitor, C7, should be placed as close as possible between VDD and GND. To further reduce the risk of this happening, a 10k ohm resistor (R5) from the VDD pin to the SNS pin and a 0.1 uF capacitor (C8 on R7 pad)) from the SNS pin to GND were added. The RC delay created by this capacitor and resistor prevents the SVS from tripping until the input supply is well above the internal trip point
- **Modifications:**
  - CT of TLC7733 is not connected, but can be used with a capacitor to add a delay between the 5V rail coming up and RST = /EN1=/EN2 of TPS70402.
  - Select the appropriate TLC77xx option to monitor the input supply voltage.
  - For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).

  - Note that with higher voltage input supplies, such as 5V, power dissipation in the linear regulator is of greater concern (see previously presented power dissipation calculations).

- **3.3V Configuration**
  - The Spartan-3 FPGA configuration and JTAG ports commonly use signals with a 2.5-V swing. Alternatively, it is possible to use 3.3-V signals simply by adding a few external resistors. The 3.3-V signals can cause a reverse current that flows from certain configurations and JTAG input pins, through the FPGA, to the V_{CCAUX} power rail. Therefore, please refer to application note SLVA159 http://focus.ti.com/lit/an/slva159a/slva159a.pdf for implementation guidance.

QUESTIONS?

- Send an email to **fpgasupport@list.ti.com**



Title	Dual LDO (TPS70402) Design	
Size: B	Number: HPA080	Rev: B
Date: 08/03/04		Drawn by:
Filename: hpa080b.sch		Sheet: of

Filename: HPA083A_bom.xls

Date: 06/22/2004

HPA083A BOM

COUNT	RefDes	DESCRIPTION	SIZE	MFR	PART NUMBER
2	C1, C5	Capacitor, Ceramic, 10-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J106KE01
2	C11, C12	Capacitor, Ceramic, 0.047-uF, 25-V, X7R, 10%	603	muRata	GRM188R71E473KA01
2	C13, C14	Capacitor, Ceramic, 3300-pF, 50-V, X7R, 10%	603	muRata	GRM188R71H332KA01
2	C15, C17	Capacitor, Ceramic, 27-pF, 50-V, C0G, 5%	603	muRata	GRM1885C1H270JA01D
2	C16, C18	Capacitor, Ceramic, 2700-pF, 50-V, X7R, 10%	603	muRata	GRM188R71H272KA01D
2	C19, C20	Capacitor, Ceramic, 22-uF, 10-V, X5R, 10%	1210	muRata	GRM32ER61A226KA65
2	C2, C4	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
2	C23, C24	Capacitor, Ceramic, 470-pF, 50-V, X7R, 10%	603	muRata	GRM188R71H471KA01
4	C3, C8, C21, C22	Capacitor,Tantalum, 330-uF, 6.3-V, 600-milliohm, 20%	7343(D)	Vishay	293D337X96R3D2
1	C6	Capacitor, Ceramic, 0.056-uF, 16-V, X7R, 10%	603	muRata	GRM188R71C563KC01
1	C7	Capacitor, Ceramic, 0.33-uF, 10-V, X5R, 10%	603	muRata	GRM188R61A334KA61
2	C9, C10	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J225KC01
8	J1 - J8	Header, 2-pin, 100mil spacing, (36-pin strip)	0.100 x 2	Sullins	PTC36SAAN
2	L1, L2	Inductor, SMT, 6.8-uH, 2.2-A, 75-milliohm	0.51x0.37	Coilcraft	DS3316P-682
3	R1, R2, R9	Resistor, Chip, 71.5k-Ohms, 1/16-W, 1%	603	Std	Std
2	R10, R11	Resistor, Chip, 30.1k-Ohms, 1/16-W, 1%	603	Std	Std
2	R12, R13	Resistor, Chip, 1.91k-Ohms, 1/16-W, 1%	603	Std	Std
3	R3, R14, R15	Resistor, Chip, 10k-Ohms, 1/16-W, 1%	603	Std	Std
1	R4	Resistor, Chip, 511k-Ohms, 1/16-W, 1%	603	Std	Std
2	R5, R6	Resistor, Chip, 2.4-Ohms, 1/8-W, 1%	1206	Std	Std
1	R7	Resistor, Chip, 28.7k-Ohms, 1/16-W, 1%	603	Std	Std
1	R8	Resistor, Chip, 3.74k-Ohms, 1/16-W, 1%	603	Std	Std
1	S1	Switch, 1P2T, Slide, PC-mount, 200-mA	79900	E_Switch	EG1218
1	U1	IC, Utralow-Noise, High PSRR, Fast RF 250 mA, LDO Linear Regulators, 2.5-V	MSOP-8	TI	TPS79425DGN
2	U2, U3	IC, SWIFT Power Controller, Adj-V, 1.5A	PWP20	TI	TPS54110PWP
1	--	PCB, 3.1 In x 2.4 In x .062 In		Any	HPA083

Notes:

1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants.
   Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted.
   All other components can be substituted with equivalent MFG's components.

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