



Section 1

Introduction

This document describes the AT89EVK-01 evaluation kit dedicated to the AT83C24 Smart Card Reader Interface IC. This board is designed to allow an easy evaluation of the AT83C24 on an application using the TDA8004.

This board can be connected on the TDA8004 footprint.

1.1 Features

The AT89EVK-01 provides the following features:

- Possibility to replace the TDA8004 (or TDA8024) with the AT89EVK-01 board . The AT89EVK-01 board is soldered on the TDA8004 footprint.
- The AT83C24 registers are programmed with the TWI link (SDA,SCL). The T89C5121 microcontroller sends the TWI commands to configure the AT83C24 registers.
- The configuration software is stored in T89C5121 Flash memory. The program can be reloaded by using FLIP / BatchISP (In-System Programming tool) and an RS-232 adaptor board (CEIBO for example).
- Hardware configuration allowed with switches and solder pads.
- The program can be modified and reloaded with Batchisp (see 2.2.2)



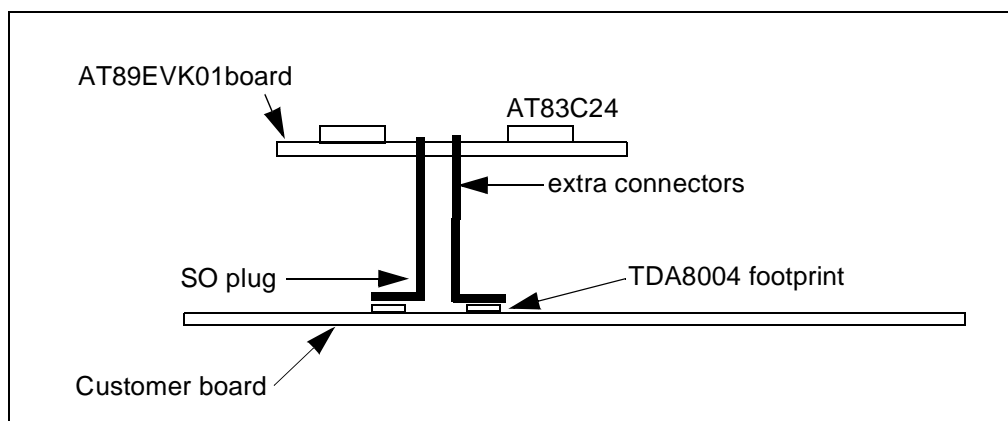
Hardware Description

2.1 TDA8004 Mode

2.1.1 Overview

The AT89EVK-01 board is soldered on the customer application by using the SO plug. If there is a problem to connect the AT89EVK-01 board on the SO plug, connectors can be added to lift the board.

Figure 2-1. General Description



Input signals of the TDA8004 footprint are connected to AT83C24.

Output signals of the TDA8004 footprint are provided by AT83C24.

The program stored in the Flash memory configures the AT83C24 registers once after the reset. The functionalities of the TDA8004 are provided by the AT83C24.

Remarks:

- The AT89EVK-01 board power supply comes from the TDA8004 footprint.
- The program stored in the Flash memory configures the AT83C24 registers once after the reset.

2.1.2 Clock signal (CLK)

The AT89EVK-01 board needs a clock signal. The AT89EVK-01 board needs a clock signal for T89C5121 (XTAL1 pin) and for AT83C24 (CLK pin).

Two solutions are proposed for the clock generation: waveform generator or crystal.

Figure 2-2. External Waveform Generator for Clock

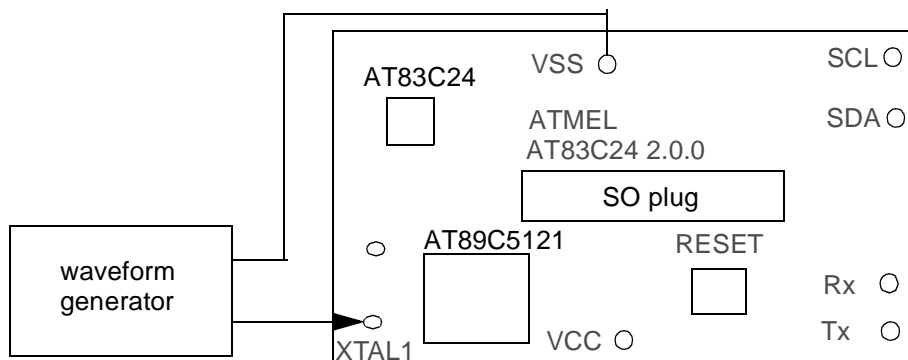
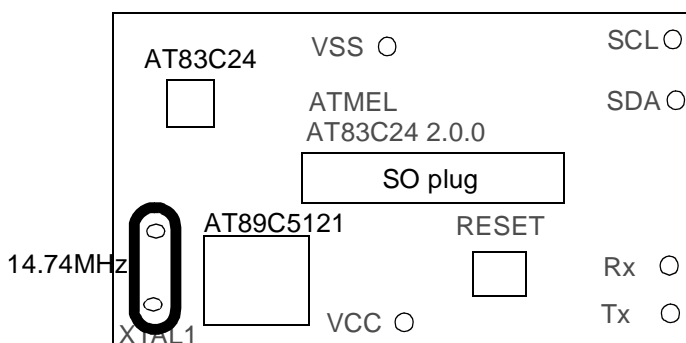


Figure 2-3. Crystal for Clock



A solder pad (SW4) is used to configure the source: crystal or external waveform generator.

Table 2-1. Clock Solder Pads Configuration

SW4	Configuration
without solder	Waveform generator
with solder	crystal

2.1.3 Smart Card Clock Signal (CCLK)

The AT83C24 outputs the smart card clock signal (CCLK). Two modes are available to generate this signal:

1. The source is CLK. The CKS prescaler is used to divide CLK signal or DCCLK signal.
2. The source is A2. The CKS prescaler is used to divide A2 signal.

2.1.4 Power Supply

The power supply comes from the TDA8004 footprint. The signal VDDP of the TDA8004 is used (5V).

The EVCC pin of the AT83C24 is connected to the VDD (3.3V). EVCC is used to supply the AT83C24 pads connected to the customer application.

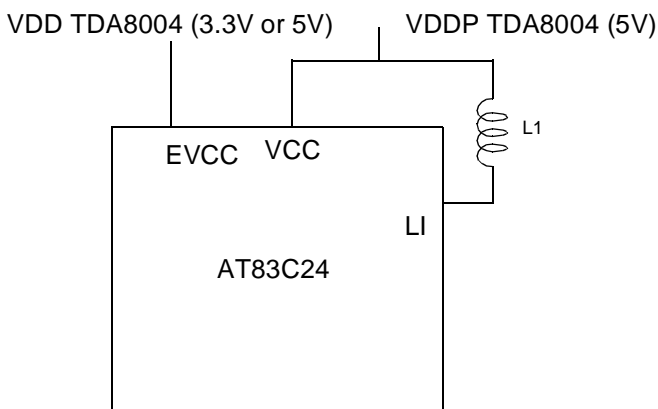
2.1.5 PRES, PRES

The TWI_SEL switch is connected on an I/O of the T89C5121. The TDA8004 (TDA8024) PRES pin and PRES\ pin are connected on T89C5121 I/Os. The position of



the TWI_SEL switch selects the polarity of the smart card presence: information on PRES or on PRES\ (see §2.1.8). See Figure 4-1 on page 16 for TWI_SEL selection.

Figure 2-4. Power Supply Configuration



Remark:

- VCC and L1 must be connected to the same voltage.

- 2.1.6 TWI Link** The TWI link is managed by T89C5121. The program stored in the Flash memory configures the AT83C24 registers once after the reset.
- The T89C5121 sends TWI commands. The AT83C24 TWI address depends on level on A2,A1,A0 pins at reset. The T89C5121 sends TWI commands at all addresses to avoid any problem of level on A2, A1, A0 at reset.
- 2.1.7 External TWI Link** If the user wants to use an external TWI source to configure the AT83C24, the 2 test points SCL and SDA are used.
- To avoid any conflict with T89C5121 signals, the T89C5121 software must check the SW2 signal before to send data on SCL and SDA.
- 2.1.8 Board configuration** The table below describes the switches and solder pads configurations.

Table 2-2. Configuration Description

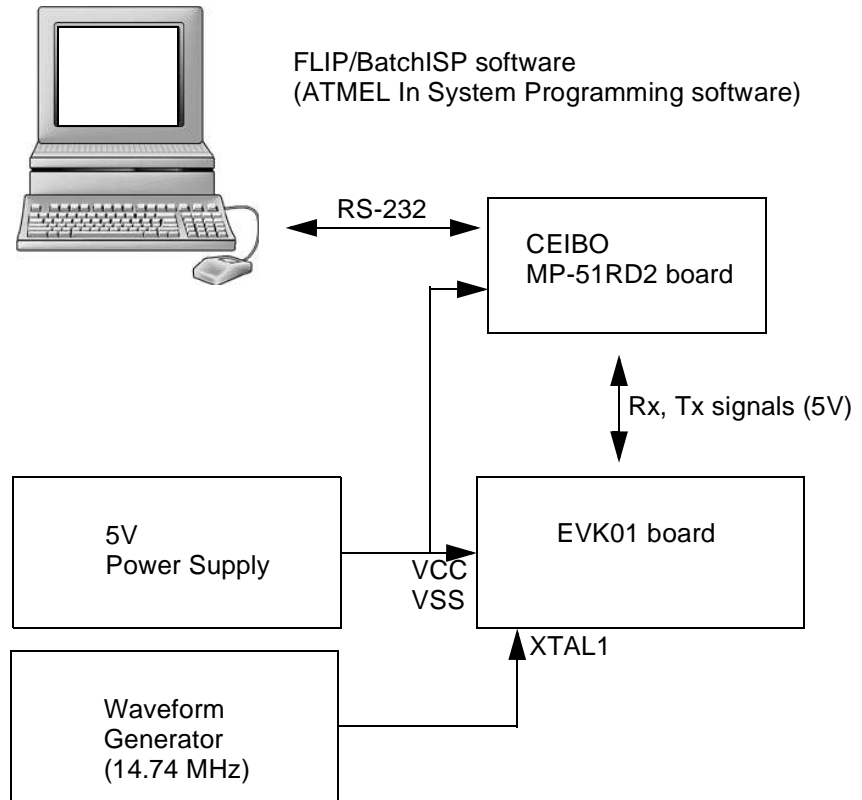
Solder pad or Switch	Default Configuration	Description
SW1	no solder	RFU (TDA8004AT)
SW2	TWI_SEL = 0	Smart card presence detection: TWI_SEL = 0: PRES indicates the smart card presence. TWI_SEL = 1: PRES\ indicates the smart card presence.
SW5		Reset button
SW4	with solder	Used for clock configuration (see §2.1.2)
SW9	solder	Used to connect TDA8004 clock on A2 (transparent mode). Use firmware from version 3 (at89evk01_V3.zip)
SW11	no solder	Used to connect a pull up resistor on RESET pin

2.2 T89C5121 Firmware Reconfiguration

The program stored in the T89C5121 (Flash version) sends TWI commands to configure the AT83C24 registers at each reset or power on.

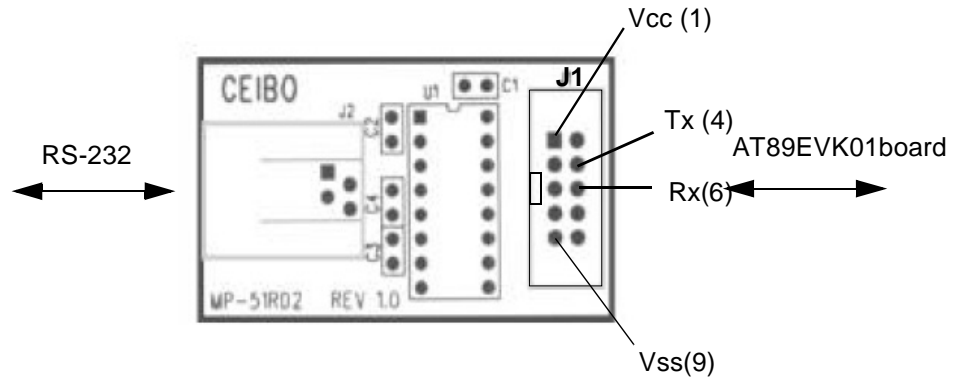
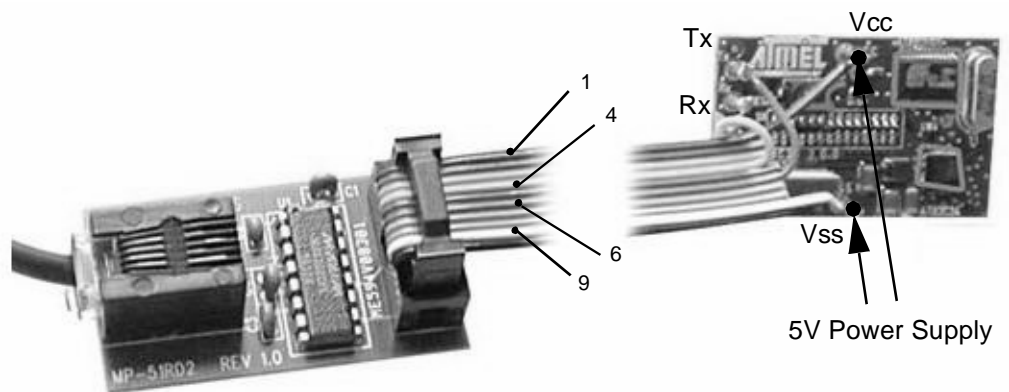
If the user wants to modify the AT83C24 configuration, it need to reprogram the T89C5121 Flash memory by using FLIP/BatchISP software (free download on www.atmel.com) as described below.

Figure 2-5. T89C5121 In System Programming Description



2.2.1 CEIBO MP-51RD2 Programmer

The CEIBO “MP-51RD2 Programmer” board is used to interface the RS-232 and the Rx Tx pins of the T89C5121. This board makes the electrical interface between microcontroller signals (5V) and RS-232 signals (12V).

Figure 2-6. CEIBO “MP-51RD2 Programmer” Board and J1 connector**Figure 2-7.** CEIBO “MP-51RD2 Programmer” Board and AT89EVK-01 connections

2.2.2 AT83C24 registers programming

The Flash memory of the T89C5121 is loaded with FLIP/BatchISP if a new configuration is needed for the AT83C24.

1. Unzip the AT89EVK01_Vx.zip (x : version)

This zip file contains 3 files :

- AT83C24_batchisp.hex : T89C5121 firmware file
 - at89evk01.bat : DOS command file
 - AT83C24_batchisp_prog.txt : script file for batchisp software
2. Copy all files at C:\Program Files\ATMEL\FLIP x.x.x\bin
 3. Connect the external waveform generator - Frequency at 14.74MHz or solder SW4
 4. Connect the RS232C cable to PC serial port
 5. Connect power supply to the AT89EVK-01 board
 6. Switch on the power supply
 7. Execute at89evk01.bat

Figure 2-8. Execution of at89evk01.bat (V1.0)

```

C:\Program Files\ATMEL\FLIP 2.2.2\bin>at89evk01
C:\Program Files\ATMEL\FLIP 2.2.2\bin>batchisp -cmdfile "AT83C24_batchisp_prog.t
xt"
Running batchisp 0.0.9 on Thu Feb 26 14:54:23 2004

T8XC5121 - RS232 - COM1 - 19200

Device selection..... PASS
Hardware selection..... PASS
Opening port..... PASS
Synchronizing target..... PASS
Reading Bootloader version..... PASS      1.2.0
Parsing HEX file..... PASS      AT83C24_batchisp.hex
Erasing..... PASS
Setting Address Range..... PASS      0x026D  0x026D
Filling buffer..... PASS      0x026D  0x026D  0x80
Setting Address Range..... PASS      0x026E  0x026E
Filling buffer..... PASS      0x026E  0x026E  0x0A
Setting Address Range..... PASS      0x026F  0x026F
Filling buffer..... PASS      0x026F  0x026F  0x00
Setting Address Range..... PASS      0x0270  0x0270
Filling buffer..... PASS      0x0270  0x0270  0x80
Setting Address Range..... PASS      0x0271  0x0271
Filling buffer..... PASS      0x0271  0x0271  0x0B
Setting Address Range..... PASS      0x0272  0x0272
Filling buffer..... PASS      0x0272  0x0272  0x00
Setting Address Range..... PASS      0x3FFD  0x3FFD
Filling buffer..... PASS      0x3FFD  0x3FFD  0x7F
Programming memory..... PASS
Verifying memory..... PASS      0x3FFD  0x3FFD
Starting Application..... PASS

Summary:  Total 24  Passed 24  Failed 0
C:\Program Files\ATMEL\FLIP 2.2.2\bin>

```


Figure 2-9. FLIP/BatchISP command script file AT83C24_batchisp_prog.txt (V1.0)

```

#      Config 0
      addrange      0x026D 0x026D
      fillbuffer    (0x80)

#      Config 1
      addrange      0x026E 0x026E
      fillbuffer    (0x0A)

#      Config 2
      addrange      0x026F 0x026F
      fillbuffer    (0x00)

#      Config 3
      addrange      0x0270 0x0270
      fillbuffer    (0x80)

#      Config 4
      addrange      0x0271 0x0271
      fillbuffer    (0x0B)

#      Interface
      addrange      0x0272 0x0272
      fillbuffer    (0x00)

```

Following the application need, the AT83C24 registers can be changed. Only the value of fillbuffer FLIP/BatchISP commands has to be modified. By default values of AT83C24 registers are:

Table 2-3. AT83C24 register address and default value

Register Name	Address	Default Values V1.0	Default Values V2.0	Default Values V3.0 ⁽¹⁾	Comments
Config0	0x26D	0x80	0x80	0x80	
Config1	0x26E	0x0A	0x0A	0x0A	
Config2	0x26F	0x00	0x24	0x24	Note: For Smart Card Clock frequency of AT83C24 at 4.5MHz, XTAL1 must be set at 4.5MHz - V1.0
Config3	0x270	0x80	0x80	0x80	
Config4	0x271	0x0B	0x0B	0x0B	
Interface	0x272	0x00	0x00	0x00	

Note: 1. Default values are included in hex file







Section 3

Software Description

3.1 AT83C24 Description

3.1.1 Overview The AT83C24 is a smart card reader IC. A TWI bus is used to configure the AT83C24. On the AT89EVK-01 board, the T89C5121 controls the TWI link.

After a reset, the T89C5121 sends commands to write values in AT83C24 registers.

3.1.2 TWI Address The address byte is sampled on A2, A1, A0 after each reset. The address is then:

A2	A1	A0	Address Byte for Read Command	Address Byte for Write Command
0	0	0	0x41	0x40
0	0	1	0x43	0x42
0	1	0	0x45	0x44
0	1	1	0x47	0x46
1	0	0	0x49	0x48
1	0	1	0x4B	0x4A
1	1	0	0x4D	0x4C
1	1	1	0x4F	0x4E

The level on A2, A1 and A0 are not stable on all applications. To avoid any problem, the software sends each command to all addresses. One command is transformed in 8 commands.

3.1.3 AT83C24 Registers The AT83C24 has 11 registers:
CONFIG0, CONFIG1, CONFIG2, CONFIG3, CONFIG4, INTERFACE, STATUS
TIMER1, TIMER0, CAPTURE0, CAPTURE1.

Several commands are used to write in AT83C24 registers.

Table 3-1. Write Commands Description

	Address Byte (See Table 2)	Command Byte	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4
Reset	0100 XXX0	1111 1111				
Write config	0100 XXX0	(10 + CONFIG0 6 bits)	CONFIG1	CONFIG2	CONFIG3	CONFIG4
Write Timer	0100 XXX0	1111 1100	TIMER1	TIMER0		
Write Interface	0100 XXX0	(0+INTERFACE 7 bits)				
General Call Reset	0000 0000	0000 0110				



Section 4

Schematics

Figure 4-1. Component Side

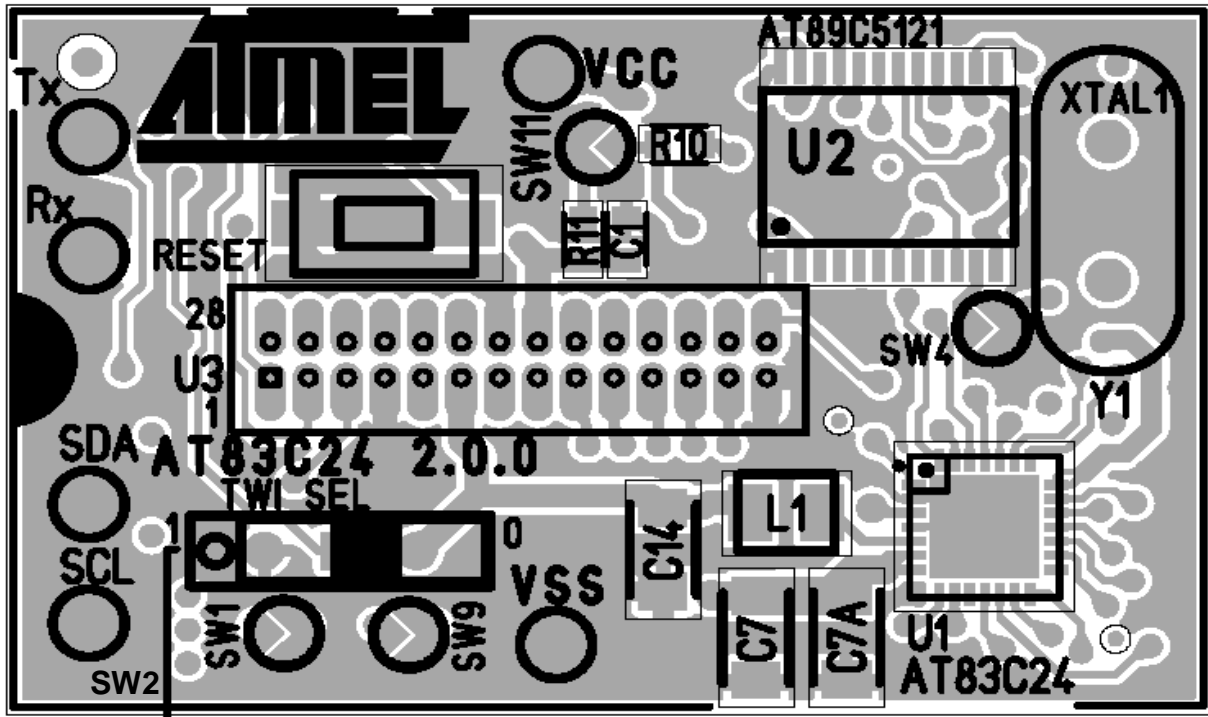


Figure 4-2. Solder Side

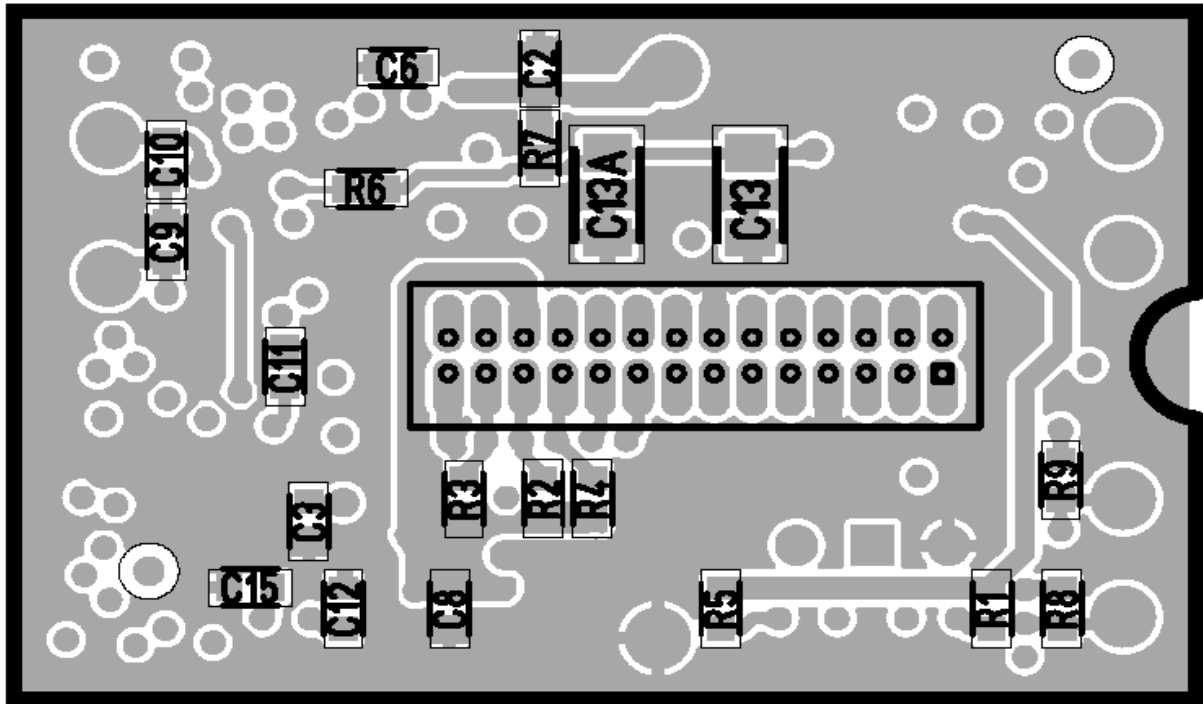


Table 4-1. Bill of materials

Reference	Part	Part Description
C10	22 pF	50V-5% Ceramic Capacitor
C12	30 pF	
C13	10 μ F	16V +/-20%
C14	4.7 μ F	25V
C15	30 pF	
C1, C2, C3, C6, C8, C11	100 nF	50V-5% Ceramic Capacitor
C7, C7A	4.7 μ F	25V
C9	22 pF	50V-5% Ceramic Capacitor
L1	4.7 μ H	20% Inductance 450 mA SMD Murata LQH32CN4R7M33L
R2, R4, R3, R10, R11	100 K	1/16W-5% Resistor SMD
R1, R5, R7, R8, R9	10 K	1/16W-5% Resistor SMD
R6	1 K	1/16W-5% Resistor SMD
U1	AT83C24QFN	
U2	AT89C5121/SSOP24	
U3	CONNECTOR	
Y1	Crystal 14,74 MHz	



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