CDCEx937-Q1 Programmable 3-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V LVCMOS Outputs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- In-System Programmability and EEPROM
  - Serial Programmable Volatile Register
  - Nonvolatile EEPROM to Store Customer Setting
- Flexible Input Clocking Concept
  - External Crystal: 8 MHz to 32 MHz
  - On-Chip VCXO: Pull Range ±150 ppm
  - Single-Ended LVCMOS up to 160 MHz
- Free Selectable Output Frequency up to 230 MHz
- Low-Noise PLL Core
  - Integrated PLL Loop Filter Components
  - Low Period Jitter (Typical 60 ps)
- Separate Output Supply Pins
  - CDCE937-Q1: 3.3 V and 2.5 V
  - CDCEL937-Q1: 1.8 V
- Flexible Clock Driver
  - Three User-Definable Control Inputs [S0/S1/S2]; for Example: SSC Selection, Frequency Switching, Output Enable or Power Down
  - Generates Highly Accurate Clocks for Video, Audio, USB, IEEE1394, RFID, Bluetooth™, WLAN, Ethernet™, and GPS
  - Generates Common Clock Frequencies Used With TI-DaVinci™, OMAP™, DSPs
  - Programmable SSC Modulation
  - Enables 0-PPM Clock Generation
- 1.8-V Device Power Supply
- Wide Temperature Range –40°C to 125°C
- Packaged in TSSOP
- Development and Programming Kit for Easy PLL Design and Programming (TI Pro-Clock™)

2 Applications

- Clusters
- Head Units
- Navigation Systems
- Advanced Driver Assistance Systems (ADAS)

3 Description

The CDCE937-Q1 and CDCEL937-Q1 devices are modular, phase-locked loop (PLL) based programmable clock synthesizers. These devices provide flexible and programmable options, such as output clocks, input signals, and control pins, so that the user can configure the CDCEx937-Q1 for their own specifications.

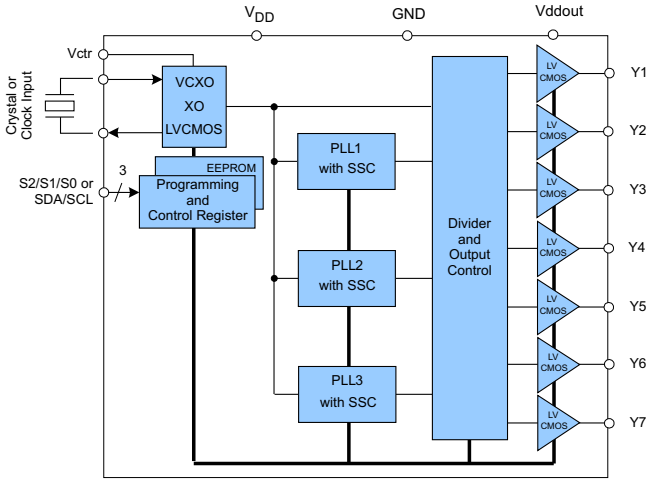
The CDCEx937-Q1 generates up to seven output clocks from a single input frequency to enable both board space and cost savings. Additionally, with multiple outputs, the clock generator can replace multiple crystals with one clock generator. This makes the device well-suited for head unit and telematics applications in infotainment and camera systems in ADAS as these platforms are evolving into smaller and more cost effective systems.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCE937-Q1, CDCEL937-Q1	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2010) to Revision C **Page**

- Changed *Applications* ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet ... 1

Changes from Revision A (March 2010) to Revision B **Page**

- Changed the PACKAGE THERMAL RESISTANCE table ... 6
- Changed RID default in *Generic Configuration Register* table From: 0h To: Xb ... 18
- Added note to PWDN description in *Generic Configuration Register* table ... 18
- Changed SLAVE_ADR default value in *Generic Configuration Register* table From: 00b To: 01b ... 18

5 Description (continued)

Furthermore, each output can be programmed in-system for any clock frequency up to 230 MHz through the integrated, configurable PLL. The PLL also supports spread-spectrum clocking (SSC) with programmable down and center spread. This provides better electromagnetic interference (EMI) performance to enable customers to pass industry standards such as CISPR-25.

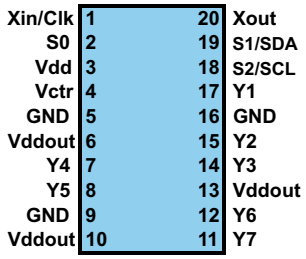
Customization of frequency programming and SSC are accessed using three user-defined control pins. This eliminates the additional interface requirement to control the clock. Specific power-up and power-down sequences can also be defined to the user's needs.

6 Device Comparison Table

DEVICE	SUPPLY (V)	PLL	OUTPUT
CDCE913-Q1	2.5 to 3.3	1	3
CDCEL913-Q1	1.8	1	3
CDCE937-Q1	2.5 to 3.3	3	7
CDCEL937-Q1	1.8	3	7
CDCE949-Q1	2.5 to 3.3	4	9
CDCEL949-Q1	1.8	4	9

7 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	Xin/CLK	I	Crystal oscillator input or LVCMOS clock input (selectable through SDA and SCL bus)
2	S0	I	User-programmable control input S0; LVCMOS inputs; Internal pullup 500 k
3	V_{DD}	P	1.8-V power supply for the device
4	V_{Ctrl}	I	VCXO control voltage (leave open or pull up to approximately 500 k when not used)
5	GND	G	Ground
6	Vddout	P	CDCE937-Q1: 3.3-V or 2.5-V supply for all outputs CDCEL937-Q1: 1.8-V supply for all outputs
7	Y4	O	LVCMOS outputs
8	Y5	O	LVCMOS outputs
9	GND	G	Ground
10	Vddout	P	CDCE937-Q1: 3.3-V or 2.5-V supply for all outputs CDCEL937-Q1: 1.8-V supply for all outputs
11	Y7	O	LVCMOS outputs
12	Y6	O	LVCMOS outputs
13	Vddout	P	CDCE937-Q1: 3.3-V or 2.5-V supply for all outputs CDCEL937-Q1: 1.8-V supply for all outputs
14	Y3	O	LVCMOS outputs
15	Y2	O	LVCMOS outputs
16	GND	G	Ground
17	Y1	O	LVCMOS outputs
18	SCL/S2	I	SCL: serial clock input(default configuration), LVCMOS internal pullup 500 k; or S2: user-programmable control input, LVCMOS inputs, and internal pullup 500 k
19	SDA/S1	I/O or I	SDA: bidirectional serial data input/output (default configuration). LVCMOS internal pullup 500 k; or S1: user-programmable control input, LVCMOS inputs, and internal pullup 500 k
20	Xout	O	Crystal oscillator output (leave open or pull up to approximately 500 k when not used)

(1) G = Ground, I = Input, O = Output, P = Power

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{DD}	–0.5	2.5	V
Input voltage, V_I(2)(3)	–0.5	V_{DD} + 0.5	V
Output voltage, V_O(2)	–0.5	Vddout + 0.5	V
Input current, I_I (V_I < 0 and V_I > V_{DD})		20	mA
Continuous output current, I_O		50	mA
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) SDA and SCL can go up to 3.6 V as stated in the *Recommended Operating Conditions*.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage		1.7	1.8	1.9	V
V_O	Output Yx supply voltage, Vddout	CDCE937-Q1	2.3		3.6	V
		CDCEL937-Q1	1.7		1.9	
V_{IL}	Low-level input voltage LVCMOS				0.3 × V_{DD}	V
V_{IH}	High-level input voltage LVCMOS		0.7 × V_{DD}			V
$V_{I(thresh)}$	Input voltage threshold LVCMOS			0.5 × V_{DD}		V
V_{IS}	Input voltage	S0	0		1.9	V
		S1, S2, SDA, SCL; $V_{I(thresh)}$ = 0.5 V_{DD}	0		3.6	
$V_{I(CLK)}$	Input voltage range CLK		0		1.9	V
I_{OH} /I_{OL}	Output current	Vddout = 3.3 V			±12	mA
		Vddout = 2.5 V			±10	
		Vddout = 1.8 V			±8	
C_L	Output load LVCMOS				10	pF
T_A	Ambient temperature		–40		125	°C
CRYSTAL/VCXO(1)						
f_{Xtal}	Crystal input frequency (fundamental mode)		8	27	32	MHz
ESR	Effective series resistance				100	Ω
f_{PR}	Pulling range (0 V ≤ Vctrl ≤ 1.8 V)(2)		±120	±150		ppm
Vctrl	Frequency control voltage		0		V_{DD}	V
C_0/C_1	Pullability ratio				220	
C_L	On-chip load capacitance at Xin and Xout		0		20	pF

(1) For more information about VCXO configuration and crystal recommendation, see *VCXO Application Guideline for CDCE(L)9xx Family* (SCAA085).
(2) Pulling range depends on crystal-type, on-chip crystal load capacitance and PCB stray capacitance; pulling range of min ± 120 ppm applies for crystal listed in *VCXO Application Guideline for CDCE(L)9xx Family* (SCAA085).

8.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)(1)

THERMAL METRIC(2)			CDCE937-Q1, CDCEL937-Q1 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Airflow = 0 lfm	89	°C/W
		Airflow = 150 lfm	75	
		Airflow = 200 lfm	74	
		Airflow = 250 lfm	74	
		Airflow = 500 lfm	69	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		31	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		55	°C/W
ψ_{JT}	Junction-to-top characterization parameter		0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter		49	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		—	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

8.5 Electrical Characteristics

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{DD}	Supply current (see Figure 1)	All outputs off, $f_{(CLK)}$ = 27 MHz, $f_{(VCO)}$ = 135 MHz	All PLLS on		29		mA
			Per PLL		9		
I_{DDOUT}	Output supply current (see Figure 2)	No load, all outputs on, f_{OUT} = 27 MHz	CDCE937, V_{DDOUT} = 3.3 V		3.1		mA
			CDCEL937, V_{DDOUT} = 1.8 V		1.5		
$I_{DD(PD)}$	Power-down current	Every circuit powered down except SDA and SCL, f_{IN} = 0 MHz, V_{DD} = 1.9 V			50		µA
$V_{(PUC)}$	Supply voltage Vdd threshold for power-up control circuit			0.85		1.45	V
$f_{(VCO)}$	VCO frequency range of PLL			80		230	MHz
f_{OUT}	LVCMOS output frequency	Vddout = 3.3 V		230			MHz
		Vddout = 1.8 V		230			
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7 V, I_I = –18 mA				–1.2	V
I_I	LVCMOS input current	VI = 0 V or V_{DD}, V_{DD} = 1.9 V				±5	µA
I_{IH}	LVCMOS input current for S0/S1/S2	V_I = V_{DD}, V_{DD} = 1.9 V				5	µA
I_{IL}	LVCMOS input current for S0/S1/S2	V_I = 0 V, V_{DD} = 1.9 V				–6	µA
C_I	Input capacitance at Xin/Clk	$V_{I(Clk)}$ = 0 V or V_{DD}			6		pF
	Input capacitance at Xout	$V_{I(Xout)}$ = 0 V or V_{DD}			2		
	Input capacitance at S0/S1/S2	V_{IS} = 0 V or V_{DD}			3		
LVCMOS PARAMETER, Vddout = 3.3 V (CDCE937)							
V_{OH}	LVCMOS high-level output voltage	Vddout = 3 V, I_{OH} = –0.1 mA		2.9			V
		Vddout = 3 V, I_{OH} = –8 mA		2.4			
		Vddout = 3 V, I_{OH} = –12 mA		2.2			
V_{OL}	LVCMOS low-level output voltage	Vddout = 3 V, I_{OL} = 0.1 mA				0.1	V
		Vddout = 3 V, I_{OL} = 8 mA				0.5	
		Vddout = 3 V, I_{OL} = 12 mA				0.8	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass			3.2		ns
t_r/t_f	Rise and fall time	Vddout= 3.3 V (20%–80%)			0.6		ns

(1) All typical values are at respective nominal V_{DD}.

Electrical Characteristics (continued)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3		60	90	ps
		3 PLL switching, Y2-to-Y7		100	150	
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3		70	100	ps
		3 PLL switching, Y2-to-Y7		120	180	
$t_{sk(o)}$	Output skew (see Table 2)(4)	f_{OUT} = 50 MHz, Y1-to-Y3			60	ps
		f_{OUT} = 50 MHz, Y2-to-Y5			160	
odc	Output duty cycle(5)	f_{VCO} = 100 MHz, Pdiv = 1	45%		55%	
LVCMOS PARAMETER, Vddout = 2.5 V (CDCE937)						
V_{OH}	LVCMOS high-level output voltage	Vddout = 2.3 V, I_{OH} = –0.1 mA	2.2			V
		Vddout = 2.3 V, I_{OH} = –6 mA	1.7			
		Vddout = 2.3 V, I_{OH} = –10 mA	1.6			
V_{OL}	LVCMOS low-level output voltage	Vddout = 2.3 V, I_{OL} = 0.1 mA			0.1	V
		Vddout = 2.3 V, I_{OL} = 6 mA			0.5	
		Vddout = 2.3 V, I_{OL} = 10 mA			0.7	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		3.4		ns
t_r/t_f	Rise and fall time	Vddout = 2.5 V (20%–80%)		0.8		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3		60	90	ps
		3 PLL switching, Y2-to-Y7		100	150	
$t_{jit(per)}$	Peak-to-peak period jitter(4)	1 PLL switching, Y2-to-Y3		70	100	ps
		3 PLL switching, Y2-to-Y7		120	180	
$t_{sk(o)}$	Output skew (see Table 2)(4)	f_{OUT} = 50 MHz, Y1-to-Y3			60	ps
		f_{OUT} = 50 MHz, Y2-to-Y5			160	
odc	Output duty cycle(5)	$f_{(VCO)}$ = 100 MHz, Pdiv = 1	45%		55%	
LVCMOS PARAMETER, Vddout = 1.8 V (CDCEL937)						
V_{OH}	LVCMOS high-level output voltage	Vddout = 1.7 V, I_{OH} = –0.1 mA	1.6			V
		Vddout = 1.7 V, I_{OH} = –4 mA	1.4			
		Vddout = 1.7 V, I_{OH} = –8 mA	1.1			
V_{OL}	LVCMOS low-level output voltage	Vddout = 1.7 V, I_{OL} = 0.1 mA			0.1	V
		Vddout = 1.7 V, I_{OL} = 4 mA			0.3	
		Vddout = 1.7 V, I_{OL} = 8 mA			0.6	
t_{PLH}, t_{PHL}	Propagation delay	All PLL bypass		2.6		ns
t_r/t_f	Rise and fall time	Vddout= 1.8 V (20%–80%)		0.7		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3		70	120	ps
		3 PLL switching, Y2-to-Y7		100	150	
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3		90	140	ps
		3 PLL switching, Y2-to-Y7		120	190	
$t_{sk(o)}$	Output skew (see Table 2)(4)	f_{OUT} = 50 MHz, Y1-to-Y3			60	ps
		f_{OUT} = 50 MHz, Y2-to-Y5			160	
odc	Output duty cycle(5)	$f_{(VCO)}$ = 100 MHz, Pdiv = 1	45%		55%	
SDA and SCL PARAMETER						
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7 V, I_I = –18 mA			–1.2	V
I_{IH}	SCL and SDA input current	V_I = V_{DD}, V_{DD} = 1.9 V			±10	µA
V_{IH}	SDA and SCL input high voltage(6)		0.7 × V_{DD}			V

(2) 10000 cycles.
(3) Jitter depends on configuration. Data is taken under the following conditions: 1-PLL : f_{IN} = 27MHz, Y2/3 = 27 MHz, (measured at Y2), 3-PLL: f_{IN} = 27 MHz, Y2/3 = 27 MHz (measured at Y2), Y4/5 = 16.384 MHz, Y6/7 = 74.25 MHz
(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and outputs are generated from the same divider; data taking on rising edge (tr).
(5) odc depends on output rise and fall time (t_r / t_f).
(6) SDA and SCL pins are 3.3 V tolerant.

Electrical Characteristics (continued)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IL}	SDA and SCL input low voltage(6)				0.3 × V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3 mA, V_{DD} = 1.7 V			0.2 × V_{DD}	V
C_I	SCL/SDA Input capacitance	V_I = 0 V or V_{DD}		3	10	pF
EEPROM						
EEcyc	Programming cycles of EEPROM		1000			cycles
EEret	Data retention		10			years

8.6 Timing Requirements

over recommended ranges of supply voltage, load, and operating ambient temperature (see Figure 12)

			MIN	NOM	MAX	UNIT
CLK_IN						
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0		160	MHz
		PLL mode	8		160	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
$duty_{CLK}$	Duty cycle CLK at V_{DD}/2		40%		60%	
SDA and SCL						
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
$t_{su(START)}$	START setup time (SCL high before SDA low)	Standard mode	4.7			µs
		Fast mode	0.6			
$t_{h(START)}$	START hold time (SCL low after SDA low)	Standard mode	4			µs
		Fast mode	0.6			
$t_{w(SCLL)}$	SCL low-pulse duration	Standard mode	4.7			µs
		Fast mode	1.3			
$t_{w(SCLH)}$	SCL high-pulse duration	Standard mode	4			µs
		Fast mode	0.6			
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
$t_{su(SDA)}$	SDA setup time	Standard mode	250			ns
		Fast mode	100			
t_r	SCL/SDA input rise time	Standard mode			1000	ns
		Fast mode			300	
t_f	SCL/SDA input fall time, standard mode and fast mode				300	ns
$t_{su(STOP)}$	STOP setup time	Standard mode	4			µs
		Fast mode	0.6			
t_{BUS}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			

8.7 Typical Characteristics

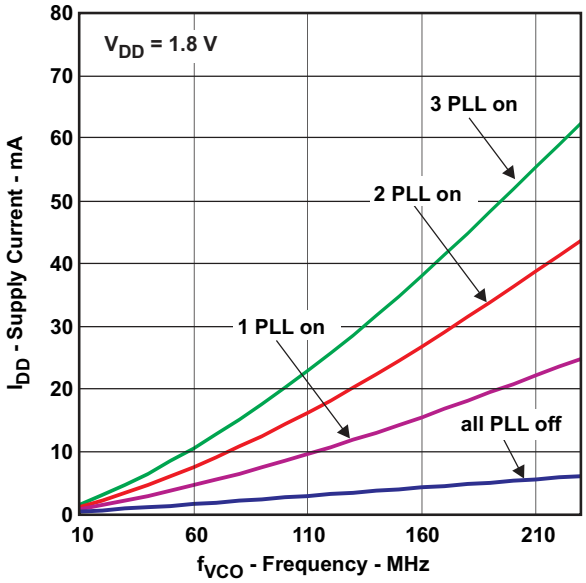


Figure 1. CDCEx937-Q1 Supply Current vs PLL Frequency

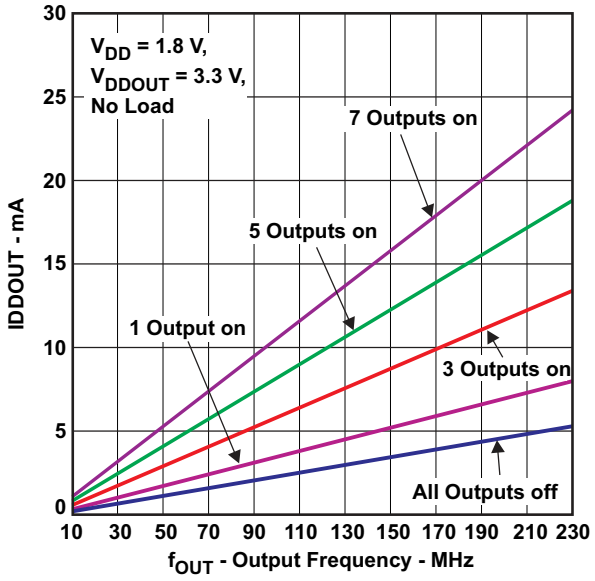


Figure 2. CDCE937-Q1 Output Current vs Output Frequency

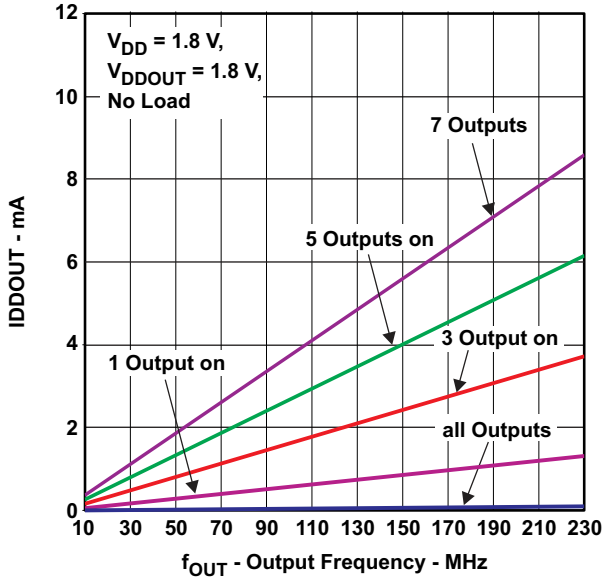


Figure 3. CDCEL937-Q1 Output Current vs Output Frequency

9 Parameter Measurement Information

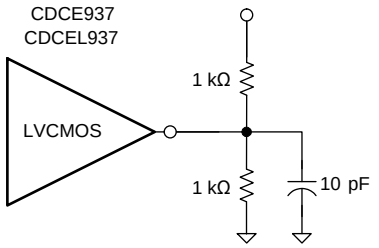


Figure 4. Test Load

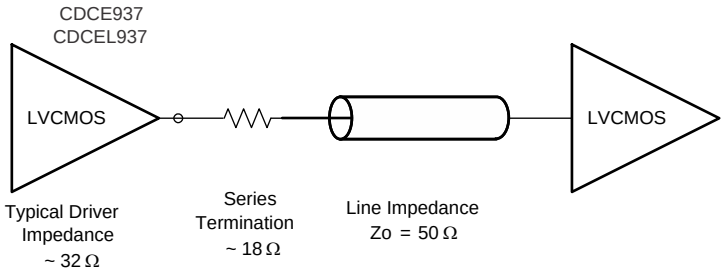


Figure 5. Test Load for 50-Ω Board Environment

10 Detailed Description

10.1 Overview

The CDCE937-Q1 and CDCEL937-Q1 devices are modular PLL-based low-cost high-performance programmable clock synthesizers, multipliers, and dividers. It generates up to seven output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using up to three independent configurable PLLs.

The CDCEx937-Q1 has separate output supply pins, VDDOUT, which is 1.8 V for CDCEL937-Q1 and from 2.5 V to 3.3 V for CDCE937-Q1.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 pF to 20 pF. Additionally, an on-chip VCXO is selectable which allows synchronization of the output frequency to an external control signal (that is, PWM signal).

The deep M/N divider ratio allows the generation of zero ppm audio or video, networking (WLAN, Bluetooth, Ethernet, GPS) or Interface (USB, IEEE1394, Memory Stick) clocks from a reference input frequency such as 27 MHz.

All PLLs supports SSC (spread-spectrum clocking). SSC can be center-spread or down-spread clocking which is a common technique to reduce electro-magnetic interference (EMI).

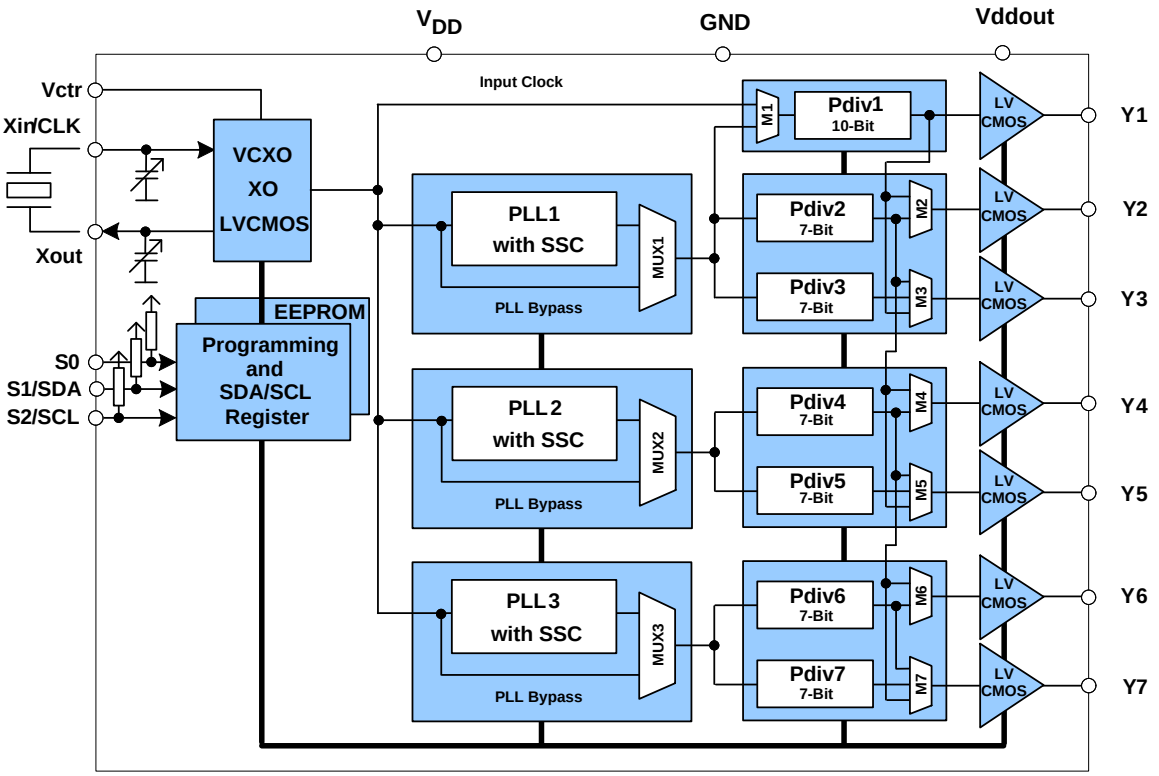
Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristic of each PLL.

The device supports non-volatile EEPROM programming for ease-customized application. It is preset to a factory default configuration (see *Default Device Setting*). It can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through SDA and SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1 and S2, can be used to control various aspects of operation including frequency selection changing the SSC parameters to lower EMI, PLL bypass, power down, and choosing between low level or 3-state for output-disable function.

The CDCEx937-Q1 operates in 1.8-V environment. It is characterized for operation from –40°C to 125°C.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Control Terminal Setting

The CDCEx937-Q1 has three user-definable control terminals (S0, S1, and S2) that allow external control of device settings. They can be programmed to any of the following setting:

- Spread spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power down control

The user can predefine up to eight different control settings. Table 1 and Table 2 explain these settings.

Table 1. Control Terminal Definition

EXTERNAL CONTROL BITS	PLL1 SETTING			PLL2 SETTING			PLL3 SETTING			Y1 SETTING
Control Function	PLL Frequency Selection	SSC Selection	Output Y2/Y3 Selection	PLL Frequency Selection	SSC Selection	Output Y4/Y5 Selection	PLL Frequency Selection	SSC Selection	Output Y6/Y7 Selection	Output Y1 and Power-Down Selection

Table 2. PLLx Setting (Can Be Selected For Each PLL Individual)(1)

SSC SELECTION (CENTER/DOWN)				
SSCx [3-BITS]			CENTER	DOWN
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	–0.25%
0	1	0	±0.5%	–0.5%
0	1	1	±0.75%	–0.75%
1	0	0	±1.0%	–1.0%
1	0	1	±1.25%	–1.25%
1	1	0	±1.5%	–1.5%
1	1	1	±2.0%	–2.0%
FREQUENCY SELECTION(2)				
FSx			FUNCTION	
0			Frequency0	
1			Frequency1	
OUTPUT SELECTION(3) (Y2 ... Y7)				
YxYx			FUNCTION	
0			State0	
1			State1	

(1) Center/Down-Spread, Frequency0/1 and State0/1 are user-definable in PLLx Configuration Register;
(2) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.
(3) State0/1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low or active

Table 3. Y1 Setting(1)

Y1 SELECTION	
Y1	FUNCTION
0	State 0
1	State 1

(1) State0 and State1 are user definable in Generic Configuration Register and can be power down, 3-state, low, or active.

S1/SDA and S2/SCL pins of the CDCEx937-Q1 are dual function pins. In default configuration they are defined as SDA and SCL for the serial interface. They can be programmed as control-pins (S1/S2) by setting the relevant bits in the EEPROM. Note that the changes to the Control register (Bit [6] of Byte [02]) have no effect until they are written into the EEPROM.

Once they are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control-pins, S1 and S2, temporally act as serial programming pins (SDA and SCL).

S0 is not a multi-use pin, it is a control pin only.

10.3.2 Default Device Setting

The internal EEPROM of CDCEx937-Q1 is preconfigured as shown in Figure 6. The input frequency is passed through to the output as a default. This allows the device to operate in default mode without the extra production step of program it. The default setting appears after power is supplied or after power-down or power-up sequence until it is re-programmed by the user to a different application configuration. A new register setting is programmed through the serial SDA and SCL interface.

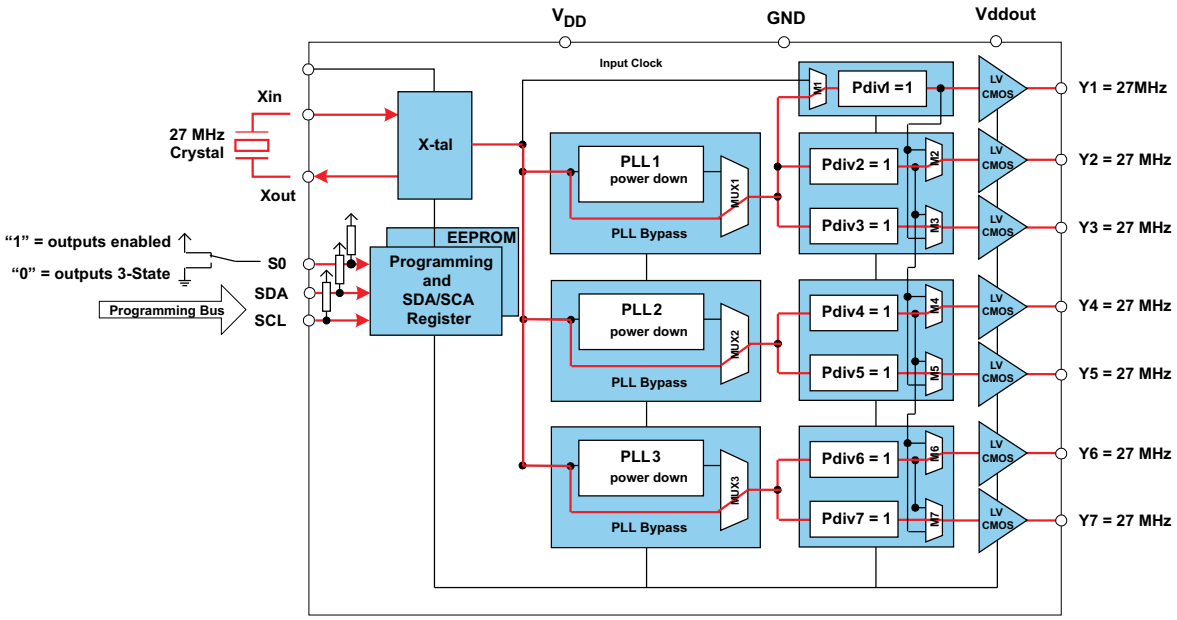


Figure 6. Default Device Setting

Table 4 shows the factory default setting for the Control Terminal Register (external control pins). In normal operation, all 8 register settings are available, but in the default configuration only the first two settings (0 and 1) can be selected with S0, as S1 and S2 configured as programming pins in default mode.

Table 4. Factory Default Setting for Control Terminal Register(1)

			Y1	PLL1 SETTINGS			PLL2 SETTINGS			PLL3 SETTINGS		
EXTERNAL CONTROL PINS			OUTPUT SELECT	FREQ. SELECT	SSC SELECT	OUTPUT SELECT	FREQ. SELECT	SSC SELECT	OUTPUT SELECT	FREQ. SELECT	SSC SELECT	OUTPUT SELECT
S2	*S1*	S0	Y1	*FS1*	*SSC1*	Y2Y3	*FS2*	*SSC2*	Y4Y5	*FS3*	*SSC3*	Y6Y7
SCL (I^2C)	SDA (I^2C)	0	*3-state*	f_{VCO1_0}	off	*3-state*	f_{VCO2_0}	off	*3-state*	f_{VCO1_0}	off	*3-state*
SCL (I^2C)	SDA (I^2C)	1	*Enabled*	f_{VCO1_0}	off	*Enabled*	f_{VCO2_0}	off	*Enabled*	f_{VCO1_0}	off	*Enabled*

(1) In default mode or when programmed respectively, S1 and S2 act as serial programming interface, SDA and SCL. They do not have any control-pin function but they are internally interpreted as if S1 = 0 and S2 = 0. However, S0 is a control-pin which in the default mode switches all outputs ON or OFF (as previously predefined).

10.4 Device Functional Modes

10.4.1 SDA and SCL Serial Interface

The CDCEx937-Q1 operates as a slave device of the 2-wire serial SDA and SCL bus, compatible with the popular SMBus or I^2C specification. It operates in the standard-mode transfer (up to 100kbit/s) and fast-mode transfer (up to 400kbit/s) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDC9xx are dual function pins. In the default configuration they are used as SDA and SCL serial programming interface. They can be re-programmed as general purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, Byte 02, Bit [6].

10.5 Programming

10.5.1 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of Bytes read-out are defined by Byte Count in the Generic Configuration Register. At Block Read instruction all bytes defined in the Byte Count has to be readout to correctly finish the read cycle.

Once a byte has been sent, it is written into the internal register and is effective immediately. This applies to each transferred byte independent of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM Write Cycle is initiated, the internal SDA register contents are written into the EEPROM. During this write cycle, data is not accepted at the SDA and SCL bus until the write cycle is completed. However, data can be read during the programming sequence (Byte Read or Block Read). The programming status can be monitored by reading *EEPIP*, Byte 01–Bit [6].

The offset of the indexed byte is encoded in the command code, as described in Table 5.

Table 5. Slave Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1 (1)	A0 (1)	R/$\overline{W}$
CDCEx913	1	1	0	0	1	0	1	1/0
CDCEx925	1	1	0	0	1	0	0	1/0
CDCEx937	1	1	0	1	1	0	1	1/0
CDCEx949	1	1	0	1	1	0	0	1/0

(1) Address bits A0 and A1 are programmable through the SDA and SCL bus (Byte 01, Bit [1:0]). This allows addressing up to 4 devices connected to the same SDA and SCL bus. The least-significant bit of the address byte designates a write or read operation.

10.5.2 Command Code Definition

Table 6. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte Offset for *Byte Read*, *Block Read*, *Byte Write* and *Block Write* operation.

10.5.3 Generic Programming Sequence

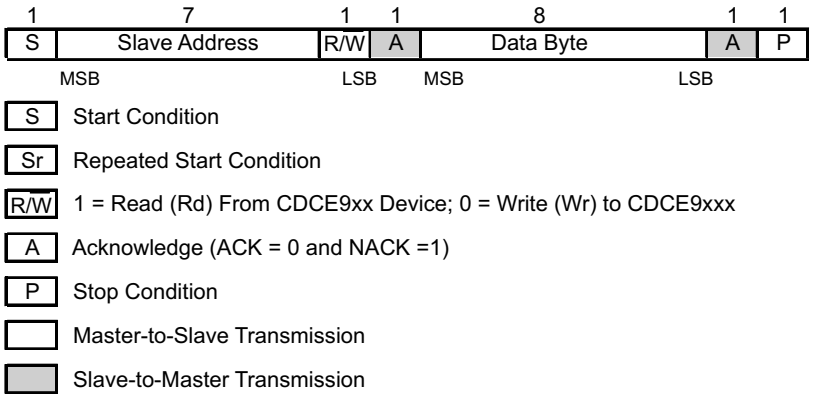


Figure 7. Generic Programming Sequence

10.5.4 Byte Write Programming Sequence

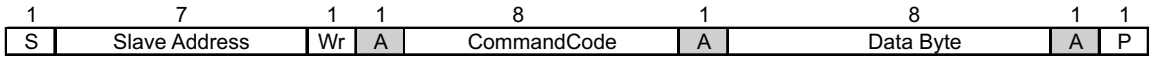


Figure 8. Byte Write Protocol

10.5.5 Byte Read Programming Sequence

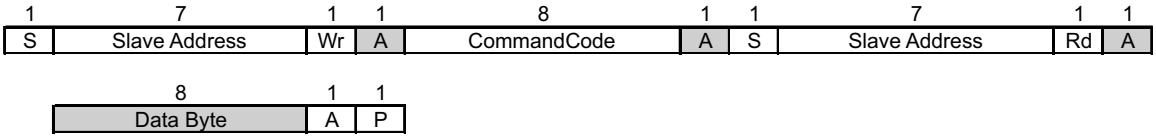
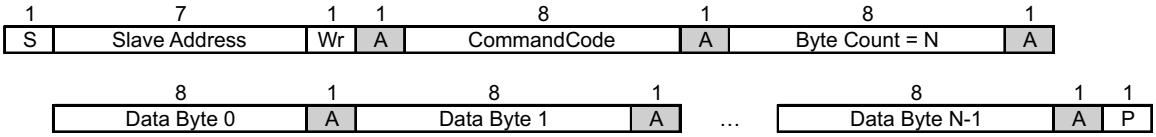


Figure 9. Byte Read Protocol

10.5.6 Block Write Programming Sequence



(1) Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, it is used for internal test purpose and must not be overwritten.

Figure 10. Block Write Protocol

10.5.7 Block Read Programming Sequence

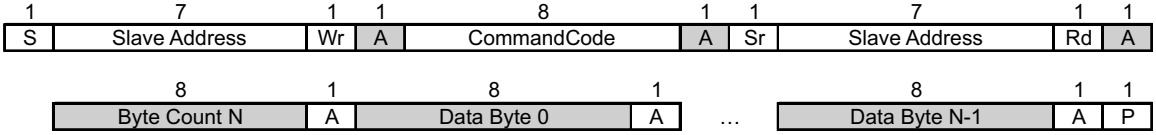


Figure 11. Block Read Protocol

10.5.8 Timing Diagram for the SDA and SCL Serial Control Interface

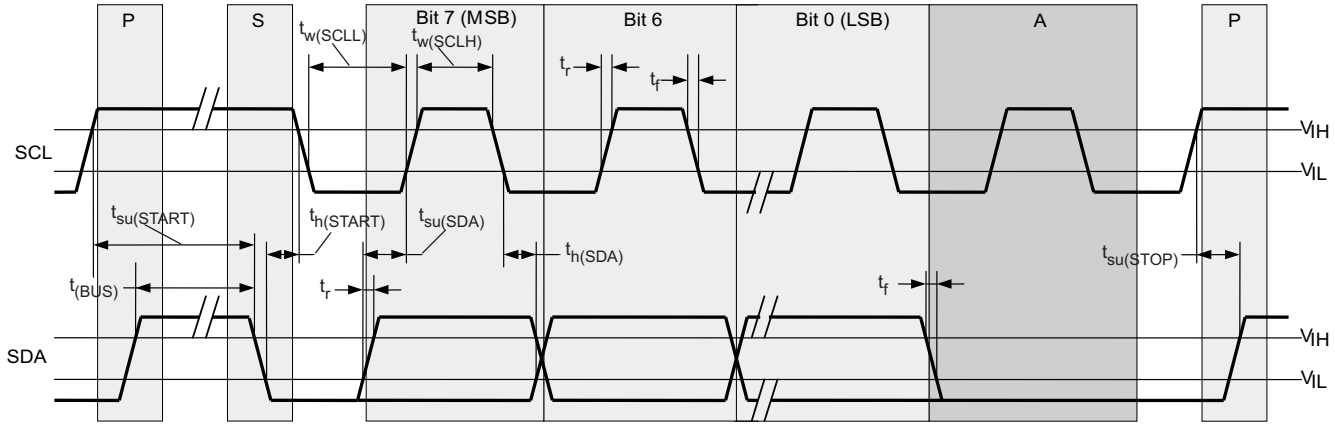


Figure 12. Timing Diagram for SDA and SCL Serial Control Interface

10.5.9 SDA and SCL Hardware Interface

Figure 13 shows how the CDCEx937-Q1 clock synthesizer is connected to the SDA and SCL serial interface bus. Multiple devices can be connected to the bus but the speed may require reduction if many devices are connected (400 kHz is the maximum).

Note that the pullup resistors (R_P) depends on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 kΩ. It must meet the minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages (for more details see SMBus or I^2C Bus specification).

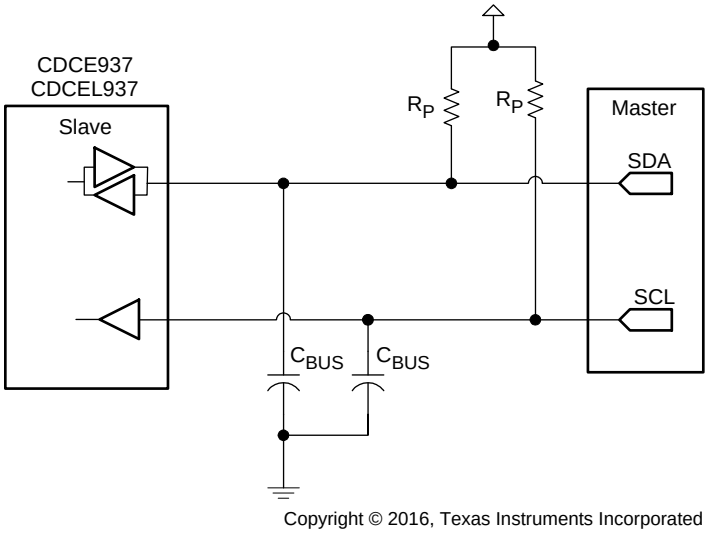


Figure 13. SDA and SCL Hardware Interface

10.6 Register Maps

10.6.1 SDA and SCL Configuration Registers

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCEx937-Q1. All settings can be manually written into the device through the SDA and SCL bus or easily programmed by using the TI Pro-Clock software. TI Pro-Clock software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 7. SDA and SCL Registers

ADDRESS OFFSET	REGISTER DESCRIPTION	TABLE
00h	Generic Configuration Register	Table 9
10h	PLL1 Configuration Register	Table 10
20h	PLL2 Configuration Register	Table 11
30h	PLL3 Configuration Register	Table 12

The grey-highlighted bits, described in the Configuration Registers tables in the following pages, belong to the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2 (see the *Control Terminal Configuration* section).

Table 8. Configuration Register, External Control Terminals

	EXTERNAL CONTROL PINS			Y1	PLL1 SETTINGS			PLL2 SETTINGS			PLL3 SETTINGS		
				OUTPUT SELECT	FREQ. SELECT	SSC SELECT	OUTPUT SELECT	FREQ. SELECT	SSC SELECT	OUTPUT SELECT	FREQ. SELECT	SSC SELECT	OUTPUT SELECT
	S2	S1	S0	Y1	FS1	SSC1	Y2Y3	FS2	SSC2	Y4Y5	FS3	SSC3	Y6Y7
0	0	0	0	Y1_0	FS1_0	SSC1_0	Y2Y3_0	FS2_0	SSC2_0	Y4Y5_0	FS3_0	SSC3_0	Y6Y7_0
1	0	0	1	Y1_1	FS1_1	SSC1_1	Y2Y3_1	FS2_1	SSC2_1	Y4Y5_1	FS3_1	SSC3_1	Y6Y7_1
2	0	1	0	Y1_2	FS1_2	SSC1_2	Y2Y3_2	FS2_2	SSC2_2	Y4Y5_2	FS3_2	SSC3_2	Y6Y7_2
3	0	1	1	Y1_3	FS1_3	SSC1_3	Y2Y3_3	FS2_3	SSC2_3	Y4Y5_3	FS3_3	SSC3_3	Y6Y7_3
4	1	0	0	Y1_4	FS1_4	SSC1_4	Y2Y3_4	FS2_4	SSC2_4	Y4Y5_4	FS3_4	SSC3_4	Y6Y7_4
5	1	0	1	Y1_5	FS1_5	SSC1_5	Y2Y3_5	FS2_5	SSC2_5	Y4Y5_5	FS3_5	SSC3_5	Y6Y7_5
6	1	1	0	Y1_6	FS1_6	SSC1_6	Y2Y3_6	FS2_6	SSC2_6	Y4Y5_6	FS3_6	SSC3_6	Y6Y7_6
7	1	1	1	Y1_7	FS1_7	SSC1_7	Y2Y3_7	FS2_7	SSC2_7	Y4Y5_7	FS3_7	SSC3_7	Y6Y7_7
	Address Offset(1)			04h	13h	10h to 12h	15h	23h	20h to 22h	25h	33h	30h to 32h	35h

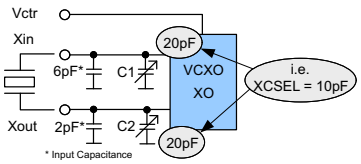
(1) Address Offset refers to the byte address in the Configuration Register in the following pages.

Table 9. Generic Configuration Register

OFFSET(1)	BIT(2)	ACRONYM	DEFAULT(3)	DESCRIPTION
00h	7	E_EL	Xb	Device identification (read-only): 1 is CDCE937-Q1 (3.3 V), 0 is CDCEL937-Q1 (1.8 V)
	6:4	RID	Xb	Revision Identification Number (read only)
	3:0	VID	1h	Vendor Identification Number (read only)
01h	7	–	0b	Reserved – always write 0
	6	EEPIP	0b	EEPROM Programming Status:(4) (read only) 0 – EEPROM programming is completed 1 – EEPROM is in programming mode
	5	EELOCK	0b	Permanently Lock EEPROM Data(5) 0 – EEPROM is not locked 1 – EEPROM is permanently locked
	4	PWDN	0b	Device Power Down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN cannot be set to 1 in the EEPROM. 0 – device active (PLL1 and all outputs are enabled) 1 – device power down (PLL1 in power down and all outputs in 3-state)
	3:2	INCLK	00b	Input clock selection: 00 – Xtal 01 – VCXO 10 – LVCMOS 11 – reserved
	1:0	SLAVE_ADR	01b	Programmable Address Bits A0 and A1 of the Slave Receiver Address
02h	7	M1	1b	Clock source selection for output Y1: 0 – input clock 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pin 18/19(6) 0 – serial programming interface SDA (pin 19) and SCL (pin 18) 1 – control pins S1 (pin 19) and S2 (pin 18)
	5:4	Y1_ST1	11b	Y1-State0/1 Definition 00 – device power down (all PLLs in power down and all outputs in 3-State) 01 – Y1 disabled to 3-state 10 – Y1 disabled to low 11 – Y1 enabled
	3:2	Y1_ST0	01b	
	1:0	Pdiv1 [9:8]	001h	10-Bit Y1-Output-Divider Pdiv1: 0 – divider reset and stand-by 1-to-1023 – divider value
03h	7:0	Pdiv1 [7:0]		

(1) Writing data beyond '40h' may affect device function.
(2) All data transferred with the MSB first.
(3) Unless customer-specific setting.
(4) During EEPROM programming, no data is allowed to be sent to the device through the SDA and SCL bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (Byte Read or Block Read).
(5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. There is no further programming possible. Data, however can still be written through SDA and SCL bus to the internal register to change device function on the fly. But new data can no longer be saved to the EEPROM. EELOCK is effective only, if written into the EEPROM!
(6) Selection of *control pins* is effective only if written into the EEPROM. Once written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA and SCL), and the two slave receiver address bits are reset to A0 = *0* and A1 = *0*.

Table 9. Generic Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
04h	7	Y1_7	0b	Y1_ST0/Y1_ST1 State Selection[7] 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1)
	6	Y1_6	0b	
	5	Y1_5	0b	
	4	Y1_4	0b	
	3	Y1_3	0b	
	2	Y1_2	0b	
	1	Y1_1	1b	
	0	Y1_0	0b	
05h	7:3	XCSEL	0Ah	Crystal Load Capacitor Selection[8] 00h → 0 pF 01h → 1 pF 02h → 2 pF : 14h-to-1Fh → 20 pF 
	2:0		0b	Reserved – do not write other than 0
06h	7:1	BCOUNT	40h	7-Bit Byte Count (defines the number of bytes which is sent from this device at the next Block Read transfer); *all* bytes have to be read out to correctly finish the read cycle.)
	0	EEWRITE	0b	Initiate EEPROM Write Cycle[4] [9] 0– no EEPROM write cycle 1 – start EEPROM write cycle (internal configuration register is saved to the EEPROM)
07h-0Fh		—	0h	Unused address range

(7) These are the bits of the Control Terminal Register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.
(8) The internal load capacitor (C1, C2) has to be used to achieve the best clock performance. External capacitors must be used only to finely adjust C_L by a few pF's. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For C_L > 20 pF, use additional external capacitors. Also, the value of the device input capacitance has to be considered which always adds 1.5 pF (6 pF//2 pF) to the selected C_L. For more information about VCXO configuration and crystal recommendation, see *VCXO Application Guideline for CDCE(L)9xx Family* (SCAA085).
(9) Note: The EEPROM WRITE bit must be sent last. This ensures that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level high does not trigger an EEPROM WRITE cycle. The EEWRITE bit has to be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

Table 10. PLL1 Configuration Register

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC Selection (Modulation Amount)[4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC1_6 [2:0]	000b	
	1:0	SSC1_5 [2:1]	000b	
11h	7	SSC1_5 [0]		
	6:4	SSC1_4 [2:0]	000b	
	3:1	SSC1_3 [2:0]	000b	
	0	SSC1_2 [2]	000b	
12h	7:6	SSC1_2 [1:0]		
	5:3	SSC1_1 [2:0]	000b	
	2:0	SSC1_0 [2:0]	000b	

(1) Writing data beyond 40h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 10. PLL1 Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
13h	7	FS1_7	0b	FS1_x: PLL1 Frequency Selection[4] 0 – f_{VCO1_0} (predefined by PLL1_0 – Multiplier/Divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – Multiplier/Divider value)
	6	FS1_6	0b	
	5	FS1_5	0b	
	4	FS1_4	0b	
	3	FS1_3	0b	
	2	FS1_2	0b	
	1	FS1_1	0b	
	0	FS1_0	0b	
14h	7	MUX1	1b	PLL1 Multiplexer: 0 – PLL1 1 – PLL1 Bypass (PLL1 is in power down)
	6	M2	1b	Output Y2 Multiplexer: 0 – Pdiv1 1 – Pdiv2
	5:4	M3	10b	Output Y3 Multiplexer: 00 – Pdiv1-Divider 01 – Pdiv2-Divider 10 – Pdiv3-Divider 11 – reserved
	3:2	Y2Y3_ST1	11b	Y2, Y3-State0/1definition: 00 – Y2/Y3 disabled to 3-State (PLL1 is in power down) 01 – Y2/Y3 disabled to 3-State 10–Y2/Y3 disabled to low 11 – Y2/Y3 enabled
	1:0	Y2Y3_ST0	01b	
15h	7	Y2Y3_7	0b	Y2Y3_x Output State Selection[4] 0 – state0 (predefined by Y2Y3_ST0) 1 – state1 (predefined by Y2Y3_ST1)
	6	Y2Y3_6	0b	
	5	Y2Y3_5	0b	
	4	Y2Y3_4	0b	
	3	Y2Y3_3	0b	
	2	Y2Y3_2	0b	
	1	Y2Y3_1	1b	
	0	Y2Y3_0	0b	
16h	7	SSC1DC	0b	PLL1 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv2	01h	7-Bit Y2-Output-Divider Pdiv2: 0 – reset and stand-by 1-to-127 is divider value
17h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv3	01h	7-Bit Y3-Output-Divider Pdiv3: 0 – reset and stand-by 1-to-127 is divider value
18h	7:0	PLL1_0N [11:4]	004h	PLL1_0: 30-Bit Multiplier/Divider value for frequency f_{VCO1_0} (for more information, see *PLL Multiplier or Divider Definition*).
19h	7:4	PLL1_0N [3:0]		
	3:0	PLL1_0R [8:5]	000h	
1Ah	7:3	PLL1_0R[4:0]		
	2:0	PLL1_0Q [5:3]	10h	
1Bh	7:5	PLL1_0Q [2:0]		
	4:2	PLL1_0P [2:0]	010b	
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection: 00 – f_{VCO1_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_0} < 175 MHz 11 – f_{VCO1_0} ≥ 175 MHz
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1: 30-Bit Multiplier/Divider value for frequency f_{VCO1_1} (for more information, see *PLL Multiplier or Divider Definition*).
1Dh	7:4	PLL1_1N [3:0]		
	3:0	PLL1_1R [8:5]	000h	
1Eh	7:3	PLL1_1R[4:0]		
	2:0	PLL1_1Q [5:3]	10h	
1Fh	7:5	PLL1_1Q [2:0]		
	4:2	PLL1_1P [2:0]	010b	
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection: 00 – f_{VCO1_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_1} < 175 MHz 11 – f_{VCO1_1} ≥ 175 MHz

Table 11. PLL2 Configuration Register

OFFSET(1)	BIT(2)	ACRONYM	DEFAULT(3)	DESCRIPTION
20h	7:5	SSC2_7 [2:0]	000b	SSC2: PLL2 SSC Selection (Modulation Amount)(4) **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC2_6 [2:0]	000b	
	1:0	SSC2_5 [2:1]	000b	
21h	7	SSC2_5 [0]		
	6:4	SSC2_4 [2:0]	000b	
	3:1	SSC2_3 [2:0]	000b	
	0	SSC2_2 [2]	000b	
22h	7:6	SSC2_2 [1:0]		
	5:3	SSC2_1 [2:0]	000b	
	2:0	SSC2_0 [2:0]	000b	
23h	7	FS2_7	0b	FS2_x: PLL2 Frequency Selection(4) 0 – f_{VCO2_0} (predefined by PLL2_0 – Multiplier/Divider value) 1 – f_{VCO2_1} (predefined by PLL2_1 – Multiplier/Divider value)
	6	FS2_6	0b	
	5	FS2_5	0b	
	4	FS2_4	0b	
	3	FS2_3	0b	
	2	FS2_2	0b	
	1	FS2_1	0b	
	0	FS2_0	0b	
24h	7	MUX2	1b	PLL2 Multiplexer: 0 – PLL2 1 – PLL2 Bypass (PLL2 is in power down)
	6	M4	1b	Output Y4 Multiplexer: 0 – Pdiv2 1 – Pdiv4
	5:4	M5	10b	Output Y5 Multiplexer: 00 – Pdiv2-Divider 01 – Pdiv4-Divider 10 – Pdiv5-Divider 11 – reserved
	3:2	Y4Y5_ST1	11b	Y4, Y5-State0/1definition: 00 – Y4/Y5 disabled to 3-State (PLL2 is in power down) 01 – Y4/Y5 disabled to 3-State 10–Y4/Y5 disabled to low 11 – Y4/Y5 enabled
	1:0	Y4Y5_ST0	01b	
25h	7	Y4Y5_7	0b	Y4Y5_x Output State Selection(4) 0 – state0 (predefined by Y4Y5_ST0) 1 – state1 (predefined by Y4Y5_ST1)
	6	Y4Y5_6	0b	
	5	Y4Y5_5	0b	
	4	Y4Y5_4	0b	
	3	Y4Y5_3	0b	
	2	Y4Y5_2	0b	
	1	Y4Y5_1	1b	
	0	Y4Y5_0	0b	
26h	7	SSC2DC	0b	PLL2 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv4	01h	7-Bit Y4-Output-Divider Pdiv4: 0 – reset and stand-by 1-to-127 – divider value
27h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv5	01h	7-Bit Y5-Output-Divider Pdiv5: 0 – reset and stand-by 1-to-127 – divider value

(1) Writing data beyond 40h may adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.

Table 11. PLL2 Configuration Register (continued)

OFFSET(1)	BIT(2)	ACRONYM	DEFAULT(3)	DESCRIPTION
28h	7:0	PLL2_0N [11:4	004h	PLL2_0: 30-Bit Multiplier/Divider value for frequency f_{VCO2_0} (for more information, see *PLL Multiplier or Divider Definition*).
29h	7:4	PLL2_0N [3:0]		
	3:0	PLL2_0R [8:5]	000h	
2Ah	7:3	PLL2_0R[4:0]		
	2:0	PLL2_0Q [5:3]	10h	
2Bh	7:5	PLL2_0Q [2:0]		
	4:2	PLL2_0P [2:0]	010b	
	1:0	VCO2_0_RANGE	00b	f_{VCO2_0} range selection: 00 – f_{VCO2_0} < 125 MHz; 01 – 125 MHz ≤ f_{VCO2_0} < 150 MHz; 10 – 150 MHz ≤ f_{VCO2_0} < 175 MHz; 11 – f_{VCO2_0} ≥ 175 MHz
2Ch	7:0	PLL2_1N [11:4]	004h	PLL2_1: 30-Bit Multiplier/Divider value for frequency f_{VCO2_1} (for more information, see *PLL Multiplier or Divider Definition*).
2Dh	7:4	PLL2_1N [3:0]		
	3:0	PLL2_1R [8:5]	000h	
2Eh	7:3	PLL2_1R[4:0]		
	2:0	PLL2_1Q [5:3]	10h	
2Fh	7:5	PLL2_1Q [2:0]		
	4:2	PLL2_1P [2:0]	010b	
	1:0	VCO2_1_RANGE	00b	f_{VCO2_1} range selection: 00 – f_{VCO2_1} < 125 MHz; 01 – 125 MHz ≤ f_{VCO2_1} < 150 MHz; 10 – 150 MHz ≤ f_{VCO2_1} < 175 MHz; 11 – f_{VCO2_1} ≥ 175 MHz

Table 12. PLL3 Configuration Register

OFFSET(1)	BIT(2)	ACRONYM	DEFAULT(3)	DESCRIPTION
30h	7:5	SSC3_7 [2:0]	000b	SSC3: PLL3 SSC Selection (Modulation Amount)(4) **Down**: 000 (off); 001 – 0.25%; 010 – 0.5%; 011 – 0.75%; 100 – 1.0%; 101 – 1.25%; 110 – 1.5%; 111 – 2.0% **Center**: 000 (off); 001 ± 0.25%; 010 ± 0.5%; 011 ± 0.75%; 100 ± 1.0%; 101 ± 1.25%; 110 ± 1.5%; 111 ± 2.0%
	4:2	SSC3_6 [2:0]	000b	
	1:0	SSC3_5 [2:1]	000b	
31h	7	SSC3_5 [0]		
	6:4	SSC3_4 [2:0]	000b	
	3:1	SSC3_3 [2:0]	000b	
	0	SSC3_2 [2]	000b	
32h	7:6	SSC3_2 [1:0]		
	5:3	SSC3_1 [2:0]	000b	
	2:0	SSC3_0 [2:0]	000b	
33h	7	FS3_7	0b	FS3_x: PLL3 Frequency Selection(4) 0 – f_{VCO3_0} (predefined by PLL3_0 – Multiplier/Divider value) 1 – f_{VCO3_1} (predefined by PLL3_1 – Multiplier/Divider value)
	6	FS3_6	0b	
	5	FS3_5	0b	
	4	FS3_4	0b	
	3	FS3_3	0b	
	2	FS3_2	0b	
	1	FS3_1	0b	
	0	FS3_0	0b	

(1) Writing data beyond 40h may affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used
(4) These are the bits of the *Control Terminal Register*. The user can pre-define up to eight different control settings. At normal device operation, these setting can be selected by the external control pins, S0, S1, and S2.

Table 12. PLL3 Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
34h	7	MUX3	1b	PLL3 Multiplexer: 0 – PLL3 1 – PLL3 Bypass (PLL3 is in power down)
	6	M6	1b	Output Y6 Multiplexer: 0 – Pdiv4 1 – Pdiv6
	5:4	M7	10b	Output Y7 Multiplexer: 00 – Pdiv4-Divider 01 – Pdiv6-Divider 10 – Pdiv7-Divider 11 – reserved
	3:2	Y6Y7_ST1	11b	Y6, Y7-State0/1definition: 00 – Y6/Y7 disabled to 3-State and PLL3 power down 01 – Y6/Y7 disabled to 3-State 10 –Y6/Y7 disabled to low 11 – Y6/Y7 enabled
	1:0	Y6Y7_ST0	01b	
35h	7	Y6Y7_7	0b	Y6Y7_x Output State Selection[4] 0 – state0 (predefined by Y6Y7_ST0) 1 – state1 (predefined by Y6Y7_ST1)
	6	Y6Y7_6	0b	
	5	Y6Y7_5	0b	
	4	Y6Y7_4	0b	
	3	Y6Y7_3	0b	
	2	Y6Y7_2	0b	
	1	Y6Y7_1	1b	
	0	Y6Y7_0	0b	
36h	7	SSC3DC	0b	PLL3 SSC down/center selection: 0 – down 1 – center
	6:0	Pdiv6	01h	7-Bit Y6-Output-Divider Pdiv6: 0 – reset and stand-by 1-to-127 – divider value
37h	7	—	0b	Reserved – do not write others than 0
	6:0	Pdiv7	01h	7-Bit Y7-Output-Divider Pdiv7: 0 – reset and stand-by 1-to-127 – divider value
38h	7:0	PLL3_0N [11:4]	004h	PLL3_0: 30-Bit Multiplier/Divider value for frequency f_{VCO3_0} (for more information, see *PLL Multiplier or Divider Definition*).
39h	7:4	PLL3_0N [3:0]		
	3:0	PLL3_0R [8:5]	000h	
3Ah	7:3	PLL3_0R[4:0]		
	2:0	PLL3_0Q [5:3]	10h	
3Bh	7:5	PLL3_0Q [2:0]		
	4:2	PLL3_0P [2:0]	010b	
	1:0	VCO3_0_RANGE	00b	f_{VCO3_0} range selection: 00 – f_{VCO3_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO3_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO3_0} < 175 MHz 11 – f_{VCO3_0} ≥ 175 MHz
3Ch	7:0	PLL3_1N [11:4]	004h	PLL3_1: 30-Bit Multiplier/Divider value for frequency f_{VCO3_1} (for more information, see *PLL Multiplier or Divider Definition*).
3Dh	7:4	PLL3_1N [3:0]		
	3:0	PLL3_1R [8:5]	000h	
3Eh	7:3	PLL3_1R[4:0]		
	2:0	PLL3_1Q [5:3]	10h	
3Fh	7:5	PLL3_1Q [2:0]		
	4:2	PLL3_1P [2:0]	010b	
	1:0	VCO3_1_RANGE	00b	f_{VCO3_1} range selection: 00 – f_{VCO3_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO3_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO3_1} < 175 MHz 11 – f_{VCO3_1} ≥ 175 MHz

11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The CDCE937-Q1 device is an easy-to-use, high-performance, programmable CMOS clock synthesizer which can be used as a crystal buffer, clock synthesizer with separate output supply pin. The CDCE937-Q1 device features an on-chip loop filter and spread-spectrum modulation. Programming can be done through the I^2C interface, or previously saved settings can be loaded from on-chip EEPROM. The pins S0, S1, and S2 can be programmed as control pins to select various output settings. This section shows some examples of using the CDCE937-Q1 device in various applications.

11.2 Typical Application

Figure 14 shows the use of the CDCE937-Q1 device in an infotainment system, such as in head unit or telematics applications, using a 1.8-V single supply. Note that bypass capacitors are not shown in this schematic.

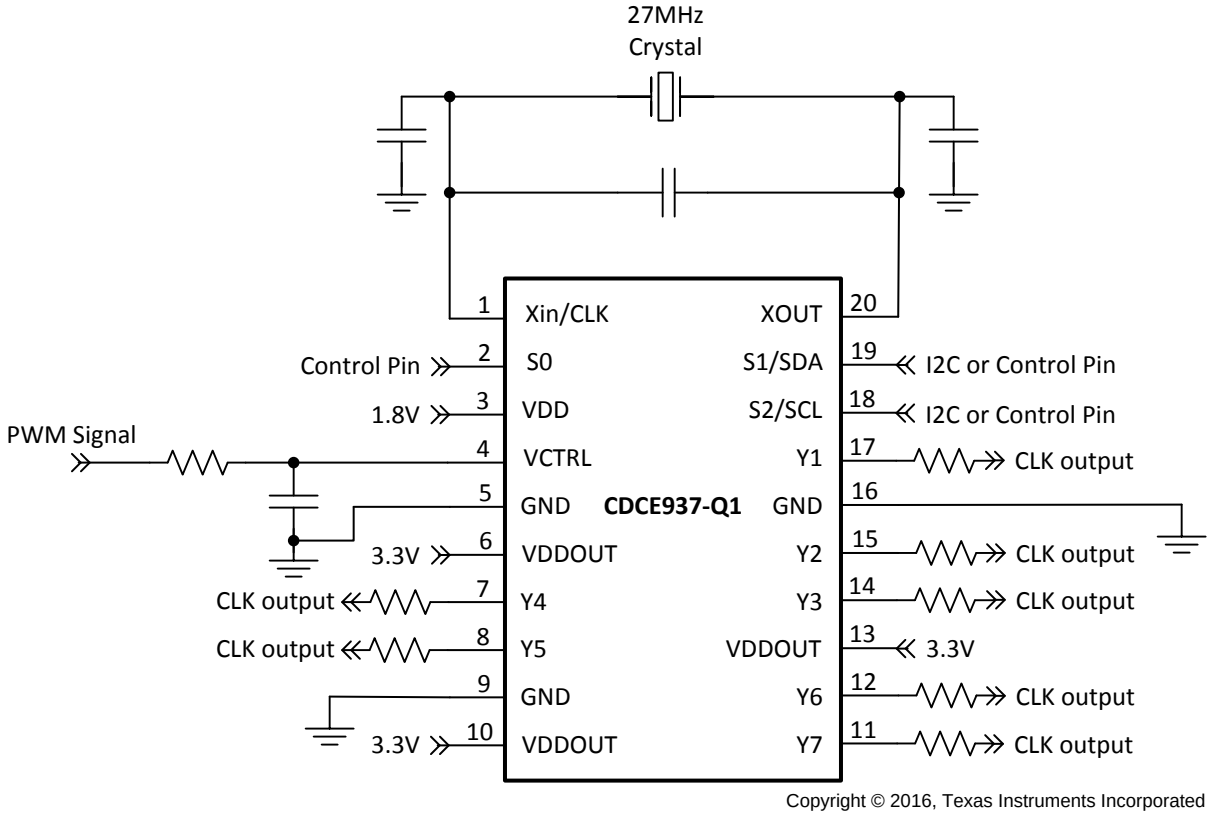


Figure 14. Single-Chip Solution Using a CDCE937-Q1 Device for Generating Clocking Frequencies

Typical Application (continued)

11.2.1 Design Requirements

The CDCE937-Q1 device supports spread-spectrum clocking (SSC) with multiple control parameters:

- Modulation amount (%)
- Modulation frequency (>20 kHz)
- Modulation shape (triangular, hershey, and others)
- Center spread or down spread (± or –)

For sample calculations of PLL constants, see *PLL Multiplier or Divider Definition*.

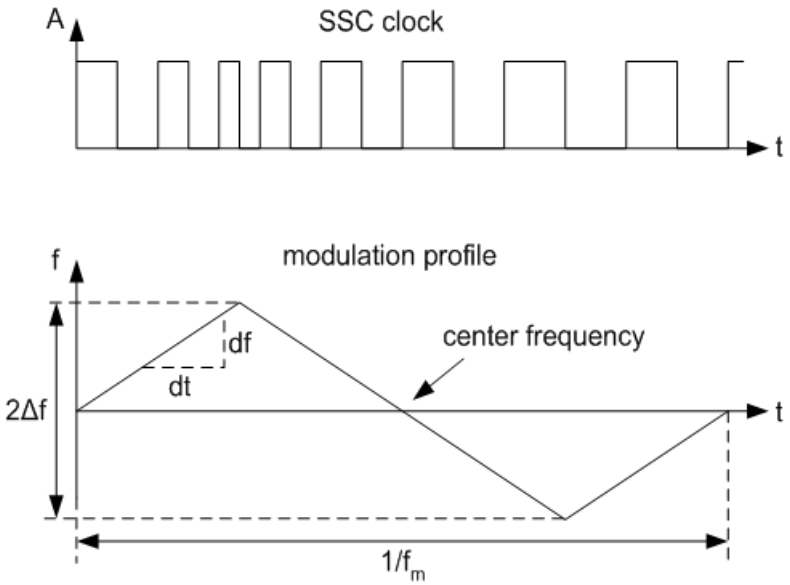
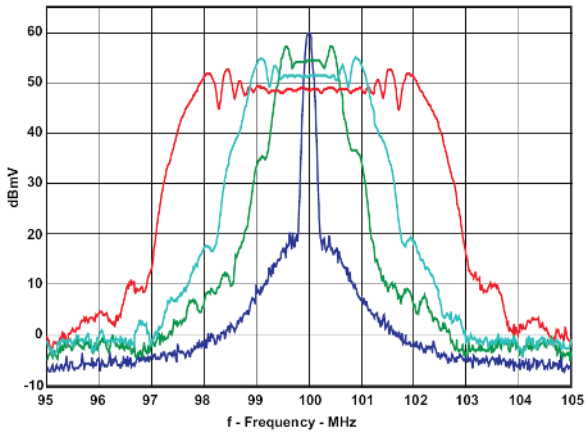


Figure 15. Modulation Frequency (fm) and Modulation Amount

11.2.2 Detailed Design Procedure

11.2.2.1 Spread-Spectrum Clock (SSC)

Spread-spectrum modulation is a method to spread emitted energy over a larger bandwidth. In clocking, spread spectrum can reduce electromagnetic interference (EMI) by reducing the level of emission from clock distribution network.



CDCS502 with a 25-MHz Crystal, FS = 1, f_{OUT} = 100 MHz, and 0%, ±0.5, ±1%, and ±2% SSC

Figure 16. Comparison Between Typical Clock Power Spectrum and Spread-Spectrum Clock

Typical Application (continued)

Spread spectrum clocking can be used to help reduce EMI to meet design specifications. For example, a specified EMI threshold of 55 dB/mV would require ±1% spread spectrum clocking to meet this requirement.

11.2.2.2 PLL Multiplier or Divider Definition

At a given input frequency (f_{IN}), the output frequency (f_{OUT}) of the CDCEx937-Q1 can be calculated with Equation 1.

$$f_{OUT} = \frac{f_{IN}}{Pdiv} x \frac{N}{M}$$

where

- M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL
- Pdiv (1 to 127) is the output divider (1)

The target VCO frequency (f_{VCO}) of each PLL can be calculated with Equation 2.

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and requires the following multiplier and divider settings:

$$P = 4 - int\left(\log_2 \frac{N}{M}\right) \left[\text{if } P < 0 \text{ then } P = 0\right]$$

$$Q = int\left(\frac{N'}{M}\right)$$

$$R = N' - M \times Q$$

where

$N' = N \times 2^P$

$N \geq M$

100 MHz < f_{VCO} > 200 MHz

Example:

for f_{IN} = 27 MHz; M = 1; N = 4; Pdiv = 2;

→ f_{OUT} = 54 MHz

→ f_{VCO} = 108 MHz

→ P = 4 – int($\log_2$4) = 4 – 2 = 2

→ N′ = 4 × 2^2 = 16

→ Q = int(16) = 16

→ R = 16 – 16 = 0

for f_{IN} = 27 MHz; M = 2; N = 11; Pdiv = 2;

→ f_{OUT} = 74.25 MHz

→ f_{VCO} = 148.50 MHz

→ P = 4 – int($\log_2$5.5) = 4 – 2 = 2

→ N′ = 11 × 2^2 = 44

→ Q = int(22) = 22

→ R = 44 – 44 = 0

The values for P, Q, R, and N' is automatically calculated when using TI Pro-Clock™ software.

11.2.2.3 Crystal Oscillator Start-Up

When the CDCE937-Q1 or CDCEL937-Q1 device is used as a crystal buffer, crystal oscillator start-up dominates the start-up time compared to the internal PLL lock time. The following diagram shows the oscillator start-up sequence for a 27-MHz crystal input with an 8-pF load. The start-up time for the crystal is on the order of approximately 250 µs compared to approximately 10 µs of lock time. In general, lock time is an order of magnitude less compared to the crystal start-up time.

Typical Application (continued)

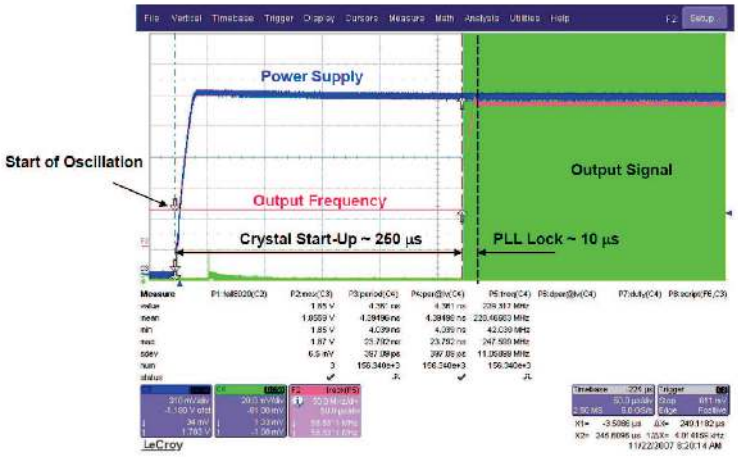


Figure 17. Crystal Oscillator Start-Up vs PLL Lock Time

11.2.2.4 Frequency Adjustment With Crystal Oscillator Pulling

The frequency for the CDCE937-Q1 or CDCEL937-Q1 device is adjusted for media and other applications with the VCXO control input V_{ctr}. If a PWM-modulated signal is used as a control signal for the VCXO, an external filter is required.

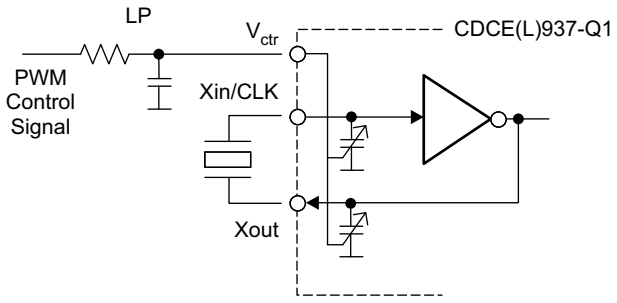


Figure 18. Frequency Adjustment Using PWM Input to the VCXO Control

11.2.2.5 Unused Inputs and Outputs

If VCXO-pulling functionality is not required, V_{ctr} must be left floating. All other unused inputs must be set to GND. Unused outputs must be left floating.

If one output block is not used, TI recommends disabling it. However, TI recommends providing a supply for all output blocks, even if they are disabled.

11.2.2.6 Switching Between XO and VCXO Mode

When the CDCEx937-Q1 device is in the crystal-oscillator or VCXO configuration, the internal capacitors require different internal capacitance. The following steps are recommended to switch to VCXO mode when the configuration for the on-chip capacitor is still set for XO mode. To center the output frequency to 0 ppm:

1. While in XO mode, put $V_{ctr} = V_{DD} / 2$
2. Switch from XO mode to VCXO mode
3. Program the internal capacitors to obtain 0 ppm at the output.

Typical Application (continued)

11.2.3 Application Curves

Figure 19, Figure 20, Figure 21, and Figure 22 show CDCE937-Q1 measurements with the SSC feature enabled. Device configuration: 27-MHz input, 27-MHz output.

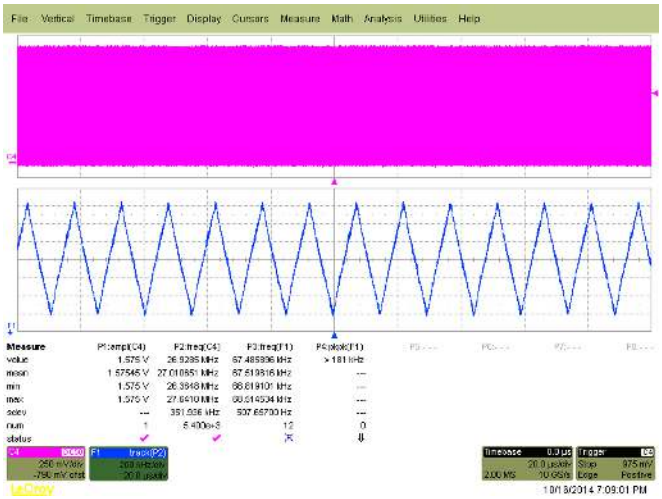


Figure 19. f_{OUT} = 27 MHz, VCO frequency < 125 MHz, SSC (2% Center)

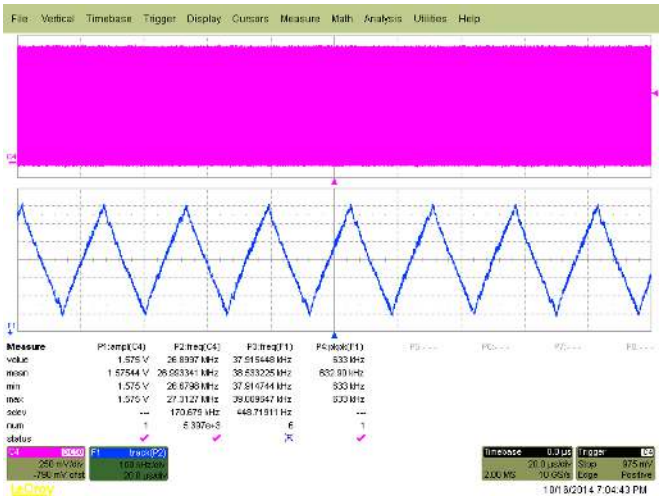


Figure 20. f_{OUT} = 27 MHz, VCO frequency > 175 MHz, SSC (1%, Center)

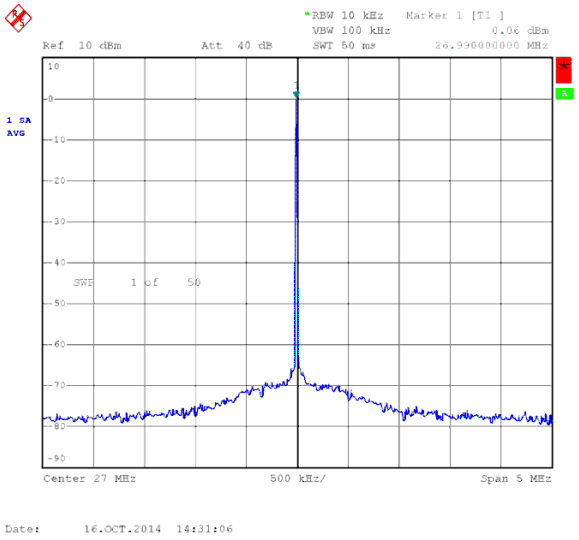


Figure 21. Output Spectrum With SSC Off

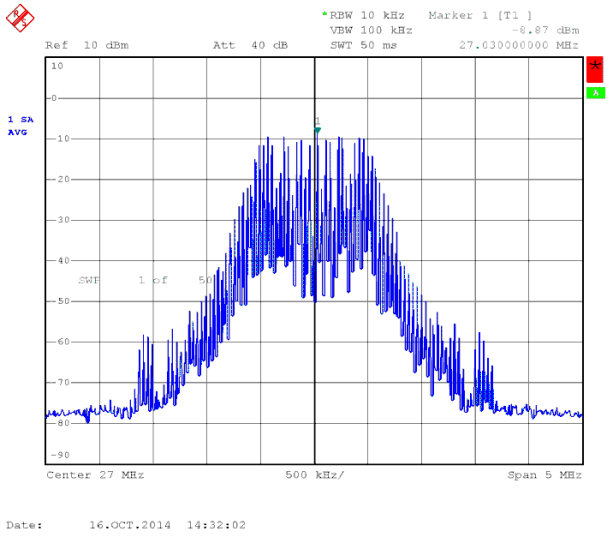


Figure 22. Output Spectrum With SSC On, 2% Center

12 Power Supply Recommendations

There is no restriction on the power-up sequence. In case V_{DDOUT} is applied first, TI recommends grounding V_{DD}. In case V_{DDOUT} is powered while V_{DD} is floating, there is a risk of high current flowing on the V_{DDOUT} pins.

The device has a power-up control that is connected to the 1.8-V supply. This keeps the whole device disabled until the 1.8-V supply reaches a sufficient voltage level. Then the device switches on all internal components, including the outputs. If a 3.3-V V_{DDOUT} is available before the 1.8-V, the outputs stay disabled until the 1.8-V supply has reached a certain level.

13 Layout

13.1 Layout Guidelines

When the CDCEx937-Q1 device is used as a crystal buffer, any parasitics across the crystal affect the pulling range of the VCXO. Therefore, take care in placing the crystal units on the board. Crystals must be placed as close to the device as possible, ensuring that the routing lines from the crystal terminals to Xin and Xout have the same length.

If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line, as it could be a source of noise coupling.

Additional discrete capacitors can be required to meet the load capacitance specification of certain crystals. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0 pF to 20 pF with steps of 1 pF. Therefore, the 0.7-pF capacitor can be discretely added on top of an internal 10 pF.

To minimize the inductive influence of the trace, TI recommends placing this small capacitor as close to the device as possible and symmetrically with respect to Xin and Xout.

Figure 23 shows a conceptual layout detailing recommended placement of power-supply bypass capacitors. For component-side mounting, use 0402 body-size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

13.2 Layout Example

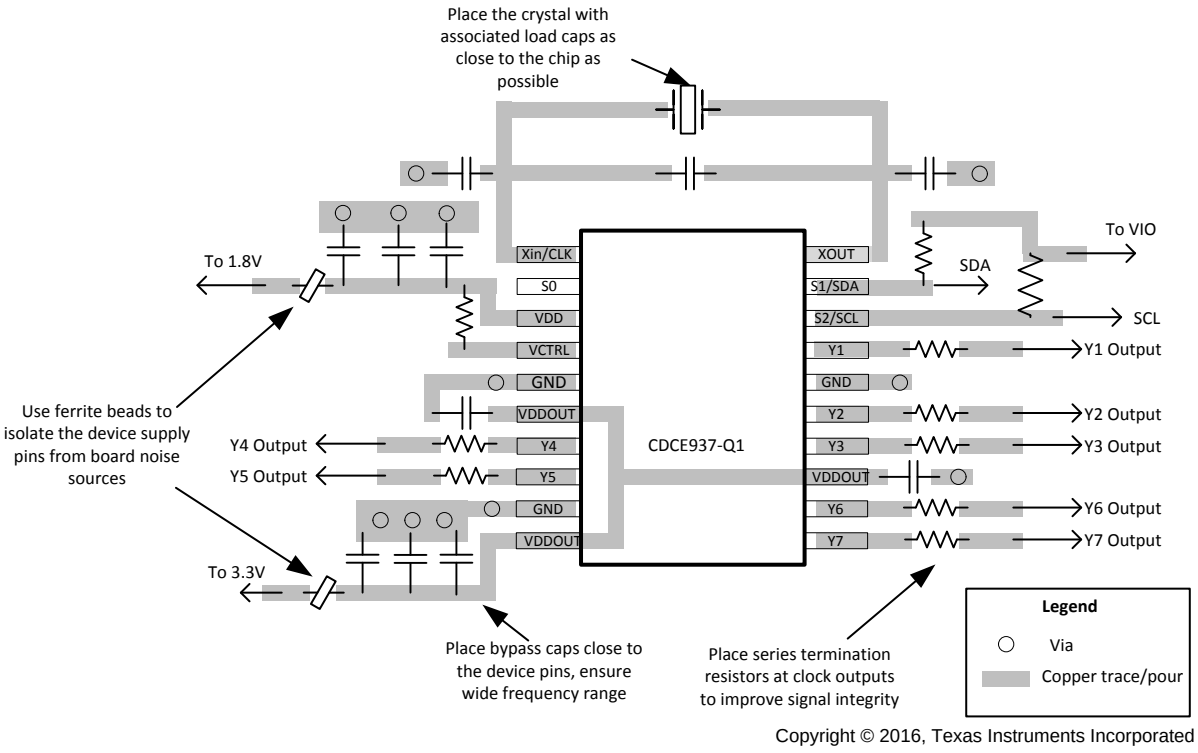


Figure 23. CDCE937-Q1 Layout Example

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

For related documentation see the following:

- *CDCE(L)9xx and CDCEx06 Programming Evaluation Module* (SCAU026)
- *VCXO Application Guideline for CDCE(L)9xx Family* (SCAA085)
- *General I2C/EEPROM Usage for the CDCE(L)9xx Family* (SCAA104)
- *Crystal Or Crystal Oscillator Replacement with Silicon Devices* (SNAA217)
- *Troubleshooting I^2C Bus Protocol* (SCAA106)
- *Usage of I^2C™ for CDCE(L)949, CDCE(L)937, CDCE(L)925, CDCE(L)913* (SCAA105)
- *Generating Low Phase-Noise Clocks for Audio Data Converters from Low Frequency Word Clock* (SCAA088)

14.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 13. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CDCE937-Q1	Click here	Click here	Click here	Click here	Click here
CDCEL937-Q1	Click here	Click here	Click here	Click here	Click here

14.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

14.5 Trademarks

DaVinci, OMAP, Pro-Clock, E2E are trademarks of Texas Instruments.
Bluetooth is a trademark of Bluetooth SIG.
Ethernet is a trademark of Xerox Corporattion.
All other trademarks are the property of their respective owners.

14.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCE937QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CDCE937Q	Samples
CDCEL937QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEL937Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CDCE937-Q1, CDCEL937-Q1 :

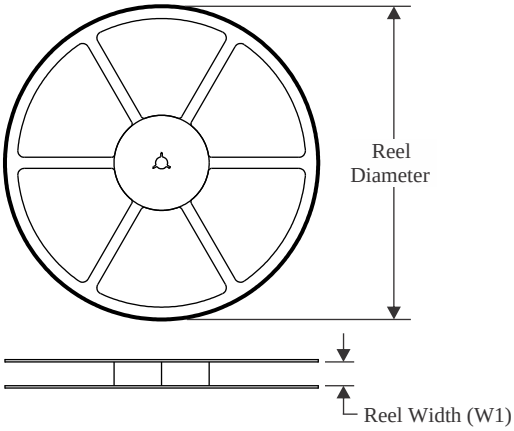
- Catalog: CDCE937, CDCEL937

NOTE: Qualified Version Definitions:

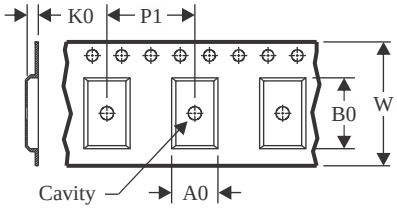
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

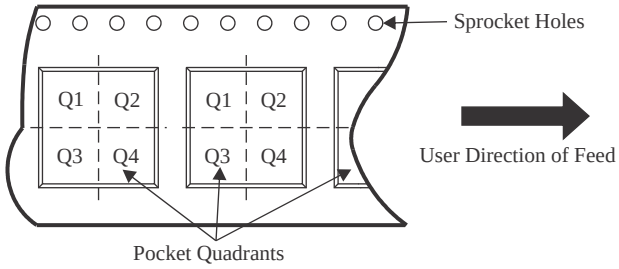


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

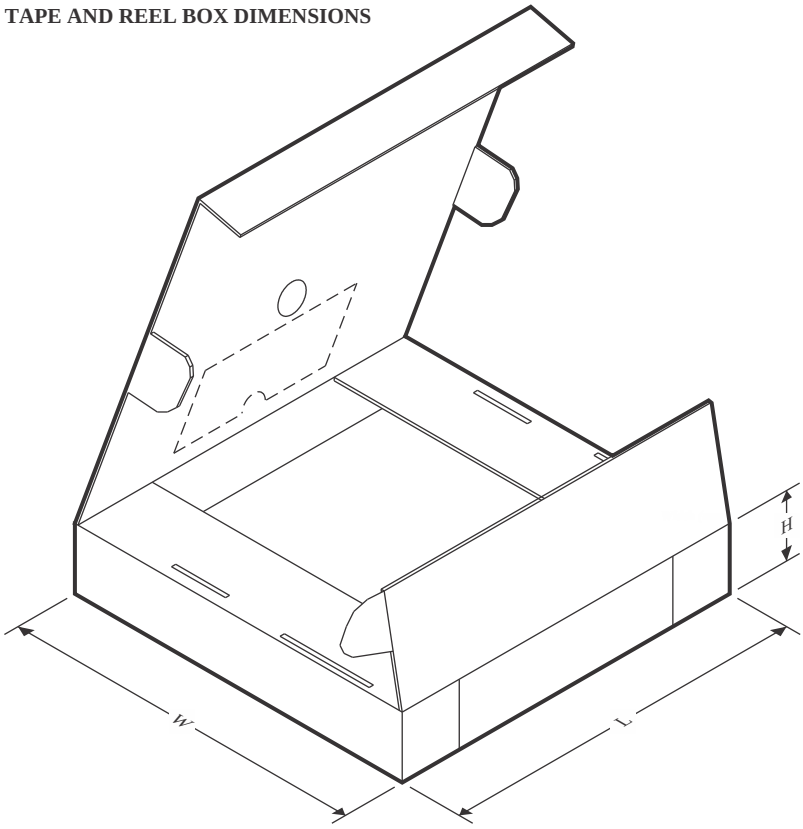
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE937QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
CDCEL937QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

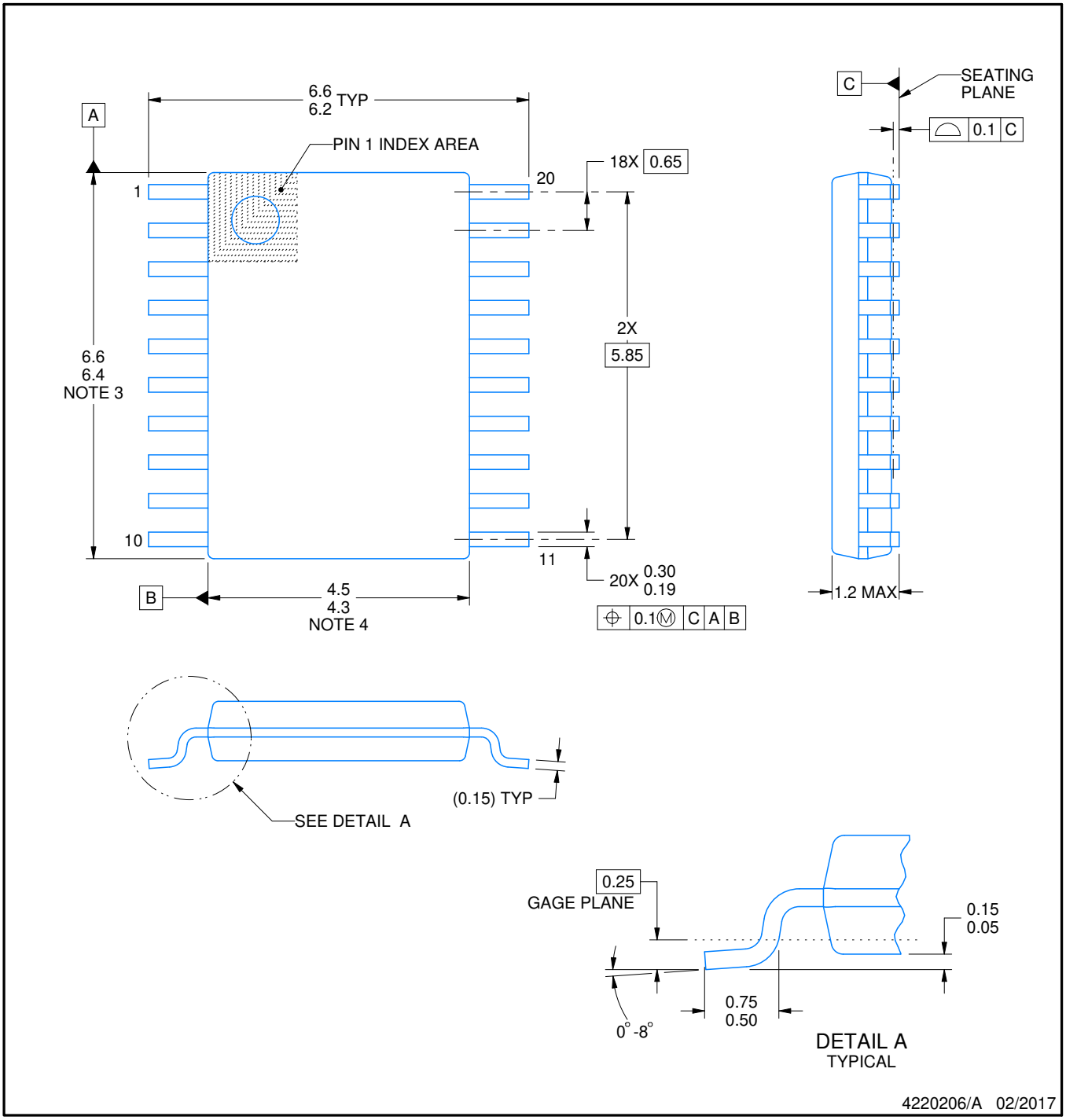
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE937QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0
CDCEL937QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0020A

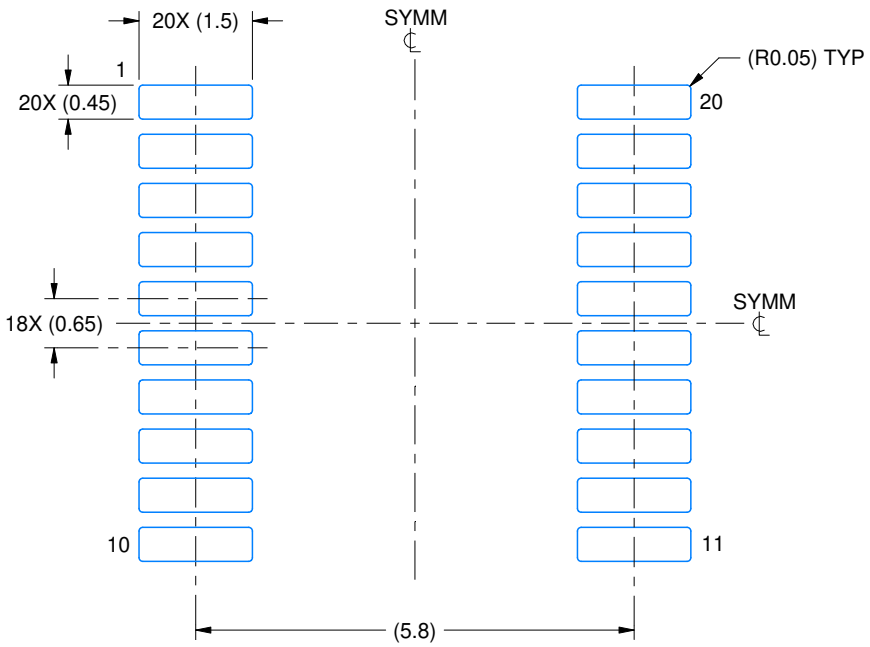
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



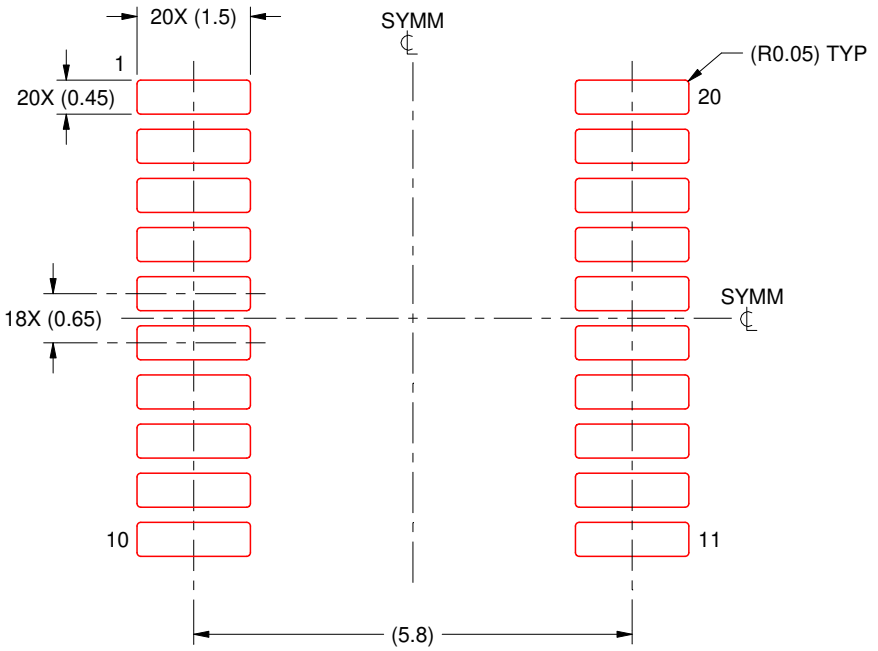
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



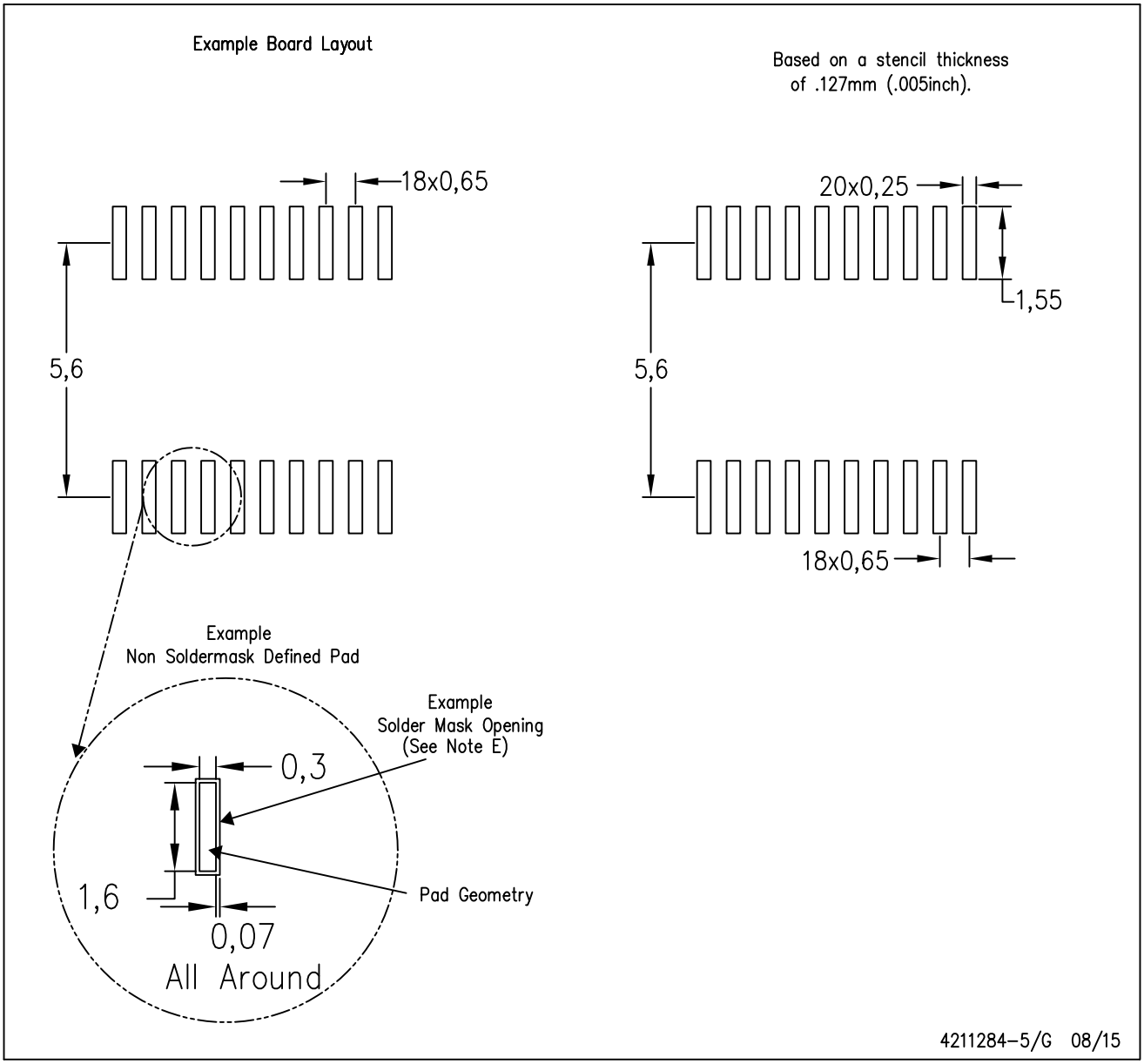
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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