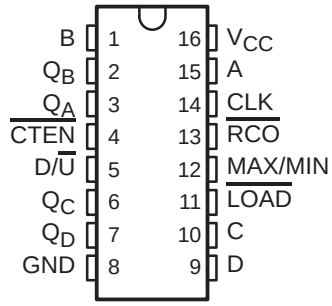
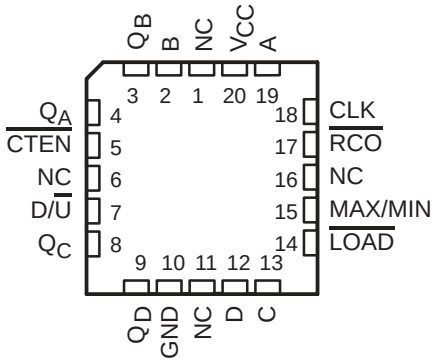
SDAS210 – D2661, DECEMBER 1982 – REVISED MAY 1986

- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**
- **Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS190, SN54ALS191 . . . J PACKAGE
SN74ALS190, SN74ALS191 . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS190, SN54ALS191 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

The ’ALS190 and ’ALS191 are synchronous, reversible up/down counters. The ’ALSL90 is a 4-bit decade counter and the ’ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input $\overline{\text{CTEN}}$ is low. A high at $\overline{\text{CTEN}}$ inhibits counting. The direction of the count is determined by the level of the down/up D/$\overline{\text{U}}$ input. When D/$\overline{\text{U}}$ is low, the counter counts up and when D/$\overline{\text{U}}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{\text{CTEN}}$ and D/$\overline{\text{U}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

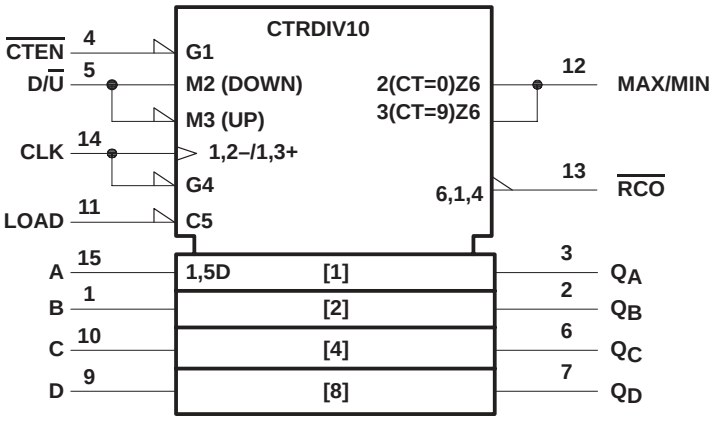
These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/$\overline{\text{U}}$, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

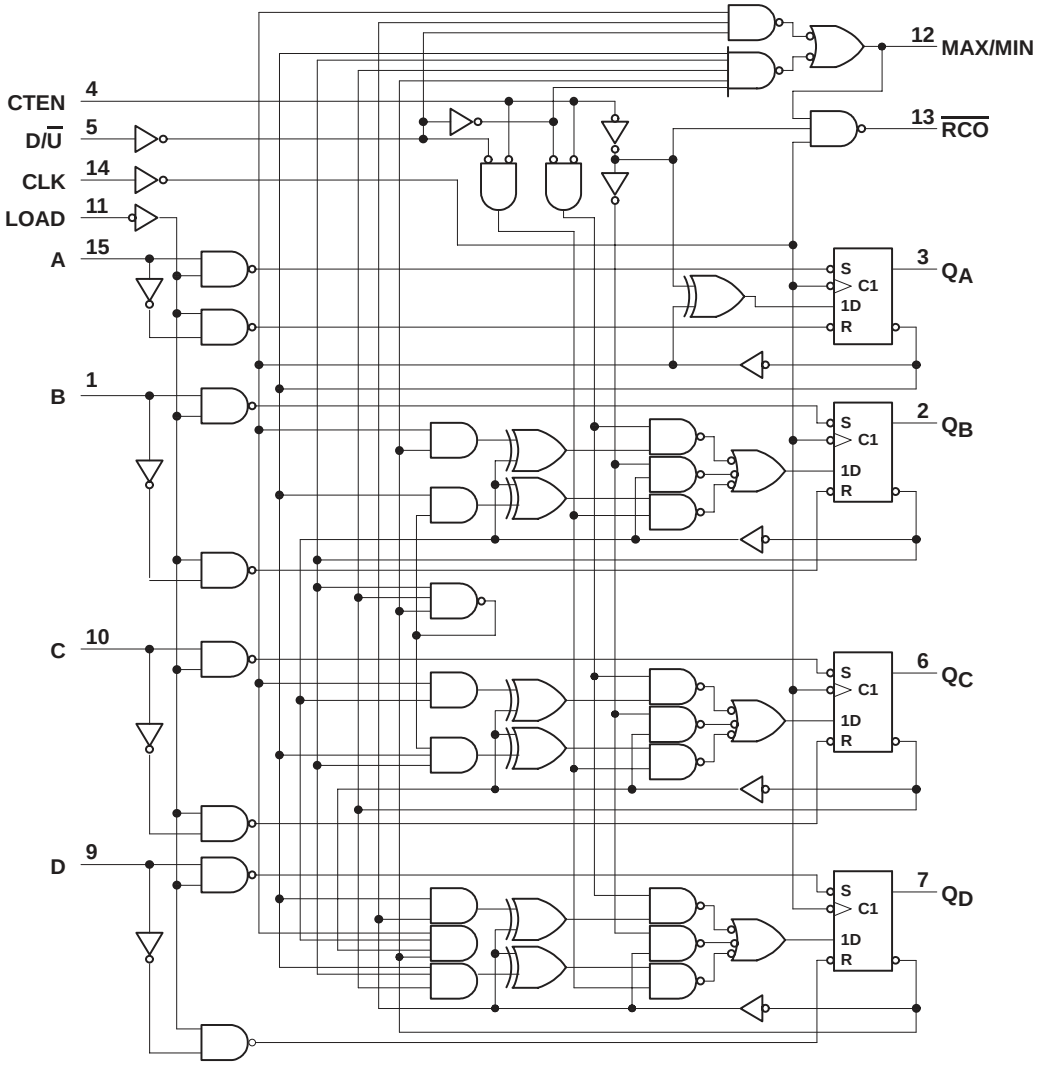
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

The SN54ALS190 and SN54ALS191 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS190 and SN74ALS191 are characterized for operation from 0°C to 70°C.

'ALS190 logic symbol†

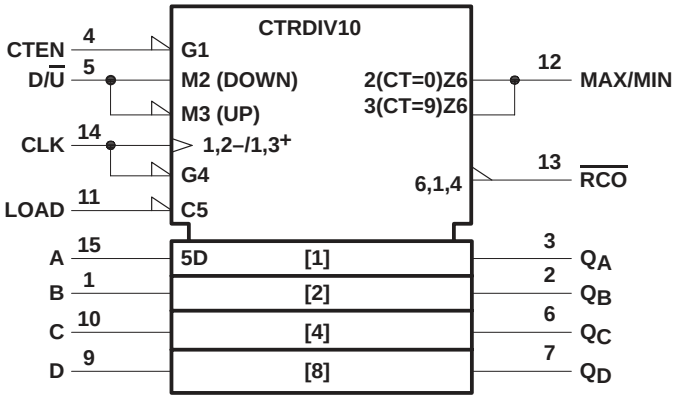


'ALS190 logic diagram (positive logic)

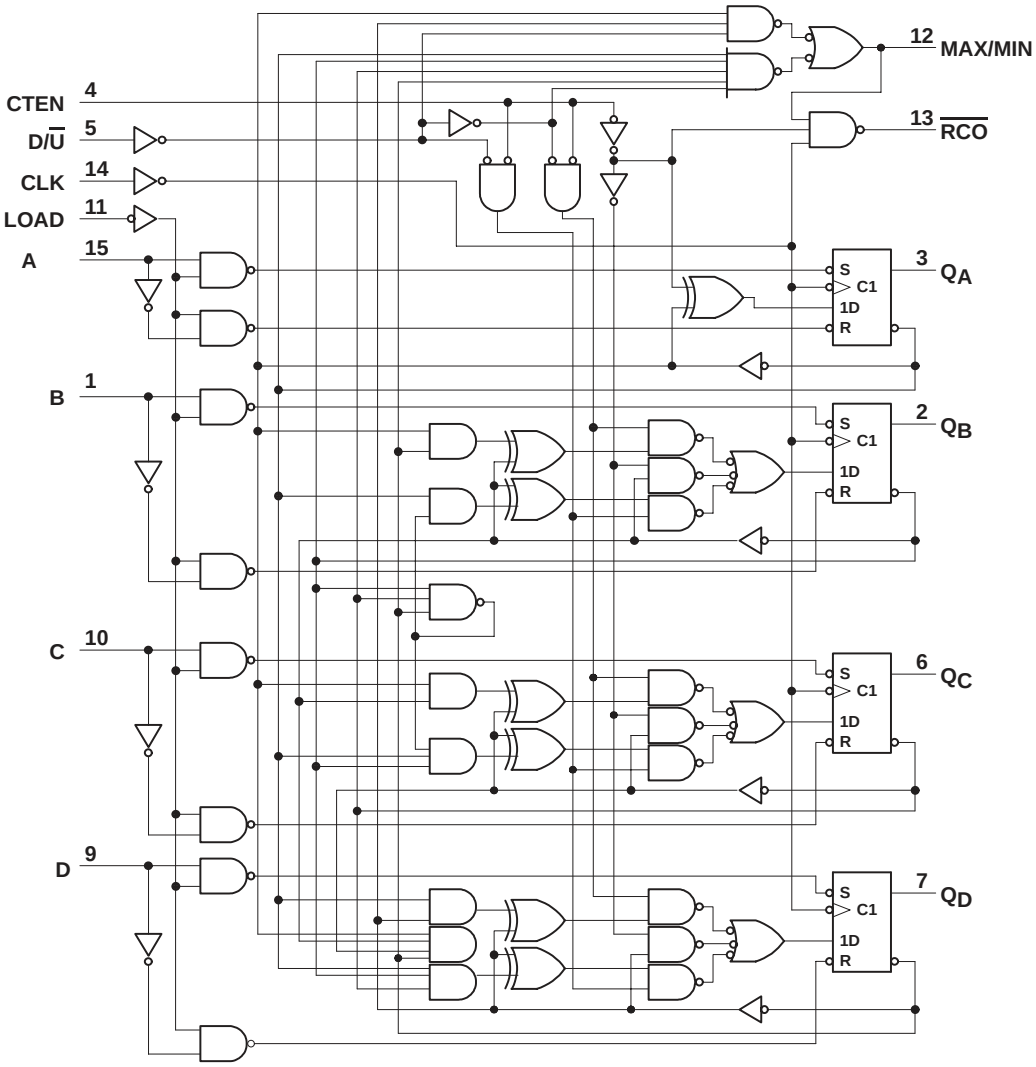


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

'ALS191 logic symbol†



'ALS191 logic diagram (positive logic)



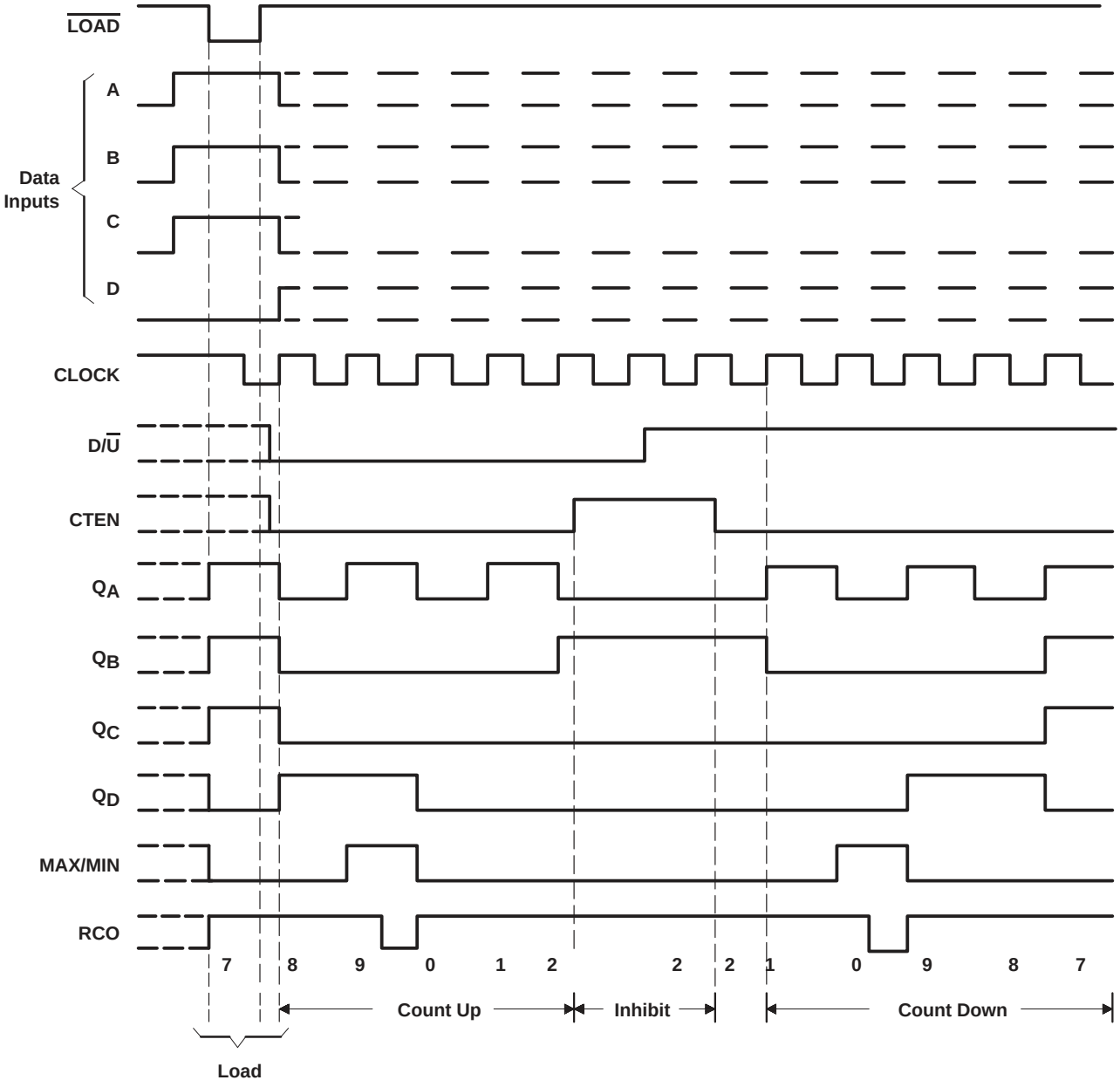
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

typical load, count, and inhibit sequences

'ALS190

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

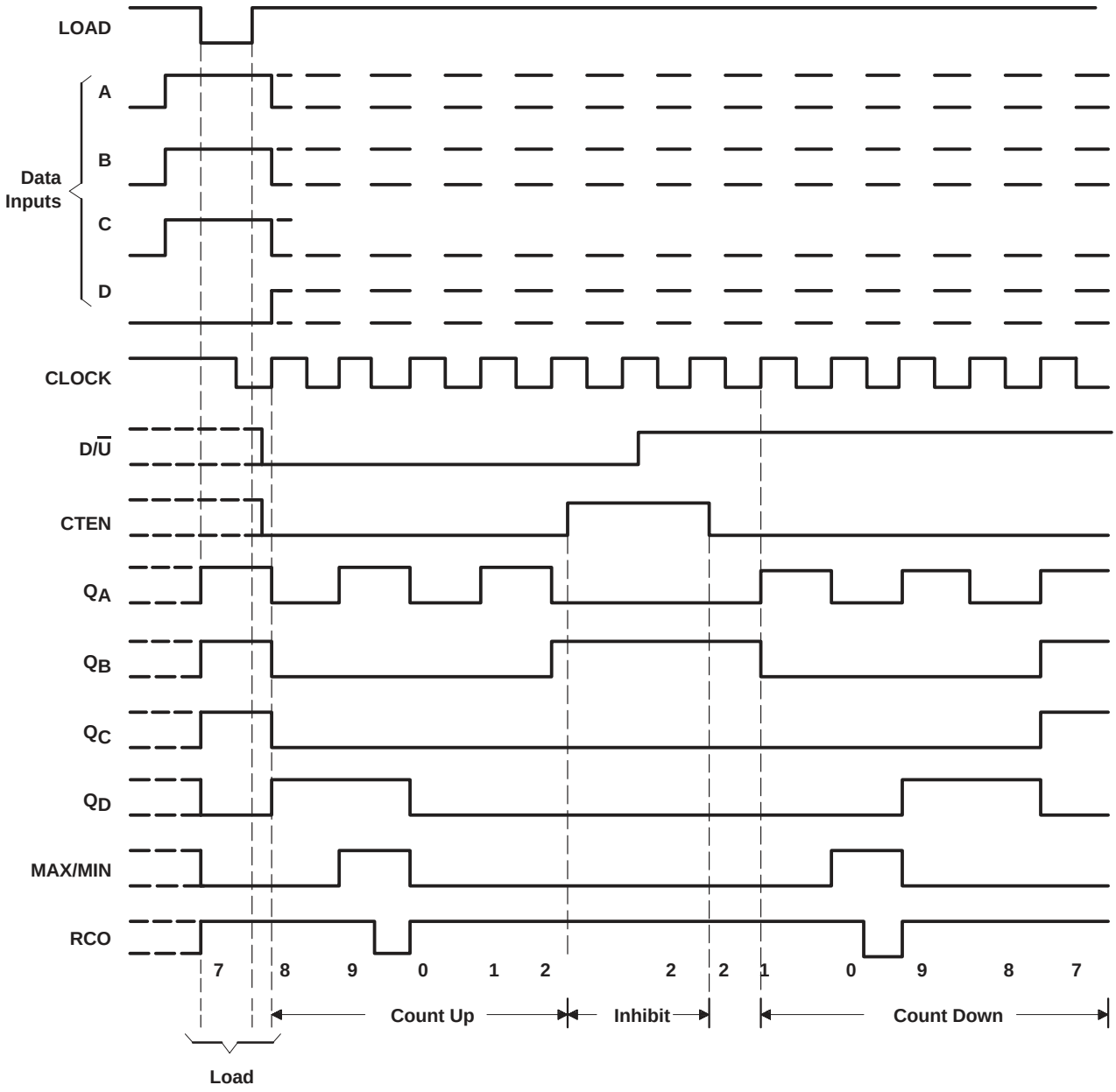


typical load, count, and inhibit sequences

'ALS191

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS190, SN54ALS191 . . . . . –55°C to 125°C
SN74ALS190, SN74ALS191 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

recommended operating conditions

				SN54ALS190 SN54ALS191			SN74ALS190 SN74ALS191			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current					–0.4			–0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency	’ALS190		0		20	0		25	MHz
		’ALS191		0		20	0		30	
t_w	Pulse duration	CLK high or low	’AS190	25			20			ns
			‘AS191	20			16.5			
		$\overline{\text{LOAD}}$ low		25			20			
t_{su}	Setup time	Data before $\overline{\text{LOAD}}\uparrow$		25			20			ns
		$\overline{\text{CTEN}}$ before CLK$\uparrow$		45			20			
		D/$\overline{\text{U}}$ before CLK$\uparrow$		45			20			
		$\overline{\text{LOAD}}$ inactive before CLK$\uparrow$		20			20			
t_{su}	Hold time	Data after $\overline{\text{LOAD}}\uparrow$		5			5			ns
		$\overline{\text{CTEN}}$ after CLK$\uparrow$		0			0			
		D/$\overline{\text{U}}$ after CLK$\uparrow$		0			0			
T_A	Operating free-air temperature			–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS190 SN54ALS191			SN74AAL190 SN74ALS191			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	$\overline{\text{CTEN}}$ OR CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
	All others					–0.1			–0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		– 112	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 0 V		12	22		12	22	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS190 SN54ALS191		SN74ALS190 SN74ALS191		
			MIN	MAX	MIN	MAX	
f_{max}	’ALS190		20		25		MHz
	’ALS191		20		30		
t_{PLH}	$\overline{LOAD}$	Any Q	7	37	8	30	ns
t_{PHL}			8	34	8	30	
t_{PLH}	A, B, C, D	Any Q	4	25	4	21	ns
t_{PHL}			4	25	5	21	
t_{PLH}	CLK	$\overline{RCO}$	5	24	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	3	26	3	18	ns
t_{PHL}			3	22	3	18	
t_{PLH}	CLK	MAX/MIN	8	37	8	31	ns
t_{PHL}			8	34	8	31	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	12	45	15	37	ns
t_{PHL}			10	36	10	28	
t_{PLH}	D/$\overline{U}$	MAX/MIN	8	35	8	25	ns
t_{PHL}			8	30	8	25	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	4	21	4	18	ns
t_{PHL}			4	23	4	18	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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