VTI TECHNOLOGIES

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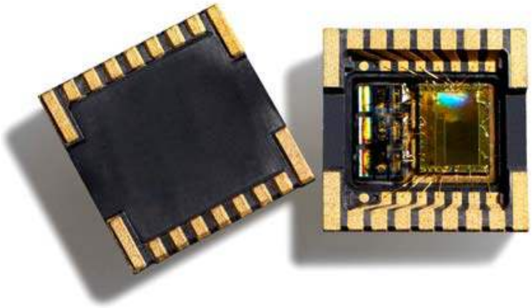
Product Family Specification



SCA3000 Series
3-axis accelerometer

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1 General Description

1.1 Introduction

SCA3000 is a three axis accelerometer family targeted for products requiring high performance with low power consumption. It consists of a 3D-MEMS sensing element and a signal conditioning ASIC packaged into a plastic Molded Interconnection Device package (MID).

A block diagram of the SCA3000 product family is presented in Figure 1 below.

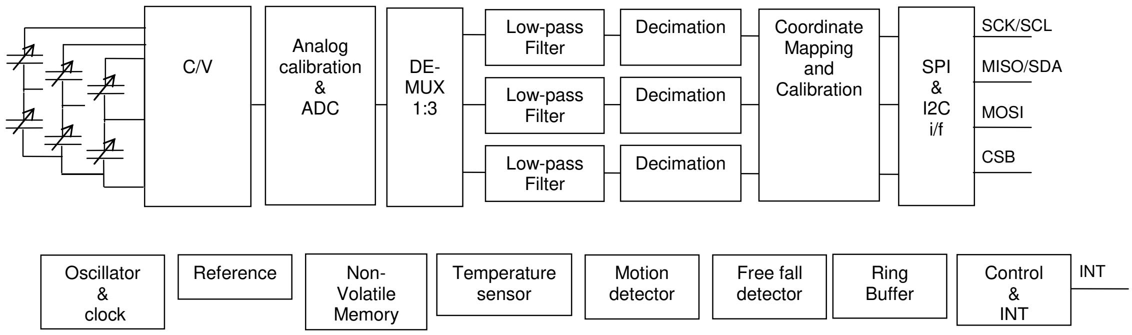

Figure 1. SCA3000 Block Diagram.

This document, no. 8257300, describes the product specification (e.g. operation modes, user accessible registers, electrical properties and application information) for the SCA3000 family. The specification for an individual sensor is available in the corresponding data sheet.

1.2 Functional Description

1.2.1 Sensing element

The sensing element is manufactured using the proprietary bulk 3D-MEMS process, which enables robust, stable and low noise & power capacitive sensors.

The sensing element consists of three acceleration sensitive masses. Acceleration will cause a capacitance change that will be then converted into a voltage change in the signal conditioning ASIC. Due to its mechanical construction, the element's measurement coordinates are rotated 45° compared to the conventional orthogonal X,Y,Z coordinate system.

1.2.2 Interface IC

The sensing element is interfaced via a capacitance-to-voltage (CV) converter. Following calibration in the analog domain, the signal is converted by a successive approximation type of analog-to-digital converter (ADC). The ADC's signal is de-multiplexed into three signal processing channels where it is low-pass filtered and decimated. After that, the signals are mapped into orthogonal coordinates (X-Y-Z) and transferred to the output registers. Depending on the product, the SCA3000 sensor supports either a fully digital serial SPI or I^{2}C interface. In normal measurement mode, acceleration data can be read via the serial bus. Other supported features are a separate motion detection mode and parallel free-fall detection. In these modes, the sensor will generate an interrupt when a pre-defined condition has been met.

The SCA3000 includes an internal oscillator, reference and non-volatile memory that enable the sensor's autonomous operation within a system. The temperature sensor is used in some product applications to enhance the temperature stability. In that case, temperature information can also be read out from the device.

1.2.3 Factory calibration

Sensors are factory calibrated and the trimmed parameters are gain, offset and the frequency of the internal oscillator. Calibration parameters will be read automatically from the internal non-volatile memory during sensor startup.

1.2.4 Supported features

Features supported by individual SCA3000 products are listed in Table 1 below.

Table 1. SCA3000 devices' summary.

Features	SCA3000-D01 (SPI) / SCA3000-D02 (I2C)	SCA3000-E01 (SPI) / SCA3000-E02 (I2C)	SCA3000-E04	SCA3000-E05
Supply voltage	2.35 V – 3.6 V	2.35 V – 3.6 V	2.35 V – 3.6 V	2.35 V – 3.6 V
I/O voltage	1.7 V – 3.6 V	1.7 V – 3.6 V	1.7 V – 3.6 V	1.7 V – 3.6 V
Measuring range	±2 g	±3 g	±6 g	±18 g
Resolution	0.75mg / 0.04°	1mg / 0.06°	2mg / 0.11°	6.25mg / 0.36°
Sensitivity	1333 counts/g	1000 counts/g	500 counts/g	160 counts/g
Output buffer	User enabled, 64 sampl./axis	User enabled, 64 sampl./axis	User enabled, 64 sampl./axis	User enabled, 64 sampl./axis
Motion detection	User enabled	User enabled	User enabled	User enabled
Free fall detection	User enabled	User enabled	User enabled	User enabled
Interface	SPI max 1.6 MHz (-D01) / I^2C fast mode (-D02)	SPI max 325 kHz (-E01) / I^2C std mode (-E02)	SPI max 325 kHz	SPI max 325 kHz
Temperature output	Yes	No	No	No
Clock	Internal	Internal	Internal	Internal

1.2.5 Operation modes

1.2.5.1 Measurement

The SCA3000 is in normal measurement mode by default after start up. The sensor offers acceleration information via the SPI or I^2C when the master requires it. The master can acquire one axis acceleration or all three axis acceleration depending on the application. Measurement resolution depends on the product type (see Table 1).

1.2.5.2 Motion Detection

Motion Detection (MD) mode is intended to be used to save system level power consumption. In this mode, the SCA3000 activates the interrupt via the INT-pin when motion is detected. Sensitivity levels can be configured via the SPI or I^2C bus for each axis. Moreover, the detection condition can be defined using sensitivity directions with AND / OR / mux logic. Once the interrupt has happened, the detected direction can be read out from the corresponding status register.

Normal acceleration information is not available in MD mode.

1.2.6 Free-Fall Detection

Free-Fall Detection (FFD) is intended to be used to save system resources. This feature activates the interrupt via the INT-pin when free-fall is detected. The minimum detectable distance depends on the individual product. Normal acceleration information is available when the FFD is enabled.

1.2.7 Interrupt

The SCA3000 has a dedicated output pin (INT) to be used as the interrupt for the master controller. Interrupt conditions can be activated and deactivated via the SPI or I^2C bus. Once the interrupt has happened, the interrupt source can be read out from the corresponding status register.

1.2.8 Temperature output

Some SCA3000 products provide 9-bit temperature information via the serial interface. See Table 1 for detailed product information.

1.2.9 Output ring buffer

In those applications where real time acceleration information is not needed, the ring buffer memory can be used to buffer acceleration data. This will release µC resources for other tasks or for example, to offer a power saving mode while SCA3000 samples acceleration data into its buffer memory.

Acceleration data is sampled at a constant sample rate by the sensor. The buffer is a FIFO type (First In First Out) where the oldest data is shifted out first. It has separate read and write address pointers, so it can be read and written simultaneously. If the buffer overflows, the oldest data is lost and the new data replaces the oldest samples.

Ring buffer logic can be configured to give an interrupt when the buffer is ½ or ¾ full. The entire ring buffer content can be read by one read sequence.

2 Reset and power up, Operation Modes, HW functions and Clock

2.1 Reset and power up

The SCA3000 has an external active low reset pin. Power supplies must be within the specified range before the reset can be released.

After releasing the reset, the SCA3000 will read configuration and calibration data from the non-volatile memory to volatile registers. Then the SCA3000 will make a check sum calculation to the read memory content. The STATUS register's CSME-bit="0" shows successful memory read operation.

2.2 Measurement Mode

2.2.1 Description

The SCA3000 enters the measurement mode by default after power-on and the CV-converter will start to feed data to the signal channel (Figure 1). Data will be reliable in the output registers after the product specific turn-on time.

The SCA3000 can also be set to optional measurement modes. See component specific data sheets for detailed functional parameters in all measurement modes. All available measurement modes for the SCA3000 are described in Table 2 below.

Table 2. Available measurement modes for SCA3000.

Available measurement modes	SCA3000-D01 SCA3000-D02	SCA3000-E01 SCA3000-E02	SCA3000-E04	SCA3000-E05
Default after power-on or reset	Measurement mode	Measurement mode	Measurement mode	Measurement mode
Optional measurement mode 1	Bypass measurement mode	Narrow band measurement mode	Narrow band measurement mode	Narrow band measurement mode
Optional measurement mode 2	Not available	Not available	Wide band measurement mode	Wide band measurement mode

2.2.1.1 Bypass measurement mode

In bypass measurement mode, the signal bandwidth of the SCA3000 is extended by bypassing the low-pass filter in signal channel. As a result of a wider measurement bandwidth, the noise level is higher.

2.2.1.2 Narrow band measurement mode

In narrow band measurement mode, the signal bandwidth of the SCA3000 is reduced by increasing low-pass filtering in signal channel. In addition, the output data rate is halved due to decimation. As a result of a narrower signal bandwidth, the noise level is lower.

2.2.1.3 Wide band measurement mode

In wide band measurement mode, the SCA3000 signal channel low-pass filtering pass band is widened. As a result of a wider measurement bandwidth, the noise level is higher.

2.2.2 Usage

The optional measurement modes can be enabled by setting the bits called MODE_BITS in MODE register to "010" or "001". See section 3.4 for MODE register details.

Acceleration data can be read from data output registers X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB and Z_MSB in all measurement modes. Each of these registers can be read one by one or using the decrement register read, which is described in section 4.1.3.2 for SPI and 4.2.1.3 for I^2C interface. See section 3.3 for output register details.

2.2.2.1 Overflow condition

Since acceleration data registers have no limiter, the possible overflow needs to be detected using bits [B7, B6, B5]. If bits [B7, B6, B5] are '011' or '100', data overflow has occurred (see Table 3). This applies for all acceleration output registers (X_LSB … Z_MSB and BUF_DATA).

Table 3. Overflow bit patterns in acceleration data registers (X_LSB … Z_MSB and BUF_DATA).

Byte	MSB byte								LSB byte					
Bit number	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2:B0
Acceleration data bit	Sign	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	
Data overflow on positive acceleration	0	1	1	x	x	x	x	x	x	x	x	x	x	xxx
Data overflow on negative acceleration	1	0	0	x	x	x	x	x	x	x	x	x	x	xxx

x = ignore

In case of overflow, the output register value must be discarded. When an overflow is detected, the bit pattern '0101 1111 1111 1xxx' is used for positive accelerations and '1010 0000 0000 0xxx' for negative accelerations until a valid acceleration value is read. In Table 4 the maximum and minimum acceleration register values that are in measuring range (for registers X_LSB … Z_MSB) for SCA3000-D0x and SCA3000-E0x are presented.

Table 4. Maximum and minimum values in the SCA3000 measuring range.

		SCA3000-D01 SCA3000-D02	SCA3000-E01 SCA3000-E02	SCA3000-E04	SCA3000-E05
First positive	[mg]	-	-	-	-
acceleration value	dec	3072	3072	3072	3072
out of range	bin	0110 0000 0000 0xxx	0110 0000 0000 0xxx	0110 0000 0000 0xxx	0110 0000 0000 0xxx
Maximum positive	[mg]	2303.25 mg	3071 mg	6142 mg	19193.75 mg
acceleration value	dec	3071	3071	3071	3071
in range	bin	0101 1111 1111 1xxx	0101 1111 1111 1xxx	0101 1111 1111 1xxx	0101 1111 1111 1xxx
Minimum negative	[mg]	-2304 mg	-3072 mg	-6144 mg	-19200 mg
acceleration value	dec	-3072	-3072	-3072	-3072
in range	bin	1010 0000 0000 0xxx	1010 0000 0000 0xxx	1010 0000 0000 0xxx	1010 0000 0000 0xxx
First negative	[mg]	-	-	-	-
acceleration value	dec	-3073	-3073	-3073	-3073
out of range	bin	1001 1111 1111 1xxx	1001 1111 1111 1xxx	1001 1111 1111 1xxx	1001 1111 1111 1xxx

2.3 Motion Detection Mode

2.3.1 Description

In MD mode, the ADC's data is not fed to the signal processing channel shown in Figure 1 but to the MD block. It consists of a digital band-pass filter (BPF), threshold level programmable digital comparator and a configurable trigger function.

BPF's -3 dB low-pass frequency is 25 Hz …60 Hz and -3 dB high-pass frequency is 0.05 Hz …1 Hz. See Figure 2 below.

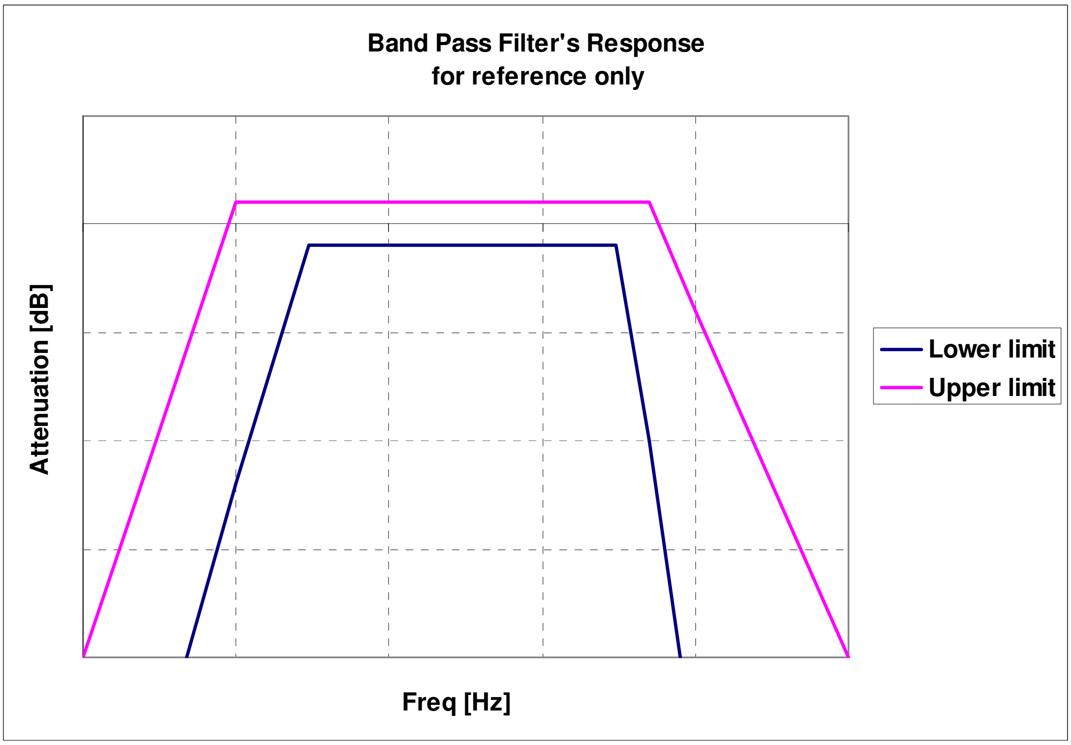

Figure 2. The MD band-pass filter's frequency response.

The absolute value of programmable Threshold Level (TL) is 0 < |TL| < FS g (FS is sensor full scale measuring range). NOTE: Due to power consumption optimization, the step size between each step and axis is not the same, see section 3.4 for threshold level details.

The triggering condition can be defined using OR/AND logic:
1. Any sensing direction can be configured to trigger the interrupt (OR condition).
2. Any sensing direction can be configured to be required to trigger the interrupt (AND condition).

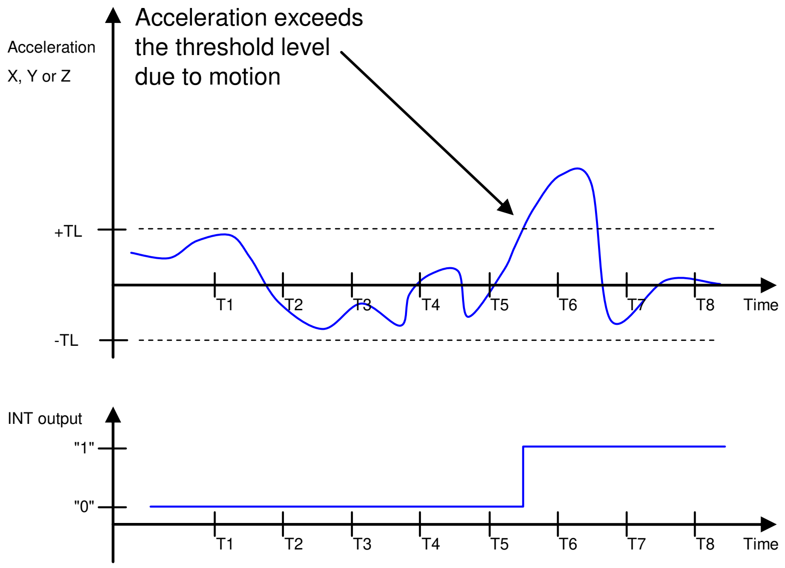

Figure 3. Motion detector operation.

2.3.2 Usage

The MD mode can be enabled by setting the MODE bits in the MODE register to "011". The trigger condition can be defined by setting REQ_Z, REQ_Y, REQ_X, EN_Z, EN_Y and EN_X bits in MD_CTRL register and Z_TH, Y_TH and Z_TH bits in MD_Z_TH, MD_Y_TH and MD_X_TH registers, respectively. See section 3.4 for the configuration register and section 2.7 for the interrupt functionality details.

In MD mode, acceleration data is not available in registers X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB, Z_MSB and BUF_DATA.

2.3.3 Examples

A simple example of motion detection usage:
1. Write "00000011" (03h) into the MODE register (enable motion detection mode, MODE_BITS = '011').
2. Acceleration data is not available when the SCA3000 is in motion detection mode.
3. The INT-pin is activated when motion is detected, see section 2.7 for detailed INT-pin information.

In the next example, the motion detector is configured to give an interrupt on motion only in the X- OR Y-axis direction:
1. Write "00000011" (03h) into MODE register (enable motion detection mode, MODE_BITS = '011')
2. Write "00000000" (00h) into UNLOCK register
3. Write "01010000" (50h) into UNLOCK register
4. Write "10100000" (A0h) into UNLOCK register

(Steps 2–4: Unlock sequence for register lock)

5. Write "00000010" (02h) into CTRL_SEL register (to select indirect MD_CTRL register)
6. Write "00000011" (03h) into CTRL_DATA register (this data is written into MD_CTRL register, enable trigger on Y-channel, EN_Y = '1', enable trigger on X-channel, EN_X = '1')

7. Acceleration data is not available when the SCA3000 is in motion detection mode
8. The INT-pin is activated when motion is detected in the X- or Y-axis direction (Z-axis direction is ignored), see section 2.7 for detailed INT-pin information.

2.4 Free-Fall Detection

2.4.1 Description

During free-fall in the gravitation field, all 3 orthogonal acceleration components are ideally equal to zero. Due to practical non-idealities, detection must be done using Threshold Level (TL) greater than 0.

When enabled, the Free-Fall Detection (FFD) will monitor 8 MSB's of the measured acceleration in the X, Y and Z directions. If the measured acceleration stays within the TL longer than time TFF (Figure 4 below), which corresponds approx 25 cm drop distance, the FFD will generate an interrupt to the INT-pin.

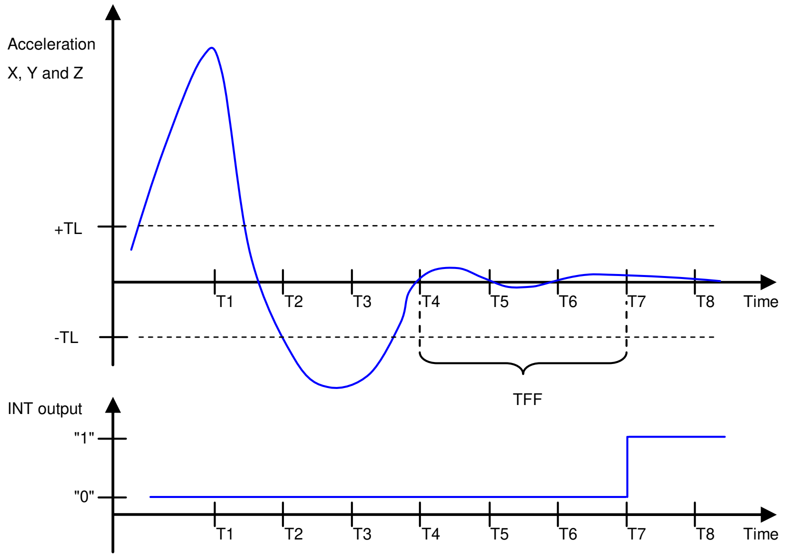

Figure 4. Free Fall condition.

2.4.2 Usage

Free-fall detection can be enabled by setting FFD_EN bit in MODE register to "1". See section 3.4 for MODE register details.

Acceleration data is available in registers X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB, Z_MSB and BUF_DATA as in measurement mode. See section 3.3 for output register and section 2.7 for interrupt functionality details.

2.4.3 Example

A simple example of free-fall detection usage:

1. Write "00010000" (10h) into the MODE register (enable free fall detection, FFD_EN = '1')
2. Acceleration data can be read normally
3. INT-pin is activated when free fall is detected, see section 2.7 for detailed INT-pin information.

2.5 Ring Buffer

2.5.1 Description

The SCA3000's Ring Buffer is a 192 acceleration data samples long (64 samples of 11 bit three axis data) internal memory to relax the real-time operation requirements of the host processor. The following parameters are configurable:

1. Each measurement axis can be individually disabled. If measurement data from e.g. Y-axis is not needed, available memory can be used for X- and Z-axis data.
2. Buffer data length can be changed from 11 to 8 bits. In 8-bit mode, data can be read out using shorter read sequence.
3. Ring buffer's input sample rate can be the same as the sensor's data rate or divided by 2 or 4. When the divider is e.g. 2, only every 2nd acceleration data will be stored.
4. The Interrupt condition, when enabled, can be selected between two: interrupt in INT-pin occurs when the buffer is 50% or 75% full.

2.5.2 Usage

The ring buffer can be enabled by setting BUF_EN bit in MODE register to "1". After enabling the buffer, acceleration data can be read from BUF_DATA register using decrement register read, which is described in section 4.1.3.2 for SPI and 4.2.1.3 for I^{2}C interface.

Each measurement axis can be individually disabled by setting corresponding bits in BUF_X_EN, BUF_Y_EN and BUF_Z_EN in OUT_CTRL register to "0".

Output data length can be changed from 11 bits to 8 bits by setting bit BUF_8BIT in MODE register to "1". See section 3.3 for bit level descriptions.

The count of available data samples in output ring buffer can be read from BUF_COUNT register. Register value is updated only when it is accessed over the SPI or I^{2}C.

Data shift out order is X,Y,Z. In 11 bit mode two bytes must be read to get all 11 bits out. In that case, the MSB byte is 1st. Examples:

1. 11 bits data length, X&Y&Z axis enabled:
   X1_MSB, X1_LSB, Y1_MSB, Y1_LSB, Z1_MSB, Z1_LSB, X2_MSB, X2_LSB, ... latest Z_LSB
2. 11 bits data length, Y&Z axis enabled:
   Y1_MSB, Y1_LSB, Z1_MSB, Z1_LSB, Y2_MSB, Y2_LSB, Z2_MSB, Z2_LSB, Y3_MSB, Y3_LSB, ..., latest Z_LSB
3. 8 bits data length, all axis enabled:
   X1, Y1, Z1, X2, Y2, Z2,..., latest Z
4. 8 bits data length, X&Z axis enabled:
   X1, Z1, X2, Z2, X3, Z3, ..., latest Z
5. 8 bits data length, Z axis enabled:
   Z1, Z2, Z3, ... , latest Z

See section 2.7 for interrupt functionality details.

Acceleration data is available in X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB and Z_MSB when the ring buffer is enabled.

2.5.2.1 Overflow condition

Overflow is detected from data ring buffer in same way as from the output registers. See section 2.2.2.1 for details.

2.5.3 Examples

A simple example of output ring buffer usage:

1. Write "10000000" (C0h) into MODE register (enable output ring buffer, BUF_EN = '1')
2. Acceleration data can be read normally
3. INT-pin is activated when buffer is ½ full, see section 2.7 for detailed INT-pin information.

In the next example, the output Ring Buffer is configured to sample only the Z-axis acceleration data with 8 bit resolution and reduced data rate (only every second sample is stored into output ring buffer). In addition, the SCA3000 is configured to give an interrupt when the output ring buffer is ¾ full:

1. Write "11000000" (C0h) into the MODE register (enable output ring buffer, BUF_EN = '1', set data length to 8 bits, BUF_8BIT = '1')
2. Write "00000000" (00h) into UNLOCK register
3. Write "01010000" (50h) into UNLOCK register
4. Write "10100000" (A0h) into UNLOCK register

   (Steps 2–4: Unlock sequence for register lock)
5. Write "00001011" (0Bh) into CTRL_SEL register (to select indirect OUT_CTRL register)
6. Write "00000101" (03h) into CTRL_DATA register (this data is written into OUT_CTRL register, store Z-axis data, BUF_Z_EN = '1', divide data rate by 2, BUF_RATE = '01')
7. Write "10000001" (81h) into INT_MASK register (set buffer interrupt level to ¾ full, BUF_F_EN = '1', set INT-pin to active high, INT_ACT = '1')
8. Acceleration data can be read normally for all axis and with full resolution. The buffer data can be read from BUF_DATA register
9. INT-pin is activated when the output ring buffer is ¾ full of Z-axis acceleration data, see section 2.7 for detailed INT-pin information.

2.6 Temperature measurement

2.6.1 Usage

Nine bit temperature information is available in the TEMP_MSB and TEMP_LSB registers, if the feature is enabled in the product (see Table 1). The TEMP_MSB register must be read before the TEMP_LSB register in order to get valid temperature data. Registers are updated with the latest temperature data when accessed. See section 3.3 for register details.

The temperature registers' typical output at +23 °C is 256 counts and a 1 °C change in temperature typically corresponds to a 1.8 LSB change in the SCA3000 temperature output. Temperature information is converted to [°C] as follows

Equation 1

$$Temp[°C] = 23°C + \frac{Temp_{dec} - 256LSB}{1.8\frac{LSB}{°C}}$$

where $Temp[°C]$ is temperature in Celsius and $Temp_{dec}$ is the temperature from TEMP_MSB and TEMP_LSB registers in decimal format.

2.7 Interrupt function (INT-pin)

2.7.1 Usage

The Motion Detector and Free Fall Detector will generate an interrupt to INT-pin when the corresponding function is enabled and the interrupt condition is met. The SCA3000's ring buffer will generate an interrupt when interrupt functionality has been enabled. Setting BUF_F_EN bit in INT_MASK register "1" results in interrupt when the register is 75% full. Setting BUF_H_EN bit in INT_MASK register "1" results in interrupt when the register is 50% full.

Setting INT_ALL bit in INT_MASK register will mask all interrupts.

The interrupt polarity (active high/low) can be configured with INT_MASK register's INT_ACT bit.

Once the interrupt has happened, the INT_STATUS register must be read to acknowledge the interrupt.

1. If at least one of MD bits in INT_STATUS register is "1", motion has been detected.
2. If FFD bit in INT_STATUS register is "1", free-fall has been detected.
3. If BUF_FULL bit is "1", Ring Buffer is 75% full. Correspondingly, if BUF_HALF is "1", the Ring Buffer is 50% full.

See section 3.3 for INT_STATUS register details.

2.8 Clock

The SCA3000 has an internal factory trimmed oscillator and clock generator. Internal frequencies vary product by product.

3 Addressing Space

The SCA3000 register contents and bit definitions are described in more detail in the following sections.

3.1 Register Description

The SCA3000 addressing space is presented in Table 5 below.

Table 5. List of registers.

Addr.	Name	Description	Mode (R, W, RW, IA)	Reg. type	Locked
00h	REVID	ASIC revision ID number	R	Conf	
01h		Reserved			-
02h	STATUS	Status register	R	Conf	
03h		Reserved			-
04h	X_LSB	X-axis LSB frame	R	Output	
05h	X_MSB	X-axis MSB frame	R	Output	
06h	Y_LSB	Y-axis LSB frame	R	Output	
07h	Y_MSB	Y-axis MSB frame	R	Output	
08h	Z_LSB	Z-axis LSB frame	R	Output	
09h	Z_MSB	Z-axis MSB frame	R	Output	
0Ah ... 0Eh		Reserved			-
0Fh	BUF_DATA	Ring buffer output register	R	Output	
10h ... 11h		Reserved			-
12h	TEMP_LSB	Temperature LSB frame	R	Output	
13h	TEMP_MSB	Temperature MSB frame	R	Output	
14h	MODE	Operating mode selection, control and configuration for: - mode selection - output buffer - free-fall detection	RW	Conf	
15h	BUF_COUNT	Count of unread data samples in output buffer	R	Output	
16h	INT_STATUS	Interrupt status register: - output buffer is not full, ½ full or ¾ full - free-fall detected / not detected - information of which axis triggered motion	R	Output	
17h	I2C_RD_SEL	Register address for I^{2}C read operation	RW	Conf	
18h	CTRL_SEL	Register address pointer for indirect control registers	RW	Conf	x
19h ... 1Dh		Reserved			-
1Eh	UNLOCK	Unlock register	RW	Conf	
1Fh ... 20h		Reserved			-

Addr.	Name	Description	Mode (R, W, RW, IA)	Reg. type	Locked
21h	INT_MASK	HW interrupt mask register (configures the operation of INT-pin): - interrupt when output buffer is ¾ full (enable / disable) - interrupt when output buffer is ½ full (enable / disable) - mask all interrupts on INT-pin (enable / disable) - INT-pin activity (INT active low / INT active high)	RW, NV	Conf	
22h	CTRL_DATA	Data to/from register which address is in CTRL_SEL (18h) register	RW, NV, IA	Conf	x
23h ... 3Fh		Reserved			-

Add. is the register address in hex format.
RW – Read / Write register, R – Read-only register, NV – Register mirrors NV-memory data (NV = non-volatile).
IA – indirect addressing used.
Registers whose read and write access is blocked by register lock is marked in "Locked" column.

3.2 Non-volatile memory

The SCA3000 has an internal non-volatile memory for calibration and configuration data. Memory content will be programmed during production and is not user configurable. Initial configuration values can be found in the following section 3.4.

3.3 Output Registers

The SCA3000 output registers (marked with 'Output' in Table 5) contents and bit definitions are described in this section. Output registers contain information of measured acceleration and temperature as well as information of the operating state and interrupts of SCA3000.

When reading the output values an MSB register must be read first because MSB register reading latches the data in to all other acceleration output registers

Address: **04h**
Register name: **X_LSB**, X-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis LSB frame

Address: **05h**
Register name: **X_MSB**, X-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis MSB frame

Address: **06h**
Register name: **Y_LSB**, Y-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis LSB frame

Address: **07h**
Register name: **Y_MSB**, Y-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis MSB frame

Address: **08h**
Register name: **Z_LSB**, Z-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis LSB frame

Address: **09h**
Register name: **Z_MSB**, Z-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis MSB frame

Address: **0Fh**
Register name: **BUF_DATA**, ring buffer output register

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Ring buffer output register

Bit level description for acceleration data from X_LSB ... Z_MSB and BUF_DATA registers is presented in Table 6 ... Table 9. Acceleration data is presented in 2's complement format. At 0 g acceleration the output is ideally 00h.

Table 6. Bit level description for acceleration registers of SCA3000-D01 and SCA3000-D02.

Byte	MSB byte								LSB byte					
Bit number Acceleration [mg]	B7 Sign	B6 1536	B5 768	B4 384	B3 192	B2 96	B1 48	B0 24	B7 12	B6 6	B5 3	B4 1.5	B3 0.75	B2:B0 xxx
SCA3000-D01,-D02 [X_LSB…Z_MSB]	s	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	xxx
SCA3000-D01,-D02 Ring buffer in 11-bit mode [BUF_DATA]	s	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	x	x	xxx
SCA3000-D01,-D02 Ring buffer in 8-bit mode [BUF_DATA]	s	d6	d5	d4	d3	d2	d1	d0	x	x	x	x	x	xxx

s = sign bit
x = not used bit

Table 7. Bit level description for acceleration registers of SCA3000-E01 and SCA3000-E02.

Byte	MSB byte								LSB byte					
Bit number Acceleration [mg]	B7 Sign	B6 2048	B5 1024	B4 512	B3 256	B2 128	B1 64	B0 32	B7 16	B6 8	B5 4	B4 2	B3 1	B2:B0 xxx
SCA3000-E01,-E02 [X_LSB…Z_MSB]	s	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	xxx
SCA3000-E01,-E02 Ring buffer in 11-bit mode [BUF_DATA]	s	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	x	x	xxx
SCA3000-E01,-E02 Ring buffer in 8-bit mode [BUF_DATA]	s	d6	d5	d4	d3	d2	d1	d0	x	x	x	x	x	xxx

s = sign bit
x = not used bit

Table 8. Bit level description for acceleration registers of SCA3000-E04.

Byte	MSB byte								LSB byte					
Bit number Acceleration [mg]	B7 Sign	B6 4096	B5 2048	B4 1024	B3 512	B2 256	B1 128	B0 64	B7 32	B6 16	B5 8	B4 4	B3 2	B2:B0 xxx
SCA3000-E04 [X_LSB…Z_MSB]	s	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	xxx
SCA3000-E04 Ring buffer in 11-bit mode [BUF_DATA]	s	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	x	x	xxx
SCA3000-E04 Ring buffer in 8-bit mode [BUF_DATA]	s	d6	d5	d4	d3	d2	d1	d0	x	x	x	x	x	xxx

s = sign bit
x = not used bit

Table 9. Bit level description for acceleration registers of SCA3000-E05.

Byte	MSB byte								LSB byte					
Bit number Acceleration [mg]	B7 Sign	B6 12800	B5 6400	B4 3200	B3 1600	B2 800	B1 400	B0 200	B7 100	B6 50	B5 25	B4 12.5	B3 6.25	B2:B0 xxx
SCA3000-E05 [X_LSB…Z_MSB]	s	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	xxx
SCA3000-E05 Ring buffer in 11-bit mode [BUF_DATA]	s	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	x	x	xxx
SCA3000-E05 Ring buffer in 8-bit mode [BUF_DATA]	s	d6	d5	d4	d3	d2	d1	d0	x	x	x	x	x	xxx

s = sign bit
x = not used bit

Address: **12h**
Register name: **TEMP_LSB**, temperature LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	TEMP	Temperature LSB frame

Address: **13h**
Register name: **TEMP_MSB**, temperature MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	TEMP	Temperature MSB frame

The bit level description for temperature data from TEMP_MSB and TEMP_LSB registers is presented in Table 10. Temperature data is presented in unsigned format. The LSB bit (bit B5 or t0 in Table 10) weight is ~0.56°C. See section 2.6 for more detailed information of converting the data to temperature in [°C].

Table 10. Bit level description for temperature registers [TEMP_MSB … TEMP_LSB].

Register	TEMP_MSB							TEMP_LSB			
Bit number	B7:B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4:B0
Bit in temperature register	xx	t8	t7	t6	t5	t4	t3	t2	t1	t0	xxxxx

x = not used bit

Address: **15h**
Register name**: BUF_COUNT**, output ring buffer status

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	COUNT	Count of available data samples in output ring buffer, for more information see section 2.5.2.

Address: **16h**
Register name: **INT_STATUS**, interrupt status register (all interrupts that are available in current operation mode)

Bits	Mode	Initial Value	Name	Description
7	R	0	BUF_FULL	Output ring buffer is ¾ full 1 – Ring buffer is ¾ full 0 – Ring buffer is not full
6	R	0	BUF_HALF	Output ring buffer is ½ full 1 – Ring buffer is ½ full 0 – Ring buffer is not full
5:4				Reserved
3	R	0	FFD	Free-fall detection 1 – Free-fall detected (0 g acceleration) 0 – Free-fall not detected
2:0	R	000	MD	Motion detector triggered channel indication 1xx – Trigger on Y-axis x1x – Trigger on X-axis xx1 – Trigger on Z-axis

3.4 Configuration Registers

SCA3000 configuration register (marked with 'Conf' in Table 5) contents and bit definitions are described in this section. Configuration registers are used to configure SCA3000 operation and the operation parameters.

Address: **00h**
Register name: **REVID**, ASIC revision ID number tied in metal

Bits	Mode	Initial Value	Name	Description
7:4	R	2h	REVMAJ	Major revision number
3:0	R	1h	REVMIN	Minor revision number

Address: **02h**
Register name: **STATUS**, status register

Bits	Mode	Initial Value	Name	Description
7:6				Reserved
5	R	0	LOCK	Status of lock register 0 – Lock is closed 1 – Lock is open
4:2				Reserved
1	R	0	CSME	EEPROM checksum error 1 – EEPROM checksum error 0 – No error
0	R	0	SPI_FRAME	SPI frame error. Bit is reset, when next correct SPI frame is received (only for products with SPI bus). 1 – SPI frame error 0 – No error

Address: **14h**
Register name: **MODE**, operation mode selection

Bits	Mode	Initial Value	Name	Description
7	RW	0	BUF_EN	Output ring buffer 1 – Enabled 0 – Disabled (Buffer in power down)
6	RW	0	BUF_8BIT	Output ring buffer data length 1 – Ring buffer is read in single 8 bit frame per stored axis (8 bit mode) 0 – Ring buffer is read in two 8 bit frames per stored axis (11 bit mode). Unused bits are set to 0.
5				Reserved
4	RW	0	FFD_EN	Free-fall detection 1 – Enabled 0 – Disabled (detection in power down)
3				Reserved
2:0	RW	000	MODE_BITS	Selects SCA3000 series operation mode 000 – Normal measurement mode 010 – Optional measurement mode 1 (see Table 2) 001 – Optional measurement mode 2 (see Table 2) 011 – MD, Motion Detector Other combinations are reserved

Address: **17h**
Register name: **I2C_RD_SEL**, register address for I^2C read operation

Bits	Mode	Initial Value	Name	Description
7:0	W	00h	ADDR	Address of register to be read via I^2C. Register is used only for I^2C read access.

Address: **18h**
Register name: **CTRL_SEL**, Control register selector, **UNLOCK REQUIRED**

Bits	Mode	Initial Value	Name	Description
7:5	RW	000		Reserved
4:0	RW	00000	SELECT	Indirect control registers, select register address for read / write access: 00001 – I2C_DISABLE 00010 – MD_CTRL (Motion Detector control) 00011 – MD_Y_TH (Motion Detector Y-threshold) 00100 – MD_X_TH (Motion Detector X-threshold) 00101 – MD_Z_TH (Motion Detector Z-threshold) 01011 – OUT_CTRL (Output control) Other combinations are reserved

CTRL_SEL register works as an address pointer for registers listed below. When this register is written the content of selected register is available for reading/writing from/to register CTRL_DATA.

Address value: **00010**
Register name: **MD_CTRL**, Motion Detector control (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description	Note
7:6			Reserved	
5	0	REQ_Z	1 – Require trigger on Z-channel 0 – Not required	Bits 5:3 can be used to build logical AND operation between channels. Example: X and Y = Require X and Y, ignore Z → 00 011 011
4	0	REQ_X	1 – Require trigger on X-channel 0 – Not required	
3	0	REQ_Y	1 – Require trigger on Y-channel 0 – Not required	
2	1	EN_Z	1 – Enable trigger on Z-channel 0 – Not required	Bits 2:0 can be used to build logical OR operation between channels. Example: X or Y = Disable Z → 00 000 011
1	1	EN_X	1 – Enable trigger on X-channel 0 – Not required	
0	1	EN_Y	1 – Enable trigger on Y-channel 0 – Not required	

Address value: **00011**
Register name: **MD_Y_TH**, Motion Detector Y-threshold (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:0	10h or 08h	Y_TH	Threshold for Y-acceleration change when MD is used.

Address value: **00100**
Register name: **MD_X_TH**, Motion Detector X-threshold (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:0	10h or 08h	X_TH	Threshold for X-acceleration change when MD is used.

Address value: **00101**
Register name: **MD_Z_TH**, Motion Detector Z-threshold (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:0	10h or 08h	Z_TH	Threshold for Z-acceleration change when MD is used.

Initial values for registers MD_X_TH, MD_Y_TH and MD_Z_TH vary with SCA3000 product types. Initial value is:

- 10h for SCA3000-D01, SCA3000-D02, SCA3000-E01 and SCA3000-E02
- 08h for SCA3000-E04 and SCA3000-E05

The bit level descriptions for registers MD_X_TH, MD_Y_TH and MD_Z_TH are presented in, Table 11 ...Table 14 below. The threshold levels are in unsigned format and they are absolute values for the acceleration that triggers the motion detector interrupt. Values presented below are typical threshold values and they are not factory calibrated.

Table 11. Bit level description for motion detector typical threshold levels (SCA3000-D01 and SCA3000-D02).

	Typical bit weights							
Bit number	B7	B6	B5	B4	B3	B2	B1	B0
SCA3000-D01, -D02 Acceleration [mg] **MD_X_TH, MD_TH_Z**	x	x	1300	650	350	200	100	50
SCA3000-D01, -D02 Acceleration [mg] **MD_Y_TH**	x	1750	850	450	250	150	100	50

x = not used bit

Table 12. Bit level description for motion detector typical threshold levels (SCA3000-E01 and SCA3000-E02).

	Typical bit weights							
Bit number	B7	B6	B5	B4	B3	B2	B1	B0
SCA3000-E01, -E02 Acceleration [mg] **MD_X_TH, MD_TH_Z**	x	x	2050	1050	550	300	150	100
SCA3000-E01, -E02 Acceleration [mg] **MD_Y_TH**	x	2700	1350	700	350	200	100	50

x = not used bit

Table 13. Bit level description for motion detector typical threshold levels (SCA3000-E04).

	Typical bit weights							
Bit number	B7	B6	B5	B4	B3	B2	B1	B0
SCA3000-E04 Acceleration [mg] **MD_X_TH, MD_TH_Z**	x	x	4100	2100	1100	600	300	200
SCA3000-E04 Acceleration [mg] **MD_Y_TH**	x	5400	2700	1400	700	400	200	100

x = not used bit

Table 14. Bit level description for motion detector typical threshold levels (SCA3000-E05).

	Typical bit weights							
Bit number	B7	B6	B5	B4	B3	B2	B1	B0
SCA3000-E05 Acceleration [mg] **MD_X_TH, MD_TH_Z**	x	x	11900	6100	3200	1700	900	600
SCA3000-E05 Acceleration [mg] **MD_Y_TH**	x	15600	7800	4100	2000	1200	600	300

x = not used bit

Address value: **01011**
Register name: **OUT_CTRL**, Output configuration (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:5			Reserved
4	1	BUF_X_EN	Store X-axis acceleration data to ring buffer 1 – enabled 0 – disabled
3	1	BUF_Y_EN	Store Y-axis acceleration data to ring buffer 1 – enabled 0 – disabled
2	1	BUF_Z_EN	Store Z-axis acceleration data to ring buffer 1 – enabled 0 – disabled
1:0	00	BUF_RATE	Additional data rate reduction after calibration before data is loaded to ring buffer (no effect on output registers data rate, see section 2.5.1) 11 – No rate reduction 10 – divide rate by 4 01 – divide rate by 2 00 – No rate reduction

Address: **1Eh**
Register name: **UNLOCK**, Unlock register lock

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	KEY	Lock can be opened by writing the following sequence into this register: 00h, 50h, A0h Writing any other sequence closes the lock. Lock state can be read from STATUS register.

Address: **21h**
Register name: **INT_MASK**, HW interrupt mask register configures the operation of the INT pin.

Bits	Mode	Initial Value	Name	Description
7	RW	0	BUF_F_EN	Interrupt when output ring buffer is ¾ full 1 – Enabled 0 – Disabled
6	RW	1	BUF_H_EN	Interrupt when output ring buffer is ½ full 1 – Enabled 0 – Disabled
5:2				Reserved
1	RW	0	INT_ALL	Mask all interrupts (only effects on the INT-pin) 1 – Mask all interrupts (including free fall detection and motion detector) 0 – Mask interrupts according to configured mode
0	RW	1	INT_ACT	INT-pin signal activity 1 – INT active high (INT-pin high) 0 – INT active low (INT-pin low)

Address: **22h**
Register name: **CTRL_DATA**, Control register data, **UNLOCK REQUIRED**

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	DATA	Data bits [7:0] of selected 8-bit control register. Write this register to actually perform the write operation to selected location. See register CTRL_SEL for information on register contents.

4 Serial Interfaces

Communication between the SCA3000 sensor and master controller is based on serial data transfer and a dedicated interrupt line (INT-pin). Two different serial interfaces are available for the SCA3000 sensor: SPI and I^2C (Phillips specification V2.1). However, only one per product is enabled by pre-programming in the factory. The SCA3000 acts as a slave on both the SPI and I^2C bus.

4.1 SPI Interface

SPI bus is a full duplex synchronous 4-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the SPI clock, and the slave as any integrated circuit receiving the SPI clock from the master. The SCA3000 sensor always operates as a slave device in master-slave operation mode. A typical SPI connection is presented in Figure 5.

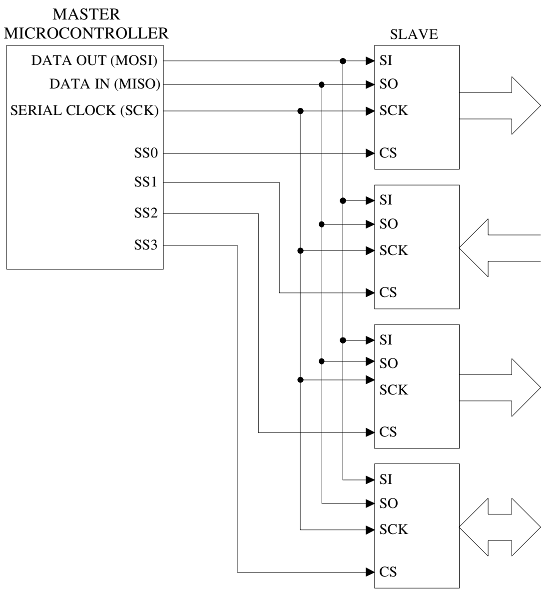

Figure 5. Typical SPI connection.

The data transfer uses the following 4-wire interface:

MOSI	master out slave in	μC → SCA3000
MISO	master in slave out	SCA3000 → μC
SCK	serial clock	μC → SCA3000
CSB	chip select (low active)	μC → SCA3000

4.1.1 SPI frame format

SCA3000 SPI frame format and transfer protocol is presented in Figure 6.

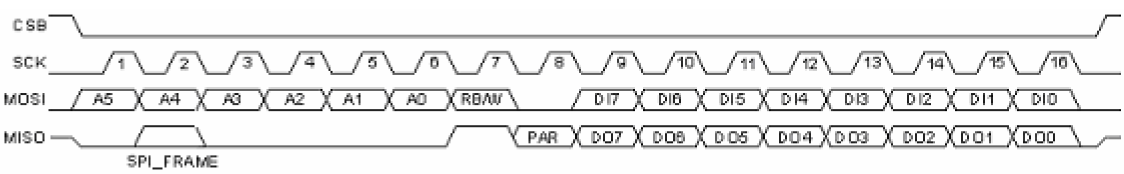

Figure 6. SPI frame format.

Each communication frame contains 16 bits. The first 8 bits in MOSI line contains info about the operation (read/write) and the register address being accessed. The first 6 bits define the 6 bit address for the selected operation, which is defined by bit 7 (‘0’ = read ‘1’ = write), which is followed by one zero bit. The later 8 bits in the MOSI line contain data for a write operation and are ‘don’t-care’ for a read operation. Bits from MOSI line are sampled in on the rising edge of SCK and bits to MISO line are latched out on falling edge of SCK.

The first bits in the MISO line are the frame error bit (SPI_FRAME, bit 2) of the previous SPI frame and odd parity bit (PAR, bit 8). Parity is calculated from data which is currently sent. Bit 7 is always ‘1’. The later 8 bits contain data for a read operation. During the write operation, these data bits are previous data bits of the addressed register.

For write commands, data is written into the addressed register on the rising edge of CSB. If the command frame is invalid as described in the section data will not be written into the register (please see "error conditioning" in section 4.1.2).

For read commands, data is latched into the internal SPI output register (shift register) on the 8th rising edge of SCK. The output register is shifted out MSB first over MISO output.

When the CSB is high state between data transfers, the MISO line is in the high-impedance state.

4.1.2 SPI bus error conditioning

While sending an SPI frame, if the CSB is raised to 1

- before sending 16 SCKs or
- the number of SCK pulses is not divisible by 8,

the frame error is activated and the frame is considered invalid. The status bit STATUS.SPI_FRAME is set to indicate the frame error condition. During the next SPI, the frame error bit is sent out as SPI_FRAME bit (see SPI_FRAME in MISO line in Figure 6). STATUS.SPI_FRAME bit is reset, if correct frame is received.

When an invalid frame is received, the last command is simply ignored and the register contents are left unchanged. If frame error happens while sending multiple samples in ring buffer mode, only the last output value is considered invalid.

4.1.3 Examples of SPI communication

4.1.3.1 Example of register read

An example of 11 bit X-axis acceleration read command is presented in Figure 7. The master gives the register address to be read via the MOSI line: '05' in hex format and '000101' in binary format, register name is X_MSB (X-axis MSB frame). 7th bit is set to '0' to indicate the read operation.

The sensor replies to a requested operation by transferring the register content via MISO line. After transferring the asked X_MSB register content, the master gives next register address to be read: '04' in hex format and '000100' in binary format, register name is X_LSB (X-axis LSB frame). The sensor replies to the requested operation by transferring the register content MSB first.

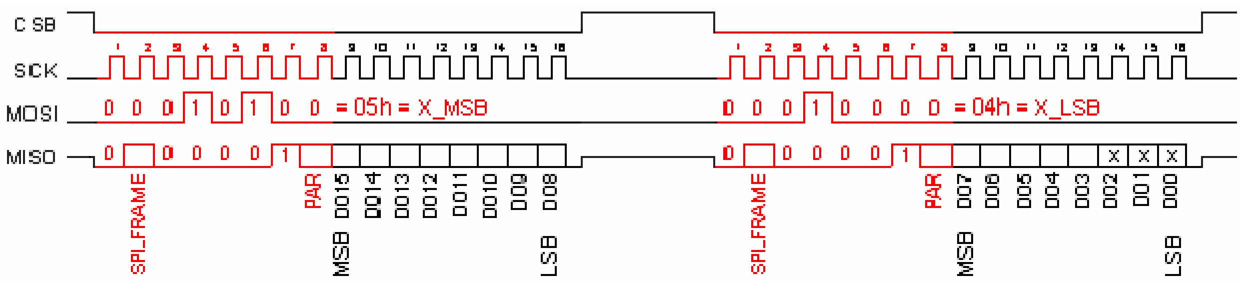

Figure 7. An example of SPI read communication.

4.1.3.2 Example of decremented register read

Figure 8 presents a decremented read operation where the content of four output registers is read by one SPI frame. After normal register addressing and one register content reading, the µC keeps the CSB line low and continues supplying the SCK pulses. After every 8 SCK pulses, the output data address is decremented by one and the previous acceleration output register's content is shifted out without parity bits. The parity bit in Figure 4 is calculated and transferred only for the first data frame. From the X_LSB register address, the SCA3000 jumps to Z_MSB. Decremented reading is possible only for registers X_LSB ... Z_MSB.

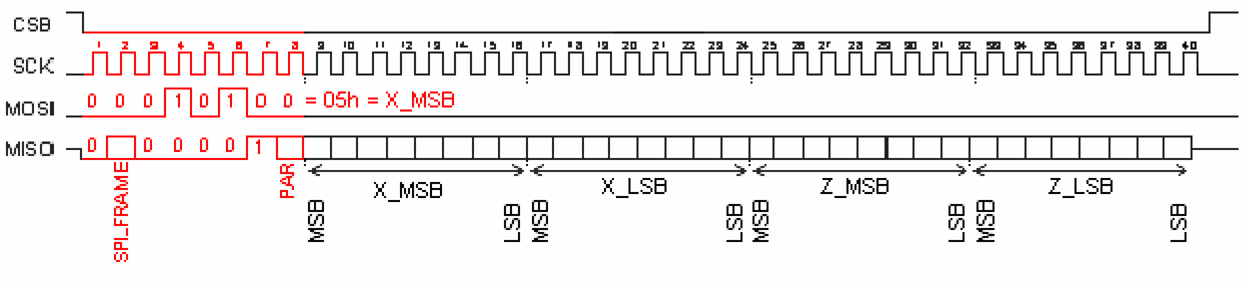

Figure 8. An example of decremented read operation.

4.1.3.3 Example of ring buffer read

An example of output ring buffer read by one SPI frame (ring buffer data length 8 bits) is presented in Figure 9. The whole ring buffer read procedure is very similar to decremented read described above. The output ring buffer is addressed (register name BUF_DATA). The SCA3000 sensor continues shifting out the ring buffer content as long as µC continues supplying the SCK pulses.

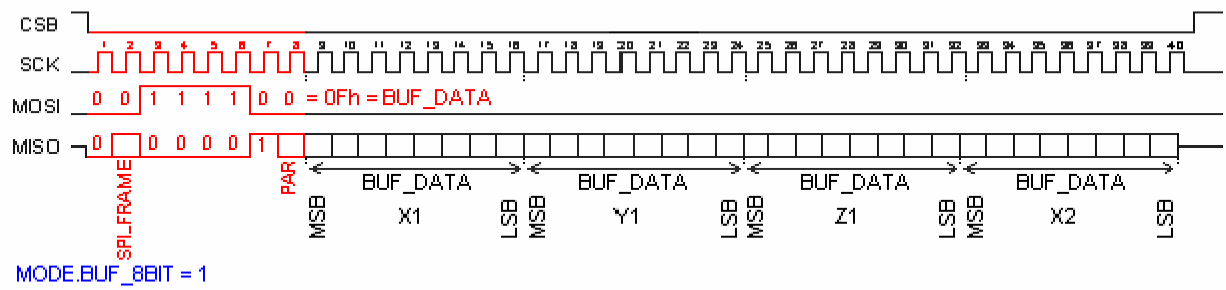

Figure 9. An example of output ring buffer read operation.

4.2 I²C Interface

I²C is a 2-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the serial clock (SCL), and the slave as any integrated circuit receiving the SCL clock from the master. The SCA3000 sensor always operates as a slave device in master-slave operation mode. When using an SPI interface, a hardware addressing is used (slaves have dedicated CSB signals), the I²C interface uses a software based addressing (slave devices have dedicated bit patterns as addresses).

The SCA3000 is compatible to the Philips I²C specification V2.1. Main used features of the I²C interface are:

- 10-bit addressing, SCA3000 I²C device address is 0x1F1
- Supports standard mode and fast mode
- Start / Restart / Stop
- Slave transceiver mode
- Designed for low power consumption

In addition to the Philips specification, the SCA3000 I²C interface supports multiple write and read mode.

4.2.1 I²C frame format

4.2.1.1 I²C write mode

In I²C write mode, the first 8 bits after device address define the SCA3000 internal register address to be written. If multiple data words are transferred by the master, the register address is decreased automatically by one (see cases 1 and 2 in Figure 10).

4.2.1.2 I²C read mode

The read mode operates as described in Philips I²C specification. I²C read operation returns the content of the register which address is defined in I2C_RD_SEL register. So when performing the I²C read operation, the register address to be read has to be written into I2C_RD_SEL register before actual read operation. Read operation starts from register address that has been written earlier in I2C_RD_SEL register. Read data is acknowledged by I²C master. Automatic read address change depends on the selected start address (see cases 3 and 4 in Figure 10).

- If address is some of registers between X_LSB → Z_MSB the register address is automatically cycled as follows:
  ... →Y_MSB → Y_LSB → X_MSB → X_LSB → Z_MSB → Z_LSB → Y_MSB → Y_LSB → ...
- If the start address is any other register, the read address is NOT automatically incremented or decremented (the data transfer continues from the same address.) This enables the burst read from output ring buffer (register BUF_DATA).

4.2.1.3 Decremented register read

Decremented reading is possible only for registers X_LSB ... Z_MSB. Refer to decremented read with SPI interface section 4.1.3.2.

4.2.2 Examples of I²C communication

Examples of I²C communication are presented below in Figure 10.

Read/write select bit (0=write, 1=read)

CASE 1: I2C 8 bit write

S	device addr 1st byte 11110AA	0	SA	device addr 2nd byte AAAAAAAA	SA	register addr 8 bits, MSB first	SA	register data 8 bits, MSB first	SA	E

CASE 2: I2C 16 bit write (any number of bytes can be written, length is determined by end condition generated by master)

S	device addr 1st byte 11110AA	0	SA	device addr 2nd byte AAAAAAAA	SA	register addr 8 bits, MSB first	SA	register data, addr + 0 8 bits, MSB first	SA	register data, addr - 1 8 bits, MSB first	SA	E

CASE 3: I2C 8 bit read, read address for SCA3000 series register should be written to I2C_RD_SEL register

S	device addr 1st byte 11110AA	0	SA	device addr 2nd byte AAAAAAAA	SA	RS	device addr 1st byte 11110AA	1	SA	register data, *addr* 8 bits, MSB first	MA	E

CASE 4: I2C 16 bit read (any number of bytes can be read, length is determined by end condition generated by master).
Automatic register address changing depends on selected start address in I2C_RD_SEL (noted by *addr* and *addr_x* on the figure).

S	device addr 1st byte 11110AA	0	SA	device addr 2nd byte AAAAAAAA	SA	RS	device addr 1st byte 11110AA	1	SA	register data, *addr* 8 bits, MSB first	MA	register data, *addr_x* 8 bits, MSB first	MA	E

S = Start condition
RS = Repeated start condition
E = End condition
SA = Slave Acknowledgement
MA = Master Acknowledgement
AA = Device address, 10 bits

Figure 10. I²C frame format.

5 Electrical Characteristics

All voltages are reference to ground. Currents flowing into the circuit have positive values.

5.1 Absolute maximum ratings

The absolute maximum ratings of the SCA3000 are presented in Table 15 below.

Table 15. Absolute maximum ratings of the SCA3000

Parameter	Value	Unit
Supply voltage (V_{dd})	-0.3 to +3.6	V
Voltage at input / output pins	-0.3 to (V_{dd} + 0.3)	V
ESD (Human body model)	±2	kV
Storage temperature	-40 ... +125	°C
Storage / operating temperature	-40 ... +85	°C
Mechanical shock *	> 10 000	g
Ultrasonic cleaning	Not allowed	

* 1 m drop on concrete may cause >>10000 g shock.

ULTRASONIC AGITATION NOT ALLOWED.

5.2 Power Supply

Please refer to the corresponding product datasheet.

5.3 Digital I/O Specification

5.3.1 Digital I/O DC characteristics

Table 16. DC characteristics of digital I/O pins.

No.	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input: CSB, MOSI, Xreset, SCK_SCL has no pull up / pull down							
1	Pull up current: CSB	V_{IN} = 0 V	I_{PU}	10		50	µA
2	Pull down current: MOSI	V_{IN} = Dvio	I_{PD}	10		50	µA
3	Pull up current Xreset	V_{IN} = 0 V	I_{PU}	3		10	µA
4	Input high voltage		V_{IH}	0.7*Dvio			V
5	Input low voltage		V_{IL}			0.3*Dvio	V
6	Hysteresis		V_{HYST}	0.1*Dvio			V
Output terminal: MISO_SDA, INT							
7	Output high voltage	I > -4 mA	V_{OH}	0.8*Dvio		Dvio	V
8	Output low voltage	I < 4 mA	V_{OL}	0		0.2*Dvio	V
9	Tristate leakage	0 < V_{MISO} < 2.7 V	I_{LEAK}	-2		2	µA

5.3.2 Digital I/O level shifter

All the SCA3000 products have an internal level shifter that can be used to interface e.g. a micro controller using lower supply than the SCA3000. The level shifter is "programmed" by providing the supply voltage of the interfaced device to the DVIO-pin. Please refer to the corresponding product data sheet for details.

5.3.3 SPI AC characteristics

The AC characteristics of the SCA3000 SPI interface are defined in Figure 11 and in Table 17.

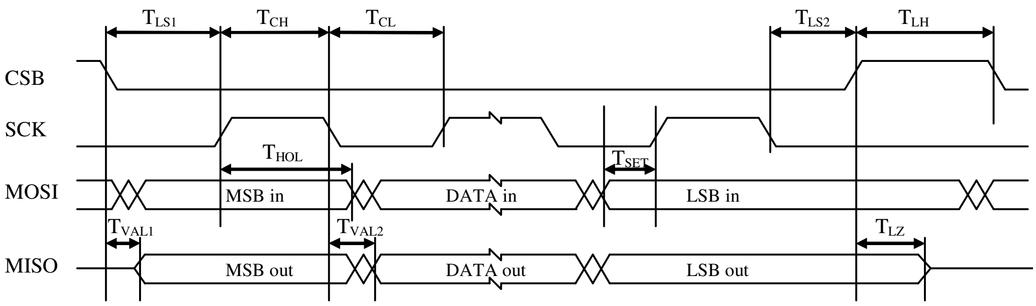

Figure 11. Timing diagram for SPI communication.

Table 17. AC characteristics of SPI communication.

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Terminal CSB, SCK							
1	Time from CSB (10%) to SCK (90%)1		T_{LS1}	$T_{per}/2$			ns
2	Time from SCK (10%) to CSB (90%)1		T_{LS2}	$T_{per}/2$			ns
Terminal SCK							
3	SCK low time	Load capacitance at MISO < 35 pF	T_{CL}	0.80* $T_{per}/2$	$T_{per}/2$		ns
4	SCK high time	Load capacitance at MISO < 35 pF	T_{CH}	0.80* $T_{per}/2$	$T_{per}/2$		ns
5	SCK Frequency		fsck = $1/T_{per}$			Product specific	MHz
Terminal MOSI, SCK							
6	Time from changing MOSI (10%, 90%) to SCK (90%)1. Data setup time		T_{SET}	$T_{per}/4$			ns
7	Time from SCK (90%) to changing MOSI (10%, 90%)1. Data hold time		T_{HOL}	$T_{per}/4$			ns
Terminal MISO, CSB							
8	Time from CSB (10%) to stable MISO (10%, 90%)	Load capacitance at MISO < 35 pF	T_{VAL1}			$T_{per}/4$	ns
9	Time from CSB (90%) to high impedance state of MISO1.	Load capacitance at MISO < 35 pF	T_{LZ}			$T_{per}/4$	ns
Terminal MISO, SCK							
10	Time from SCK (10%) to stable MISO (10%, 90%)1.	Load capacitance at MISO < 35 pF	T_{VAL2}			$1.3 \cdot T_{per}/4$	ns

Terminal MOSI, CSB				
11	Time between SPI cycles, CSB at high level (90%)	T_{LH}	$4 \cdot T_{per}$	ns

T_{per} is SCK period

5.3.4 I²C AC characteristics

Please, see Phillips Semiconductors, The I²C bus specification, Version 2.1, January 2000, pp. 31-33.

6 Package Characteristics

6.1 Dimensions

The package dimensions are presented in Figure 12 below (dimensions in millimeters [mm] with ±50 µm tolerance).

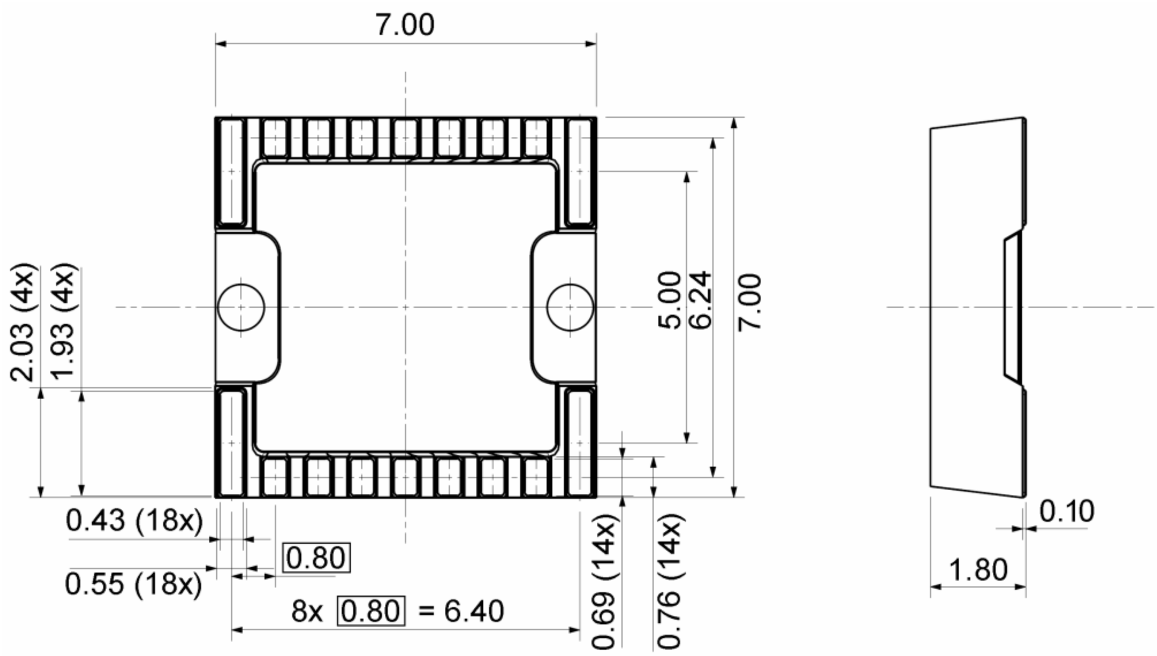

Figure 12. SCA3000 package dimensions.

7 Application information

7.1 Pin Description

SCA3000 pin numbers are presented in Figure 14 below and pin descriptions in Table 18.

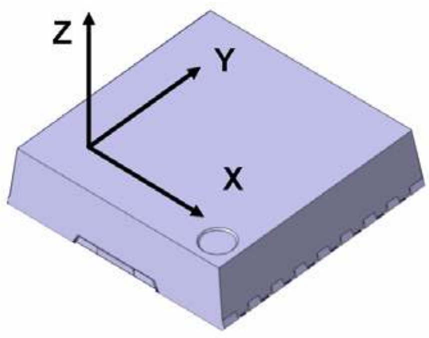

Figure 13. SCA3000 sensing directions.

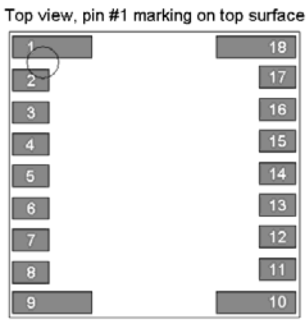

Figure 14. SCA3000 pin numbers.

Table 18. SCA3000 pin descriptions.

Pin #	Name	SCA3000-D01, SCA3000-E01, SCA3000-E04	SCA3000-D02, SCA3000-E02
1	NC	Not connected	Not connected
2	XRESET	External reset, active low	External reset, active low
3	INT	Interrupt output	Interrupt output
4	CLK	Connect to ground	Connect to ground
5	DVSS	Digital ground	Digital ground
6	DVDD	Digital supply	Digital supply
7	DVIO	Digital I/O supply	Digital I/O supply
8	CSB	Chip select	Not connected
9	NC	Not connected	Not connected
10	NC	Not connected	Not connected
11	SCK_SCL	SPI serial clock (SCK)	I^2C serial clock (SCL)
12	MISO_SDA	SPI data out (MISO)	I^2C data in / out (SDA)
13	MOSI	SPI data in (MOSI)	Not connected
14	AVDD	Analog supply	Analog supply
15	AVSS	Analog ground	Analog ground
16	AVSS	Analog ground	Analog ground
17	ATSTIO	Not connected	Not connected
18	NC	Not connected	Not connected

7.2 Recommended circuit diagram

1. Connect 100 nF SMD capacitor between each supply voltage and ground level.
2. Connect 1 µF capacitor between each supply voltage and ground level.
3. Use one regulator for analog and digital supply (AVDD and DVDD).
4. Use separate regulator for digital IO supply (DVIO).
5. Xreset is needed always in start up: when Xreset is low, raise power supplies inside specification, then set Xreset high.
6. INT-pin is used with output buffer as well as in Free Fall and Motion Detection mode.
7. Serial interface (SPI or I^2C) logical '1' level is determined by DVIO supply voltage level.

Recommended circuit diagram for the SCA3000 with SPI interface is presented in Figure 15 below.

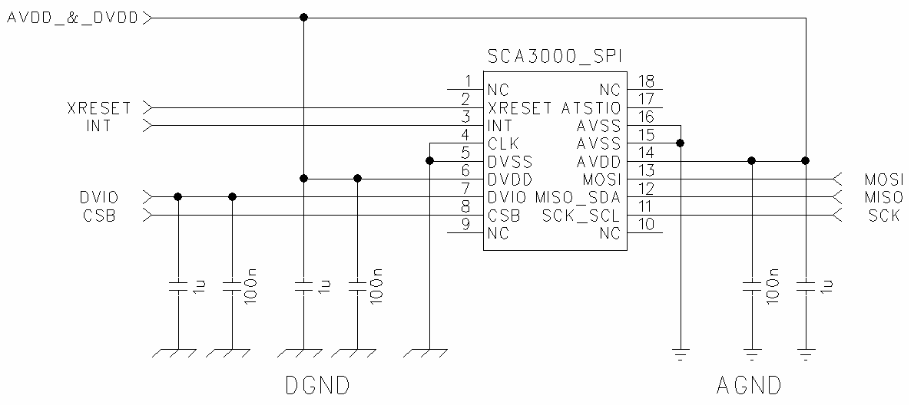

Figure 15. Recommended circuit diagram for the SCA3000 with SPI interface.

Recommended circuit diagram for the SCA3000 with I^2C interface is presented in Figure 16 below.

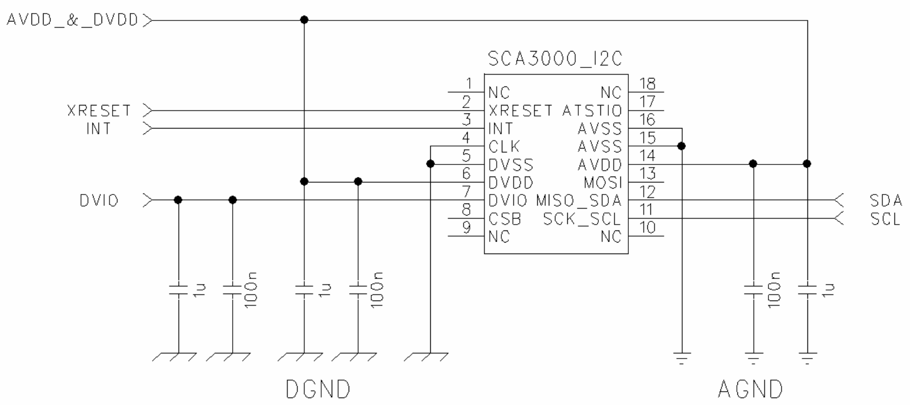

Figure 16. Recommended circuit diagram for the SCA3000 with I^2C interface.

7.3 Recommended PWB layout

General PWB layout recommendations for SCA3000 products (refer to Figure 15, Figure 16 and Figure 17):

1. Locate 100 nF SMD capacitors right next to the SCA3000 package.
2. 1 µF capacitors can be located near the node where AVDD and DVDD are routed on separate ways.
3. Use separate ground planes for AGND and DGND. Connect separate ground planes together on PWB.
4. Use double sided PWB, connect the bottom side plane to DGND.

Recommended PWB pad layout for SCA3000 is presented in Figure 17 below (dimensions in millimeters, [mm]).

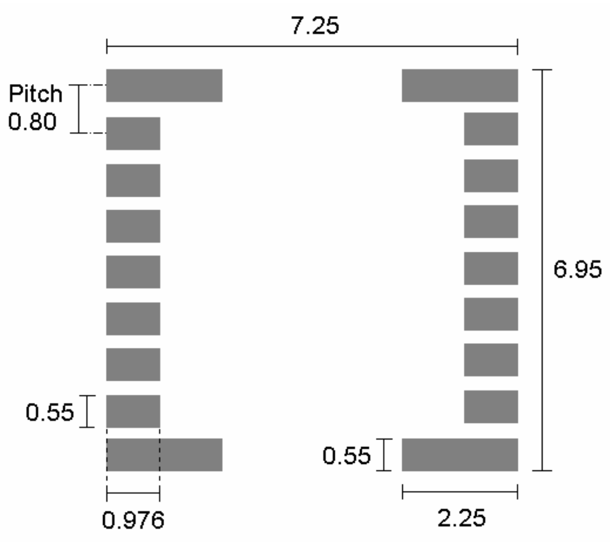

Figure 17. Recommended PWB pad layout for SCA3000.

Recommended PWB layout for the SCA3000 with SPI interface is presented in Figure 18 below (circuit diagram presented in Figure 15 above).

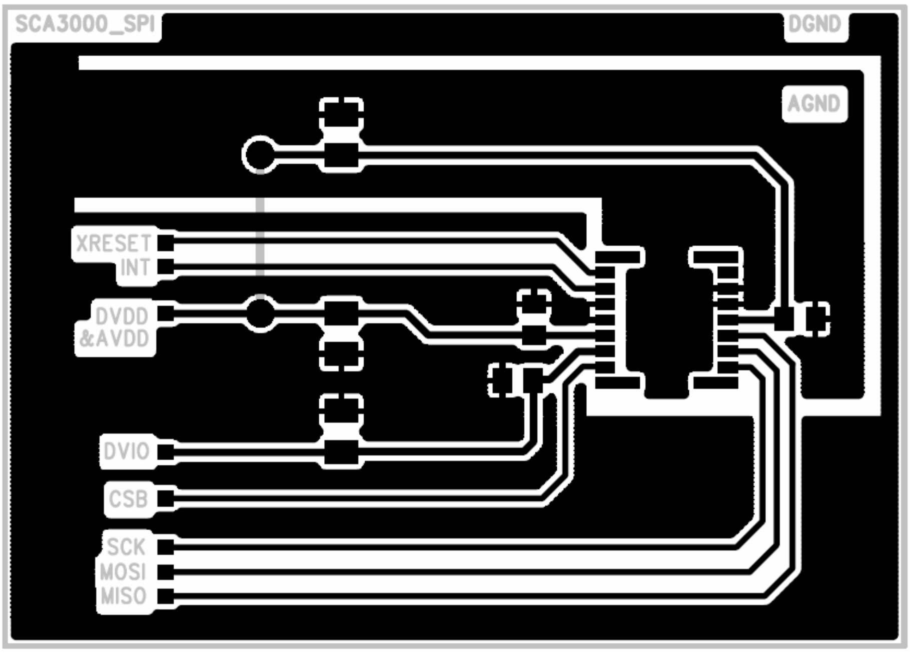

Figure 18. Recommended PWB layout for SCA3000 with SPI interface (not actual size, for reference only).

Recommended PWB layout for SCA3000 with I^{2}C interface is presented in Figure 19 below (circuit diagram presented in Figure 16 above).

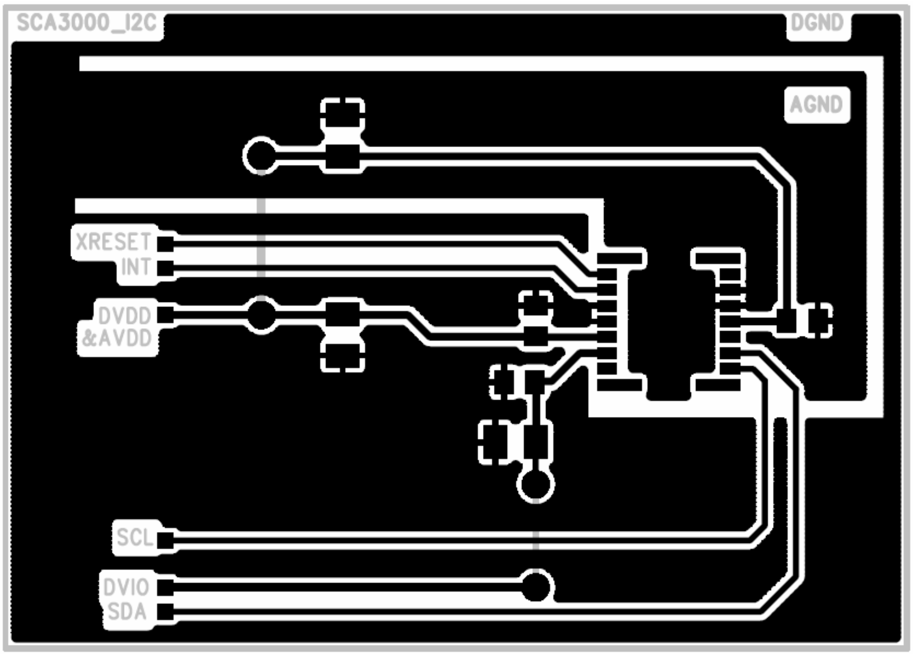

Figure 19. Recommended PWB layout for SCA3000 with I^{2}C interface (not actual size, for reference only).

7.4 Assembly instructions

The Moisture Sensitivity Level (MSL) of the SCA3000 component is 3 according to the IPC/JEDEC J-STD-020C. Please refer to the document "TN54 SCA3000 Assembly Instructions" for more detailed information of SCA3000 assembly.

7.5 Tape and reel specifications

Please refer to the document "TN54 SCA3000 Assembly Instructions" for tape and reel specifications.

8 Data sheet references

8.1 Offset

SCA3000's offset will be calibrated in X = 0 g, Y = 0 g, and Z = +1 g (Z measuring axis is parallel to earth's gravitation) position, see Figure 20.

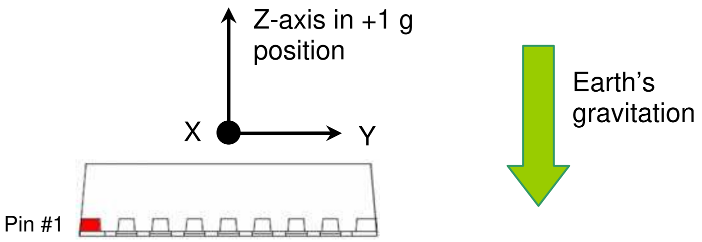

Figure 20. SCA3000 offset (0 g) position.

8.1.1 Offset calibration error

Offset calibration error is the difference between the sensor's actual output reading and the nominal output reading in calibration conditions. Error is calculated by

Equation 2

$$Offset_{X-axisCalibEr} = \frac{Output_{X-axis} - Output}{Sens} \cdot 1000 ,$$

where $Output_{X\text{-}axisCalibEr}$ is sensor's X-axis calibration error in [mg], $Output_{X\text{-}axis}$ is sensor's X-axis output reading [counts], $Output$ is sensor's nominal output in 0 g position and $Sens$ sensor's nominal sensitivity [counts/g].

8.1.2 Offset temperature error

Offset temperature error is the difference between the sensor's output reading in different temperatures and the sensor's calibrated offset value at room temperature. Error is calculated by

Equation 3

$$Offset_{X-axisTempEr\,@\,T} = \frac{Output_{X-axis\,@\,T} - Output_{X-axis\,@\,RT}}{Sens} \cdot 1000 ,$$

where $Output_{X\text{-}axisTempEr@T}$ is sensor's X-axis temperature error in [mg] in temperature T, $Output_{X\text{-}axis@T}$ is sensor's X-axis output reading [counts] in temperature T, $Output_{X\text{-}axis@T}$ X-axis output reading [counts] at room temperature RT and $Sens$ sensor's nominal sensitivity [counts/g]. Sensor is in 0 g position for every measurement point.

8.2 Sensitivity

During sensitivity calibration, the sensor is placed in ±1 g positions having one of the sensor's measuring axis at a time parallel to the earth's gravitation, see Figure 21.

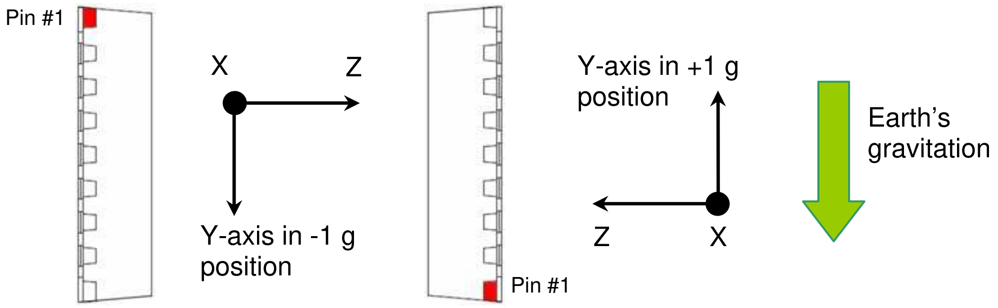

Figure 21. SCA3000 positions for Y-axis sensitivity measurement.

Sensitivity is calculated by

Equation 4

$$Sens_{Y-axis} = \frac{Output_{Y-axis@+1g} - Output_{Y-axis@-1g}}{2g},$$

where $Sens_{Y\text{-}axis}$ is sensor's Y-axis sensitivity in [counts/g], $Output_{Y\text{-}axis@+1g}$ sensor's Y-axis output reading [counts] in +1 g position and $Output_{Y\text{-}axis@\text{-}1g}$ is sensor's Y-axis output reading [counts] in -1 g position.

8.2.1 Sensitivity calibration error

Sensitivity calibration error is the difference between sensor's measured sensitivity and the nominal sensitivity at room temperature conditions. Error is calculated by

Equation 5

$$Sens_{Y-axisCalibEr} = \frac{Sens_{Y-axis} - Sens}{Sens} \cdot 100\%,$$

where $Sens_{Y\text{-}axisCalibEr}$ is sensor's Y-axis sensitivity calibration error in [%], $Sens_{Y\text{-}axis}$ sensor's Y-axis sensitivity [counts/g] at room temperature conditions and $Sens$ is sensor's nominal sensitivity [counts/g].

8.2.2 Sensitivity temperature error

Sensitivity temperature error is the difference between sensor's sensitivity at different temperatures and the calibrated sensitivity. Error is calculated by

Equation 6

$$Sens_{Y-axisTempEr@T} = \frac{Sens_{Y-axis@T} - Sens_{Y-axis@RT}}{Sens_{Y-axis@RT}} \cdot 100\%,$$

where $Sens_{Y\text{-}axisTempEr@T}$ is sensor's Y-axis sensitivity temperature error in [%] in temperature T, $Sens_{Y\text{-}axis@T}$ is sensor's measured Y-axis sensitivity [counts/g] at temperature T and $Sens_{Y\text{-}axis@RT}$ is sensor's measured Y-axis sensitivity [counts/g] at room temperature RT.

8.3 Linearity

The linearity error characterization method described below is applied for those SCA3000 series components that have measuring range ±3g or below.

Accurate input acceleration needed in linearity characterization is generated using centrifugal force in centrifuge, see Figure 22. The RPM of the centrifuge is sweeped so that wanted input acceleration values are applied in parallel to the sensor's measuring axis.

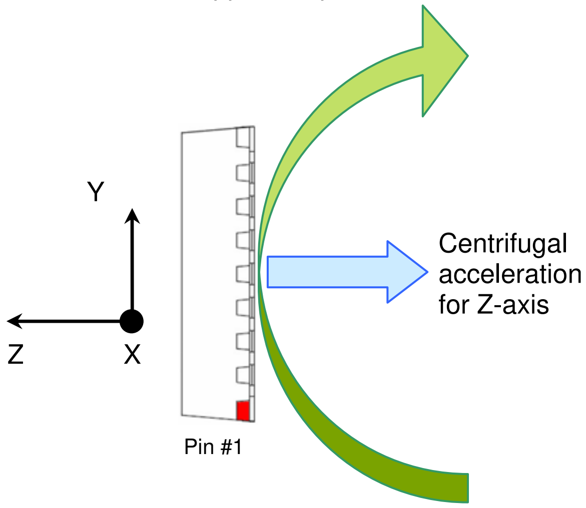

Figure 22. Centrifugal acceleration applied for SCA3000 Z-axis.

Linearity error is the deviation from the straight line through sensor's sensitivity calibration points, see Figure 23.

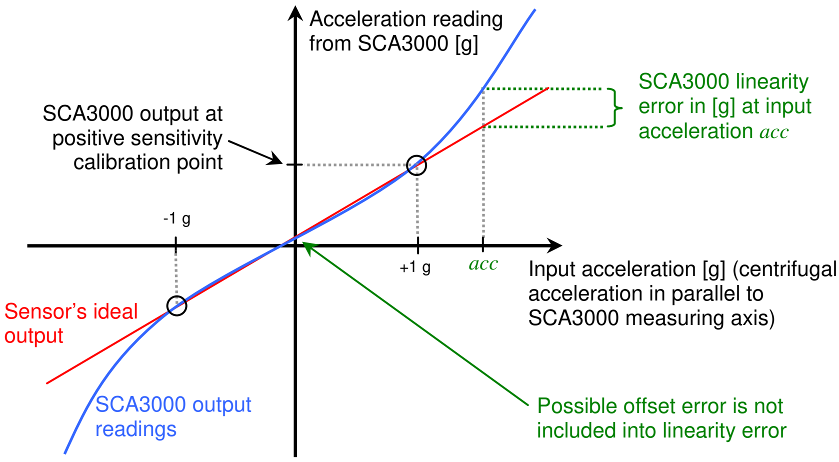

Figure 23. SCA3000's linearity error at input acceleration acc.

Linearity error is calculated by

Equation 7

$$LinEr_{Z-axis\,@\,acc} = \frac{Output_{Z-axis\,@\,acc} - Output_{@\,acc}}{Sens \cdot FS} \cdot 100\% \,,$$

where $LinEr_{Z\text{-}axis@acc}$ is sensor's Z-axis linearity error [%FS] on input acceleration acc, $Output_{Z\text{-}axis@acc}$ is sensor's measured Z-axis output [counts] on input acceleration acc, $Output_{@acc}$ is sensor's nominal output [counts] on input acceleration acc, $Sens$ is sensor's nominal sensitivity [counts/g] and FS is sensor's full scale measuring range [g] (for example for SCA3000-D01 ±2g → FS = 2 g).

Sensor's ideal output $Output_{@acc}$ (in Equation 7) is calculated from the straight line through sensitivity calibration points (the red straight line in Figure 23). Nominal output is calculated by

Equation 8

$$Output_{@\,acc} = acc \cdot \frac{Output_{+1g} - Output_{-1g}}{2g} + offset = acc \cdot \frac{Output_{+1g} - Output_{-1g}}{2g} + \frac{Output_{+1g} + Output_{-1g}}{2},$$

where $Output_{@acc}$ is sensor's nominal output [counts] with input acceleration acc in [g], $Output_{+1g}$ is sensor's measured output [counts] at +1 g input acceleration and $Output_{-1g}$ is sensor's measured output at -1 g input acceleration. Possible $offset$ term [counts] is included into nominal output, because it is not included in to linearity error.

8.4 Noise

Output noise n_X, n_Y and n_Z in X,Y and Z directions is the measured standard deviation of the output values when the sensor is in 0 g position at room temperature. Average noise/axis is calculated by

Equation 9

$$n = \sqrt{\frac{1}{3}\left(n_X^2 + n_Y^2 + n_Z^2\right)},$$

where n is sensor's noise [g] per axis, n_X is sensor's X-axis noise [g], n_Y is sensor's Y-axis noise [g] and n_Z is sensor's Z-axis noise [g].

SCA3000 demo-kit design can be used as a reference design for noise measurements, refer to "SCA3000 DEMO KIT User Manual 8259300".

8.5 Bandwidth

Signal bandwidth is measured in a shaker by sweeping the piston movement frequency with constant amplitude (Figure 24).

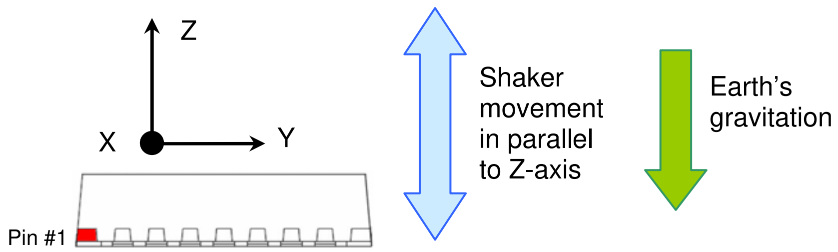

Figure 24. SCA3000 movement in Z-axis bandwidth measurement.

8.6 Cross-axis sensitivity

Cross-axis sensitivity is sum of the alignment and the inherent sensitivity errors. Cross-axis sensitivity of one axis is a geometric sum of the sensitivities in two perpendicular directions.

Cross-axis sensitivity [%] of X-axis is given by

Equation 10

$$Cross_X = \pm \frac{\sqrt{S_{XY}^2 + S_{XZ}^2}}{S_X} \cdot 100\%,$$

where S_{XY} is X-axis sensitivity to Y-axis acceleration [Count/g], S_{XZ} is X-axis sensitivity to Z-axis acceleration [Count/g] and S_X is sensitivity of X-axis [Count/g].

Cross-axis sensitivity [%] of Y-axis is given by

Equation 11

$$Cross_Y = \pm \frac{\sqrt{S_{YX}^2 + S_{YZ}^2}}{S_Y} \cdot 100\%,$$

where S_{YX} is Y-axis sensitivity to X-axis acceleration [Count/g], S_{YZ} is Y-axis sensitivity to Z-axis acceleration [Count/g] and S_Y is sensitivity of Y-axis [Count/g].

Cross-axis sensitivity [%] of Z-axis is given by

Equation 12

$$Cross_Z = \pm \frac{\sqrt{S_{ZX}^2 + S_{ZY}^2}}{S_Z} \cdot 100\%,$$

where S_{ZX} is Z-axis sensitivity to X-axis acceleration [Count/g], S_{ZY} is Z-axis sensitivity to Y-axis acceleration [Count/g] and S_Z is sensitivity of Z-axis [Count/g].

Cross-axis sensitivity of SCA3000 family is measured in centrifuge over specified measurement range during qualification. Correct mounting position of component is important during the measurement of cross-axis sensitivity.

8.7 Turn-on time

Turn-on time is the time when the last of one X, Y, Z axis output readings stabilizes into its final value after XRESET is pulled high. The final value limits in turn-on time measurements is defined to be ±1 % of the sensor's full scale measuring range (for example for SCA3000-D01 ±2g → FS = 2 g). Turn-on time definition for Z-axis is presented in Figure 25 below.

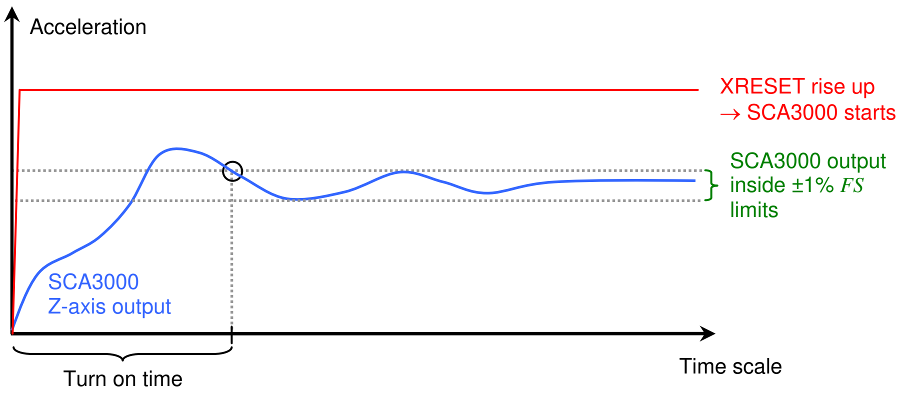

Figure 25. Turn-on time definition for one axis.

9 Order Information

Order code	Description	Packing	Quantity
SCA3000-D01-1	3-Axis accelerometer with SPI interface, +/-2g, 100 pcs	T&R	100
SCA3000-D01-10	3-Axis accelerometer with SPI interface, +/-2g, 1000 pcs	T&R	1000
SCA3000-D01-25	3-Axis accelerometer with SPI interface, +/-2g, 2500 pcs	T&R	2500
SCA3000-D02-1	3-Axis accelerometer with I2C interface, +/-2g, 100 pcs	T&R	100
SCA3000-D02-10	3-Axis accelerometer with I2C interface, +/-2g, 1000 pcs	T&R	1000
SCA3000-D02-25	3-Axis accelerometer with I2C interface, +/-2g, 2500 pcs	T&R	2500
SCA3000-E01-1	3-Axis accelerometer with SPI interface, +/-3g, 100 pcs	T&R	100
SCA3000-E01-10	3-Axis accelerometer with SPI interface, +/-3g, 1000 pcs	T&R	1000
SCA3000-E01-25	3-Axis accelerometer with SPI interface, +/-3g, 2500 pcs	T&R	2500
SCA3000-E02-1	3-Axis accelerometer with I2C interface, +/-3g, 100 pcs	T&R	100
SCA3000-E02-10	3-Axis accelerometer with I2C interface, +/-3g, 1000 pcs	T&R	1000
SCA3000-E02-25	3-Axis accelerometer with I2C interface, +/-3g, 2500 pcs	T&R	2500
SCA3000-E04-1	3-Axis accelerometer with SPI interface, +/-6g, 100 pcs	T&R	100
SCA3000-E04-10	3-Axis accelerometer with SPI interface, +/-6g, 1000 pcs	T&R	1000
SCA3000-E04-25	3-Axis accelerometer with SPI interface, +/-6g, 2500 pcs	T&R	2500
SCA3000-E05-1	3-Axis accelerometer with SPI interface, +/-18g, 100 pcs	T&R	100
SCA3000-E05-10	3-Axis accelerometer with SPI interface, +/-18g, 1000 pcs	T&R	1000
SCA3000-E05-25	3-Axis accelerometer with SPI interface, +/-18g, 2500 pcs	T&R	2500
SCA3000-D01 PWB	PWB assy, 3-Axis accelerometer with SPI interface, +/-2g	Bulk	1
SCA3000-D02 PWB	PWB assy, 3-Axis accelerometer with I2C interface, +/-2g	Bulk	1
SCA3000-E01 PWB	PWB assy, 3-Axis accelerometer with SPI interface, +/-3g	Bulk	1
SCA3000-E02 PWB	PWB assy, 3-Axis accelerometer with I2C interface, +/-3g	Bulk	1
SCA3000-E04 PWB	PWB assy, 3-Axis accelerometer with SPI interface, +/-6g	Bulk	1
SCA3000-E05 PWB	PWB assy, 3-Axis accelerometer with SPI interface, +/-18g	Bulk	1
SCA3000-D01DEMO	SCA3000-D01 DEMOKIT	Bulk	1

10 Document Change Control

Version	Date	Change Description
0.01	09.09.2005	Initial draft.
....		...
0.08	20.09.2005	Draft release for schematic and layout design.
0.09	23.09.2005	FF and MD description added.
0.10	12.10.2005	Introduction and functional descriptions edited, measurement mode, ring buffer, temperature measurement, interrupt, oscillator, reset and register descriptions added. Register and bit names changed to be more descriptive.
0.11	13.10.2005	Typo etc minor corrections.
0.12	14.10.2005	Draft release.
0.13	01.11.2005	Register initial values and examples added.
0.14	09.11.2005	Language corrections.
0.15	26.01.2006	New product versions updated. Output and ring buffer bit level definitions changed. This definition is valid from samples v0.3 onwards. Register level changes in temperature output.
0.16	15.02.2006	Updated: - absolute maximum ratings, - temperature output equation, - I^2C device address, specification references
0.17	14.03.2006	Updated: - recommended circuit diagrams, sections "Packing" and "Handling and storage" added
0.18	27.03.2006	Layout change
A	27.04.2006	Updated: - recommended circuit diagrams, - sections "Packing" and "Handling and storage" - section "Specification references" updated and renamed to "Data sheet references" MD threshold levels
A.01	27.06.2006	Updated: - document name changed to "SCA3000 Product Family Specification" - section "6.1 Package dimensions" updated sections "7.4 Solder paste and stencil parameters" and "7.5 Reflow" updated to "7.4 Assembly instructions" - section "9.1 Packing and handling" updated to "7.5 Tape and reel specifications" Contact information
A.02	30.6.2006	Order information added
A.03	11.9.2006	SCA3000-E04 information added
A.04	27.03.2007	Added: - SCA3000-E04 wide band measurement mode, - Typos corrected - New product types: SCA3000-E05 and SCA3000-L01
A.05	01.06.2007	Added: - New product type: SCA3000-D03 - I2C communication added for SCA3000-L01
A.06	30.10.2007	Corrections: typos, axis orientation
A.07	02.02.2009	Corrected recommended PWB layouts. Removed references to D03 and L01.

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