

## General Description

The 84021 is a general purpose, Crystal-to-LVCMOS/LVTTL High Frequency Synthesizer. The 84021 has a selectable TEST\_CLK or crystal input. The VCO operates at a frequency range of 620MHz to 780MHz. The VCO frequency is programmed in steps equal to the value of the input reference or crystal frequency. The VCO and output frequency can be programmed using the serial or parallel interface to the configuration logic.

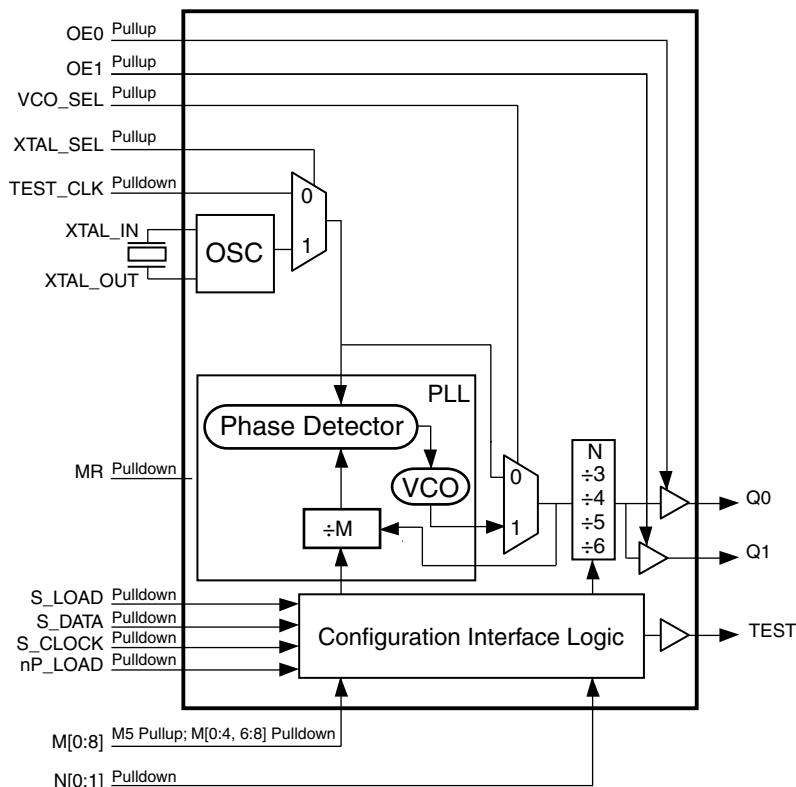
## Features

- Two LVCMOS/LVTTL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL TEST\_CLK
- Output frequency range: 103.3MHz to 260MHz
- Crystal input frequency range: 14MHz to 40MHz
- VCO range: 620MHz to 780MHz
- Parallel or serial interface for programming counter and output dividers
- RMS period jitter: 14.7ps (typical), ( $N \div 4$ ,  $V_{DDO} = 3.3V \pm 5\%$ )
- RMS phase jitter at 155.52MHz, using a 38.88MHz crystal (12kHz to 20MHz): 2.61ps (typical)

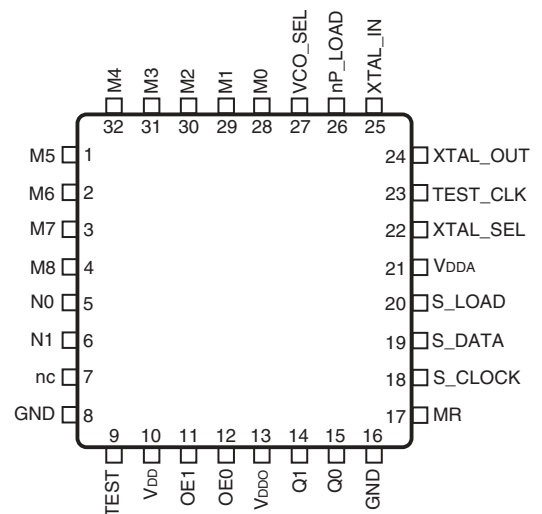
| Offset | Noise Power   |
|--------|---------------|
| 100Hz  | -87.9 dBc/Hz  |
| 1kHz   | -115.8 dBc/Hz |
| 10kHz  | -124.2 dBc/Hz |
| 100kHz | -127.7 dBc/Hz |

- Full 3.3V or mixed 3.3V core/2.5V or 1.8V output supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment



**84021**  
**32 Lead LQFP**  
**7mm x 7mm x 1.4mm package body**  
**Y Package**  
**Top View**

## Functional Description

*NOTE: The functional description that follows describes operation using a 25MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 5, NOTE 1.*

The 84021 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 25MHz crystal provides a 25MHz phase detector reference frequency. The VCO of the PLL operates over a range of 620MHz to 780MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVCMOS output buffers. The divider provides a 50% output duty cycle.

The programmable features of the 84021 support two input modes to program the M divider and N output divider. The two input operational modes are parallel and serial. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP\_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 and N1 is passed directly to the M divider and N output divider. On the LOW-to-HIGH transition of the nP\_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP\_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the

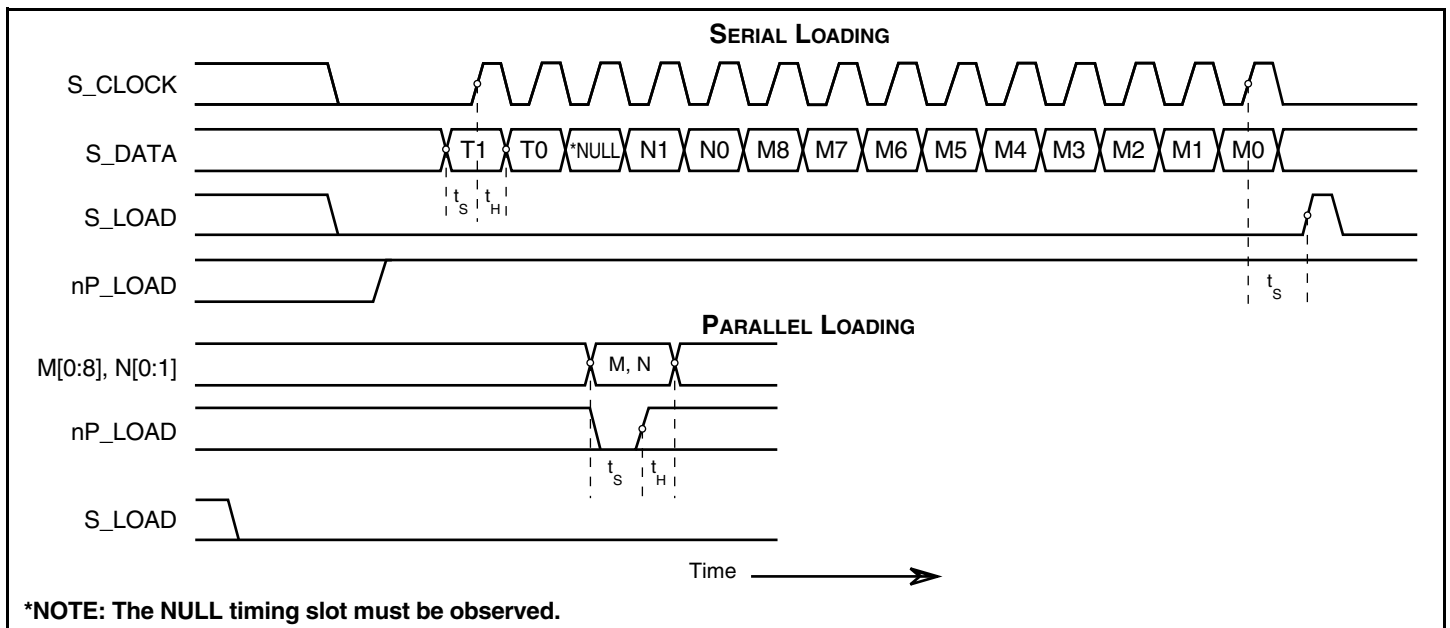
VCO frequency, the crystal frequency and the M divider is defined as follows:  $f_{VCO} = f_{xtal} \times M$

The M value and the required values of M0 through M8 are shown in Table 3B, Programmable VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 25MHz reference are defined as  $25 \leq M \leq 31$ . The frequency out is defined as follows:

$$F_{OUT} = \frac{f_{VCO}}{N} = \frac{f_{xtal} \times M}{N}$$

Serial operation occurs when nP\_LOAD is HIGH and S\_LOAD is LOW. The shift register is loaded by sampling the S\_DATA bits with the rising edge of S\_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S\_LOAD transitions from LOW-to-HIGH. The M divide and N output divide values are latched on the HIGH-to-LOW transition of S\_LOAD. If S\_LOAD is held HIGH, data at the S\_DATA input is passed directly to the M divider and N output divider on each rising edge of S\_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

| T1 | T0 | TEST Output                  |
|----|----|------------------------------|
| 0  | 0  | LOW                          |
| 0  | 1  | S_DATA, Shift Register Input |
| 1  | 0  | Output of M Divider          |
| 1  | 1  | CMOS FOUT                    |



**Figure 1. Parallel & Serial Load Operations**

**Table 1. Pin Descriptions**

| Number                            | Name                                 | Type   |          | Description  |
|-----------------------------------|--------------------------------------|--------|----------|--|
| 1                                 | M5                                   | Input  | Pullup   | M divider inputs. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels.  |
| 2, 3, 4,<br>28, 29,<br>30, 31, 32 | M6, M7, M8,<br>M0, M1,<br>M2, M3, M4 | Input  | Pulldown |  |
| 5, 6                              | N0, N1                               | Input  | Pulldown | Determines N output divider value as defined in Table 3C, Function Table. LVCMOS/LVTTL interface levels.   |
| 7                                 | nc                                   | Unused |          | No connect.  |
| 8, 16                             | GND                                  | Power  |          | Power supply pins.   |
| 9                                 | TEST                                 | Output |          | Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels.  |
| 10                                | V <sub>DD</sub>                      | Power  |          | Core supply pin.   |
| 11, 12                            | OE1, OE0                             | Input  | Pullup   | Output enable. When logic HIGH, the outputs are enabled (default). When logic LOW, the outputs are in an Hi-Z state. See Table 3E, OE Function Table. LVCMOS/LVTTL interface levels.   |
| 13                                | V <sub>DDO</sub>                     | Power  |          | Output supply pin.   |
| 14, 15                            | Q1, Q0                               | Output |          | Single-ended clock outputs. LVCMOS/LVTTL interface levels.   |
| 17                                | MR                                   | Input  | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When Logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, and T values. LVCMOS/LVTTL interface levels. |
| 18                                | S_CLOCK                              | Input  | Pulldown | Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.  |
| 19                                | S_DATA                               | Input  | Pulldown | Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels.  |
| 20                                | S_LOAD                               | Input  | Pulldown | Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels.  |
| 21                                | V <sub>DDA</sub>                     | Power  |          | Analog supply pin.   |
| 22                                | XTAL_SEL                             | Input  | Pullup   | Selects between crystal or test inputs as the PLL reference source. Selects XTAL inputs when HIGH. Selects TEST_CLK when LOW. LVCMOS/LVTTL interface levels.   |
| 23                                | TEST_CLK                             | Input  | Pulldown | Single-ended test clock input. LVCMOS/LVTTL interface levels.  |
| 24,<br>25                         | XTAL_OUT<br>XTAL_IN                  | Input  |          | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.  |
| 26                                | nP_LOAD                              | Input  | Pulldown | Parallel load input. Determines when data present at M[8:0] is loaded into M divider, and when data present at N[1:0] sets the N output divider value. LVCMOS/LVTTL interface levels.  |
| 27                                | VCO_SEL                              | Input  | Pullup   | Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels.  |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter                                  | Test Conditions              | Minimum | Typical | Maximum | Units |
|-----------------------|--|------------------------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                          |                              |         | 4       |         | pF    |
| C <sub>PD</sub>       | Power Dissipation Capacitance (per output) | V <sub>DDO</sub> = 3.465V    |         | 15      |         | pF    |
|                       |  | V <sub>DDO</sub> = 2.625V    |         | 15      |         | pF    |
|                       |  | V <sub>DDO</sub> = 1.89V     |         | 20      |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                      |                              |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                    |                              |         | 51      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance                           | V <sub>DDO</sub> = 3.3V ± 5% |         | 7       |         | Ω     |
|                       |  | V <sub>DDO</sub> = 2.5V ± 5% |         | 7       |         | Ω     |
|                       |  | V <sub>DDO</sub> = 1.8V ± 5% |         | 10      |         | Ω     |

## Function Tables

**Table 3A. Parallel and Serial Mode Function Table**

| Inputs |         |      |      |        |         |        | Conditions  |
|--------|---------|------|------|--------|---------|--------|---|
| MR     | nP_LOAD | M    | N    | S_LOAD | S_CLOCK | S_DATA |   |
| H      | X       | X    | X    | X      | X       | X      | Reset. Forces outputs LOW.  |
| L      | L       | Data | Data | X      | X       | X      | Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.             |
| L      | ↑       | Data | Data | L      | X       | X      | Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs. |
| L      | H       | X    | X    | L      | ↑       | Data   | Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK.                   |
| L      | H       | X    | X    | ↑      | L       | Data   | Contents of the shift register are passed to the M divider and N output divider.                                  |
| L      | H       | X    | X    | ↓      | L       | Data   | M divider and N output divider values are latched.  |
| L      | H       | X    | X    | L      | X       | X      | Parallel or serial input do not affect shift registers.   |
| L      | H       | X    | X    | H      | ↑       | Data   | S_DATA passed directly to M divider as it is clocked.   |

NOTE: L = LOW  
H = HIGH  
X = Don't care  
↑ = Rising edge transition  
↓ = Falling edge transition

**Table 3B. Programmable VCO Frequency Function Table**<sup>(NOTE 1)</sup>

| VCO Frequency (MHz) | M Divide | 256 | 128 | 64 | 32 | 16 | 8  | 4  | 2  | 1  |
|---------------------|----------|-----|-----|----|----|----|----|----|----|----|
|                     |          | M8  | M7  | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 625                 | 25       | 0   | 0   | 0  | 0  | 1  | 1  | 0  | 0  | 1  |
| •                   | •        | •   | •   | •  | •  | •  | •  | •  | •  | •  |
| 700                 | 28       | 0   | 0   | 0  | 0  | 1  | 1  | 1  | 0  | 0  |
| •                   | •        | •   | •   | •  | •  | •  | •  | •  | •  | •  |
| 775                 | 31       | 0   | 0   | 0  | 0  | 1  | 1  | 1  | 1  | 1  |

NOTE 1: These M divide values and the resulting frequencies correspond to TEST\_CLK or crystal frequency of 25MHz.

**Table 3C. Programmable Output Divider Function Table (PLL Enabled)**

| Inputs |    | N Divider Value | Output Frequency (MHz) |         |
|--------|----|-----------------|------------------------|---------|
| N1     | N0 |                 | Minimum                | Maximum |
| 0      | 0  | 3               | 206.7                  | 260     |
| 0      | 1  | 4               | 155                    | 195     |
| 1      | 0  | 5               | 124                    | 156     |
| 1      | 1  | 6               | 103.3                  | 130     |

**Table 3D. Commonly Used Configuration Function Table**

| Inputs        |                 |                 | Output Frequency (MHz) |
|---------------|-----------------|-----------------|------------------------|
| Crystal (MHz) | M Divider Value | N Divider Value | Minimum                |
| 19.44         | 32              | 4               | 155.52                 |
| 19.53125      | 32              | 4               | 156.25                 |
| 25            | 25              | 4               | 156.25                 |
| 25            | 25              | 5               | 125                    |
| 25.50         | 25              | 3               | 212.50                 |
| 25.50         | 25              | 4               | 159.375                |
| 25.50         | 25              | 6               | 106.25                 |
| 38.88         | 16              | 4               | 155.52                 |

**Table 3E. Output Enable & Clock Enable Function Table**

| Control Inputs |     | Output  |         |
|----------------|-----|---------|---------|
| OE0            | OE1 | Q0      | Q1      |
| 0              | 0   | Hi-Z    | Hi-Z    |
| 0              | 1   | Hi-Z    | Enabled |
| 1              | 0   | Enabled | Hi-Z    |
| 1              | 1   | Enabled | Enabled |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item                                     | Rating                                     |
|--|--|
| Supply Voltage, $V_{DD}$                 | 4.6V                                       |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs | 0V to $V_{DD}$<br>-0.5V to $V_{DD} + 0.5V$ |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$                  |
| Package Thermal Impedance, $\theta_{JA}$ | 47.9°C/W (0 lfm)                           |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C                             |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  or  $1.8V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$**

| Symbol    | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|-----------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$  | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$ | Analog Supply Voltage |                 | $V_{DD} - 0.36$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO}$ | Output Supply Voltage |                 | 3.135           | 3.3     | 3.465    | V     |
|           |                       |                 | 2.375           | 2.5     | 2.625    | V     |
|           |                       |                 | 1.71            | 1.8     | 1.89     | V     |
| $I_{DD}$  | Power Supply Current  |                 |                 |         | 110      | mA    |
| $I_{DDA}$ | Analog Supply Current |                 |                 |         | 24       | mA    |
| $I_{DDO}$ | Output Supply Current |                 |                 |         | 5        | mA    |

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  or  $1.8V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

| Symbol   | Parameter                   |  | Test Conditions                            | Minimum         | Typical | Maximum        | Units   |
|----------|-----------------------------|--|--|-----------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage          |  |  | 2               |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage           | OE[0:1], N[0:1], M[0:8], XTAL_SEL, VCO_SEL, S_DATA, S_CLOCK, S_LOAD, nP_LOAD, MR |  | -0.3            |         | 0.8            | V       |
|          |                             | TEST_CLOCK   |  | -0.3            |         | 1.3            | V       |
| $I_{IH}$ | Input High Current          | MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD, M[0:4], M[6:8], N0, N1           | $V_{DD} = V_{IN} = 3.465V$                 |                 |         | 150            | $\mu A$ |
|          |                             | M5, OE0, OE1, XTAL_SEL, VCO_SEL  | $V_{DD} = V_{IN} = 3.465V$                 |                 |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current           | MR, S_CLOCK, TEST_CLK, S_DATA, S_LOAD, nP_LOAD, M[0:4], M[6:8], N0, N1           | $V_{DD} = 3.465V, V_{IN} = 0V$             | -5              |         |                | $\mu A$ |
|          |                             | M5, OE0, OE1, XTAL_SEL, VCO_SEL  | $V_{DD} = 3.465V, V_{IN} = 0V$             | -150            |         |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 |  | $V_{DDO} = 3.3V \pm 5\%$                   | 2.6             |         |                | V       |
|          |                             |  | $V_{DDO} = 2.5V \pm 5\%$                   | 1.8             |         |                | V       |
|          |                             |  | $V_{DDO} = 1.8V \pm 5\%$                   | $V_{DDO} - 0.3$ |         |                | V       |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |  | $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$ |                 |         | 0.5            | V       |
|          |                             |  | $V_{DDO} = 1.8V \pm 5\%$                   |                 |         | 0.4            | V       |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section, *Output Load Test Circuit diagrams*.

**Table 5. Input Frequency Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  or  $1.8V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

| Symbol   | Parameter       |                  | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------|------------------|-----------------|---------|---------|---------|-------|
| $f_{IN}$ | Input Frequency | TEST_CLK; NOTE 1 |                 | 14      |         | 40      | MHz   |
|          |                 | XTAL; NOTE 1     |                 | 14      |         | 40      | MHz   |
|          |                 | S_CLOCK          |                 |         |         | 50      | MHz   |

NOTE 1: For the input crystal and TEST\_CLK frequency range, the M value must be set for the VCO to operate within the 620MHz to 780MHz range. Using the minimum input frequency of 14MHz, valid values of M are  $45 \leq M \leq 55$ . Using the maximum input frequency of 40MHz, valid values of M are  $16 \leq M \leq 19$ .

**Table 6. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 14          |         | 40      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance ( $C_O$ )        |                 |             |         | 7       | pF       |

## AC Electrical Characteristics

**Table 7A. AC Characteristics,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$**

| Symbol   | Parameter                     | Test Conditions  | Minimum | Typical | Maximum | Units |
|--|-------------------------------|--|---------|---------|---------|-------|
| $f_{OUT}$  | Output Frequency              |  | 103.3   |         | 260     | MHz   |
| $f_{jit(per)}$   | Period Jitter, RMS; NOTE 1, 2 | N = 3  |         | 13.5    | 26.4    | ps    |
|  |                               | N = 4  |         | 14.7    | 34.2    | ps    |
|  |                               | N = 5  |         | 16.7    | 42.4    | ps    |
|  |                               | N = 6  |         | 24.7    | 40.8    | ps    |
|  |                               | M=40, N=4, 16.667MHz XTAL,<br>$f_{OUT}=166.67\text{MHz}$ |         | 4.5     | 6.9     | ps    |
| M=40, N=5, 16.667MHz XTAL,<br>$f_{OUT}=133.33\text{MHz}$ |                               | 4.6  | 7.8     | ps      |         |       |
| $t_{sk(o)}$  | Output Skew; NOTE 2, 3        |  |         |         | 100     | ps    |
| $t_R / t_F$  | Output Rise/Fall Time         | 20% to 80%   | 100     |         | 800     | ps    |
| $t_S$  | Setup Time                    | M, N to nP_LOAD  | 5       |         |         | ns    |
|  |                               | S_DATA to S_CLOCK  | 5       |         |         | ns    |
|  |                               | S_CLOCK to S_LOAD  | 5       |         |         | ns    |
| $t_H$  | Hold Time                     | M, N to nP_LOAD  | 5       |         |         | ns    |
|  |                               | S_DATA to S_CLOCK  | 5       |         |         | ns    |
|  |                               | S_CLOCK to S_LOAD  | 5       |         |         | ns    |
| odc  | Output Duty Cycle             | N $\neq$ 3   | 44      |         | 56      | %     |
|  |                               | M=40, N=4, 16.667MHz XTAL,<br>$f_{OUT}=166.67\text{MHz}$ | 45      |         | 55      | %     |
|  |                               | M=40, N=5, 16.667MHz XTAL,<br>$f_{OUT}=133.33\text{MHz}$ | 47      |         | 53      | %     |
| $t_{LOCK}$   | PLL Lock Time                 |  |         |         | 1       | ms    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .



**Table 7B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

| Symbol         | Parameter                     | Test Conditions                                   | Minimum | Typical | Maximum | Units |   |
|----------------|-------------------------------|---|---------|---------|---------|-------|---|
| $f_{OUT}$      | Output Frequency              |   | 103.3   |         | 260     | MHz   |   |
| $f_{jit(per)}$ | Period Jitter, RMS; NOTE 1, 2 | N = 3   |         | 11.4    | 18.8    | ps    |   |
|                |                               | N = 4   |         | 13.3    | 28.3    | ps    |   |
|                |                               | N = 5   |         | 16.0    | 39.8    | ps    |   |
|                |                               | N = 6   |         | 19.2    | 32.4    | ps    |   |
|                |                               | M=40, N=4, 16.667MHz XTAL,<br>$f_{OUT}=166.67MHz$ |         | 4.3     | 6.2     | ps    |   |
|                |                               | M=40, N=5, 16.667MHz XTAL,<br>$f_{OUT}=133.33MHz$ |         | 4.5     | 7.7     | ps    |   |
| $t_{sk(o)}$    | Output Skew; NOTE 2, 3        |   |         |         | 90      | ps    |   |
| $t_R / t_F$    | Output Rise/Fall Time         | 20% to 80%  | 100     |         | 800     | ps    |   |
| $t_S$          | Setup Time                    | M, N to nP_LOAD                                   |         | 5       |         | ns    |   |
|                |                               | S_DATA to S_CLOCK                                 |         | 5       |         | ns    |   |
|                |                               | S_CLOCK to S_LOAD                                 |         | 5       |         | ns    |   |
| $t_H$          | Hold Time                     | M, N to nP_LOAD                                   |         | 5       |         | ns    |   |
|                |                               | S_DATA to S_CLOCK                                 |         | 5       |         | ns    |   |
|                |                               | S_CLOCK to S_LOAD                                 |         | 5       |         | ns    |   |
| odc            | Output Duty Cycle             | N $\neq$ 3  |         | 44      |         | 56    | % |
|                |                               | M=40, N=4, 16.667MHz XTAL,<br>$f_{OUT}=166.67MHz$ |         | 45      |         | 55    | % |
|                |                               | M=40, N=5, 16.667MHz XTAL,<br>$f_{OUT}=133.33MHz$ |         | 47      |         | 53    | % |
| $t_{LOCK}$     | PLL Lock Time                 |   |         |         | 1       | ms    |   |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Jitter performance using XTAL inputs.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

**Table 7C. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

| Symbol         | Parameter                     | Test Conditions                                   | Minimum | Typical | Maximum | Units |   |
|----------------|-------------------------------|---|---------|---------|---------|-------|---|
| $f_{OUT}$      | Output Frequency              |   | 103.3   |         | 260     | MHz   |   |
| $f_{jit(per)}$ | Period Jitter, RMS; NOTE 1, 2 | N = 3   |         | 9.4     | 13.2    | ps    |   |
|                |                               | N = 4   |         | 10.8    | 19.6    | ps    |   |
|                |                               | N = 5   |         | 12.7    | 32.5    | ps    |   |
|                |                               | N = 6   |         | 13.4    | 25.4    | ps    |   |
|                |                               | M=40, N=4, 16.667MHz XTAL,<br>$f_{OUT}=166.67MHz$ |         | 5.4     | 8.3     | ps    |   |
|                |                               | M=40, N=5, 16.667MHz XTAL,<br>$f_{OUT}=133.33MHz$ |         | 5.1     | 8.8     | ps    |   |
| $t_{sk(o)}$    | Output Skew; NOTE 2, 3        |   |         |         | 90      | ps    |   |
| $t_R / t_F$    | Output Rise/Fall Time         | 20% to 80%  | 100     |         | 800     | ps    |   |
| $t_S$          | Setup Time                    | M, N to nP_LOAD                                   |         | 5       |         | ns    |   |
|                |                               | S_DATA to S_CLOCK                                 |         | 5       |         | ns    |   |
|                |                               | S_CLOCK to S_LOAD                                 |         | 5       |         | ns    |   |
| $t_H$          | Hold Time                     | M, N to nP_LOAD                                   |         | 5       |         | ns    |   |
|                |                               | S_DATA to S_CLOCK                                 |         | 5       |         | ns    |   |
|                |                               | S_CLOCK to S_LOAD                                 |         | 5       |         | ns    |   |
| odc            | Output Duty Cycle             | N $\neq$ 3  |         | 40      |         | 60    | % |
|                |                               | M=40, N=4, 16.667MHz XTAL,<br>$f_{OUT}=166.67MHz$ |         | 44      |         | 56    | % |
|                |                               | M=40, N=5, 16.667MHz XTAL,<br>$f_{OUT}=133.33MHz$ |         | 48      |         | 52    | % |
| $t_{LOCK}$     | PLL Lock Time                 |   |         |         | 1       | ms    |   |

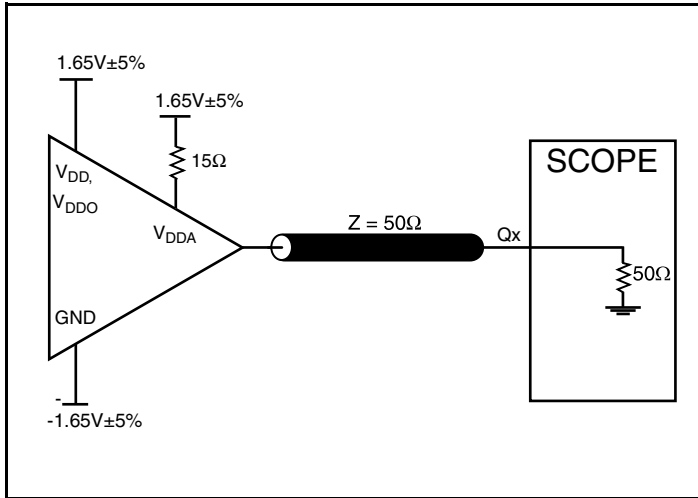
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Jitter performance using XTAL inputs.

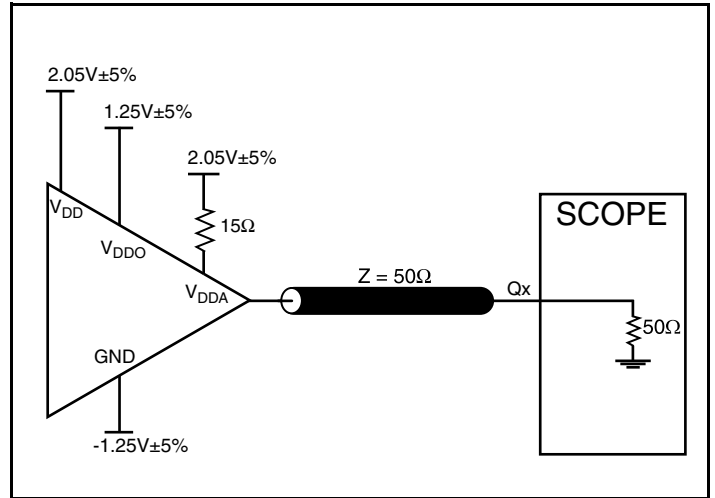
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

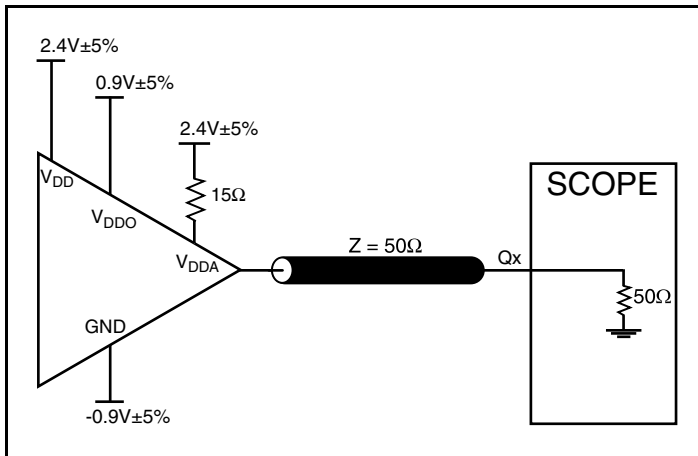
## Parameter Measurement Information



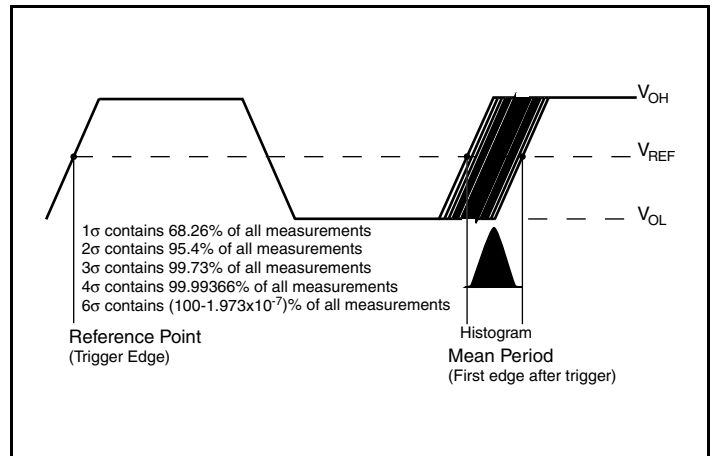
3.3V Core/3.3V Output Load AC Test Circuit



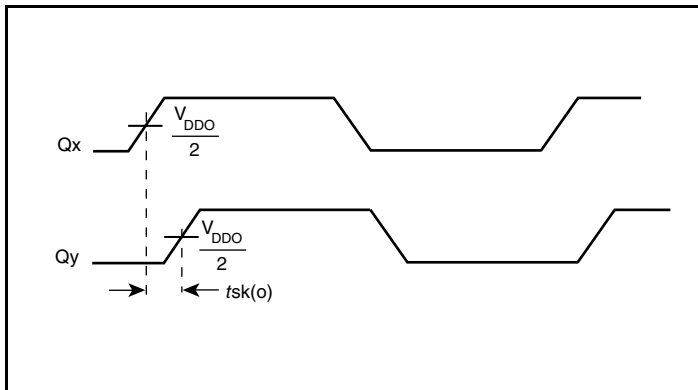
3.3V Core/2.5V Output Load AC Test Circuit



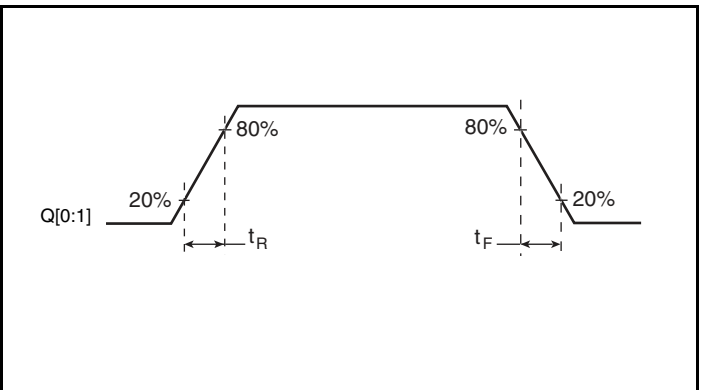
3.3V Core/1.8V Output Load AC Test Circuit



Period Jitter

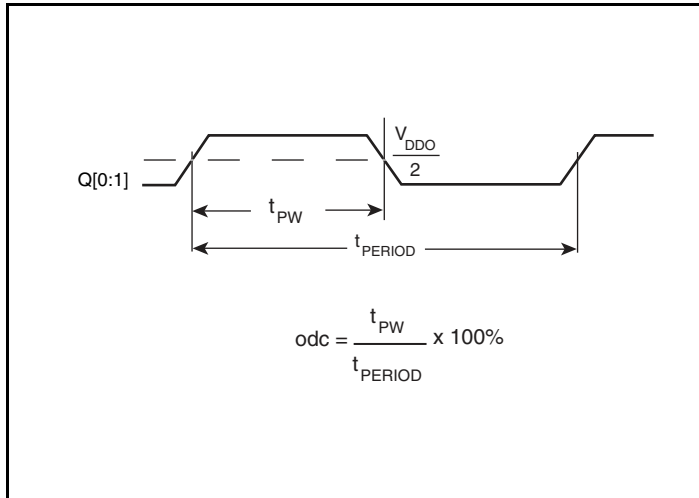


Output Skew



Output Rise/Fall Time

## Parameter Measurement Information, continued



**Output Duty Cycle/Pulse Width/Period**

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL\_IN to ground.

##### TEST\_CLK Input

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST\_CLK to ground.

##### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Outputs:

##### TEST Output

The unused TEST output can be left floating. There should be no trace attached.

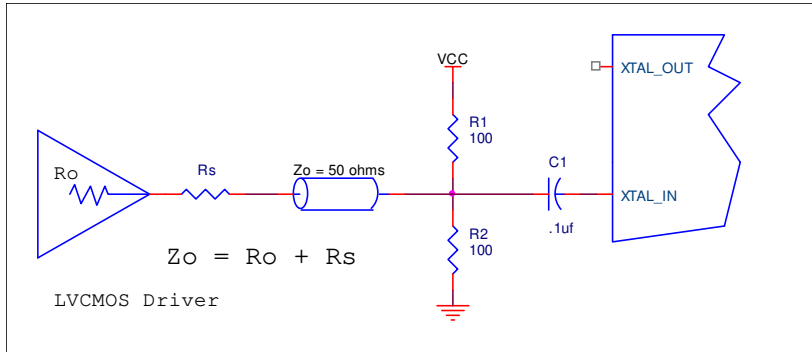
##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. We recommend that there is no trace attached.

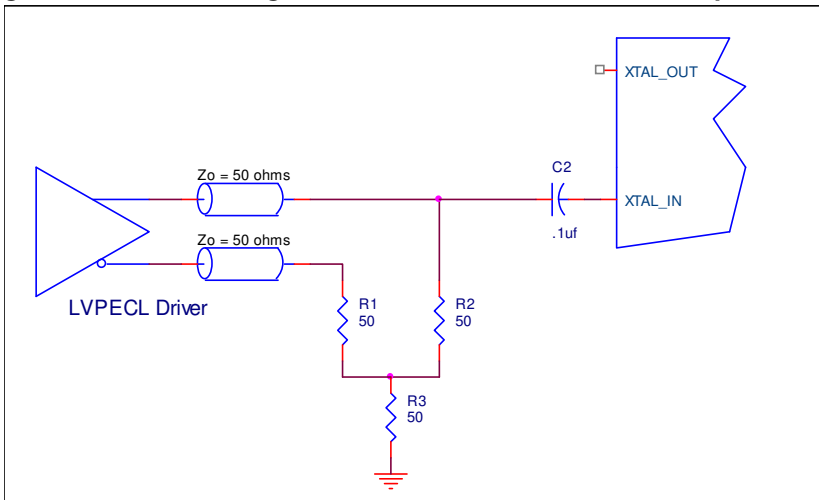
## Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2$   $50\Omega$ . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Layout Guideline

Figure 3 shows a schematic example of the 84021. In this example, a series termination is shown. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18pF parallel resonant crystal is used. The C1 = 22pF and C2 = 22pF are approximate values for frequency accuracy. The C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 84021 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the

device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

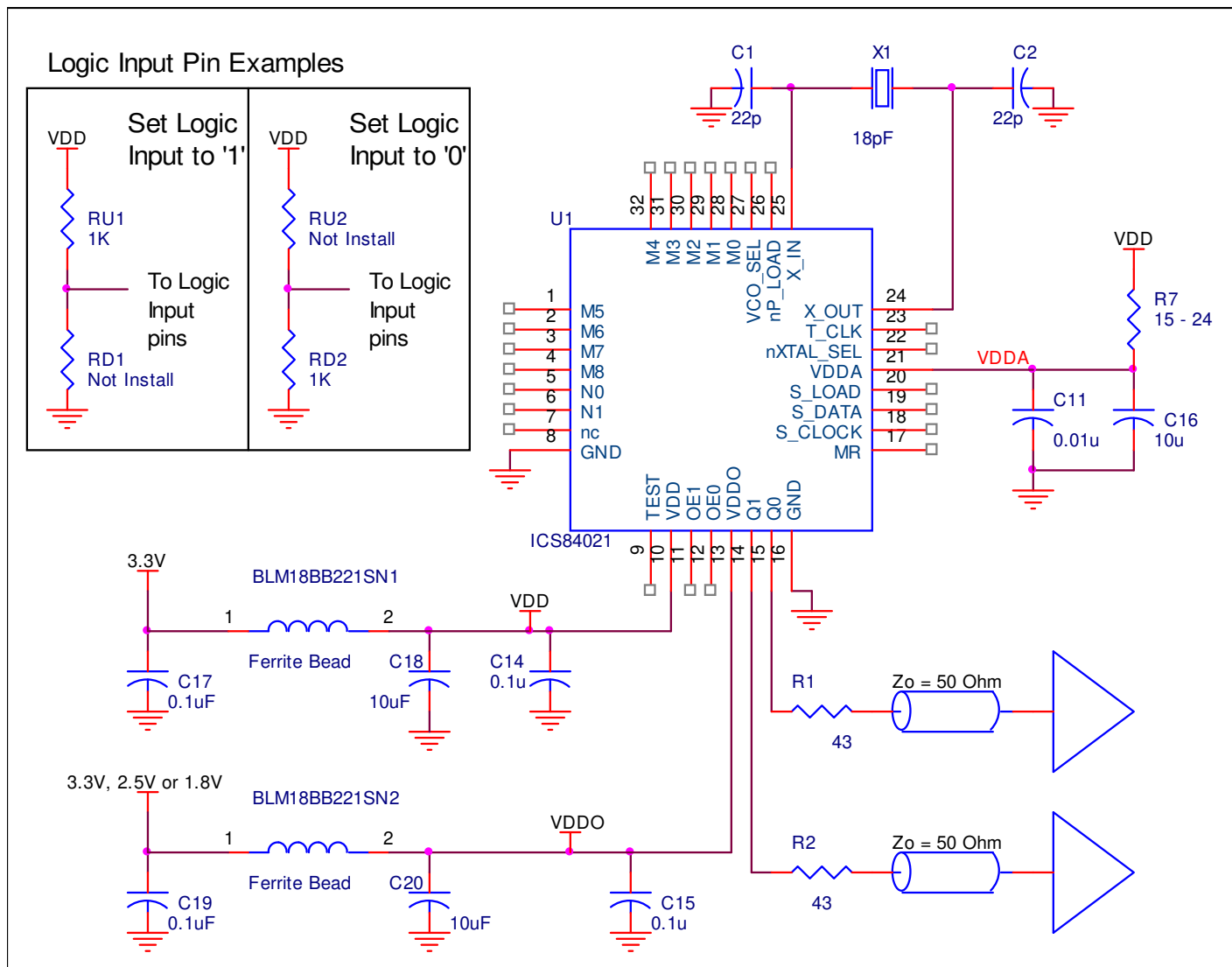


Figure 3. 84021 Application Schematic Example

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead LQFP**

| $\theta_{JA}$ by Velocity                    |          |          |          |
|--|----------|----------|----------|
| Linear Feet per Minut                        | 0        | 1        | 2.5      |
| Single-Layer PCB, JEDEC Standard Test Boards | 67.8°C/W | 55.9°C/W | 50.1°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 47.9°C/W | 42.1°C/W | 39.4°C/W |

## Transistor Count

The transistor count for 84021 is: 4325

# Package Outline and Package Dimensions

## Package Outline - Y Suffix for 32 Lead LQFP

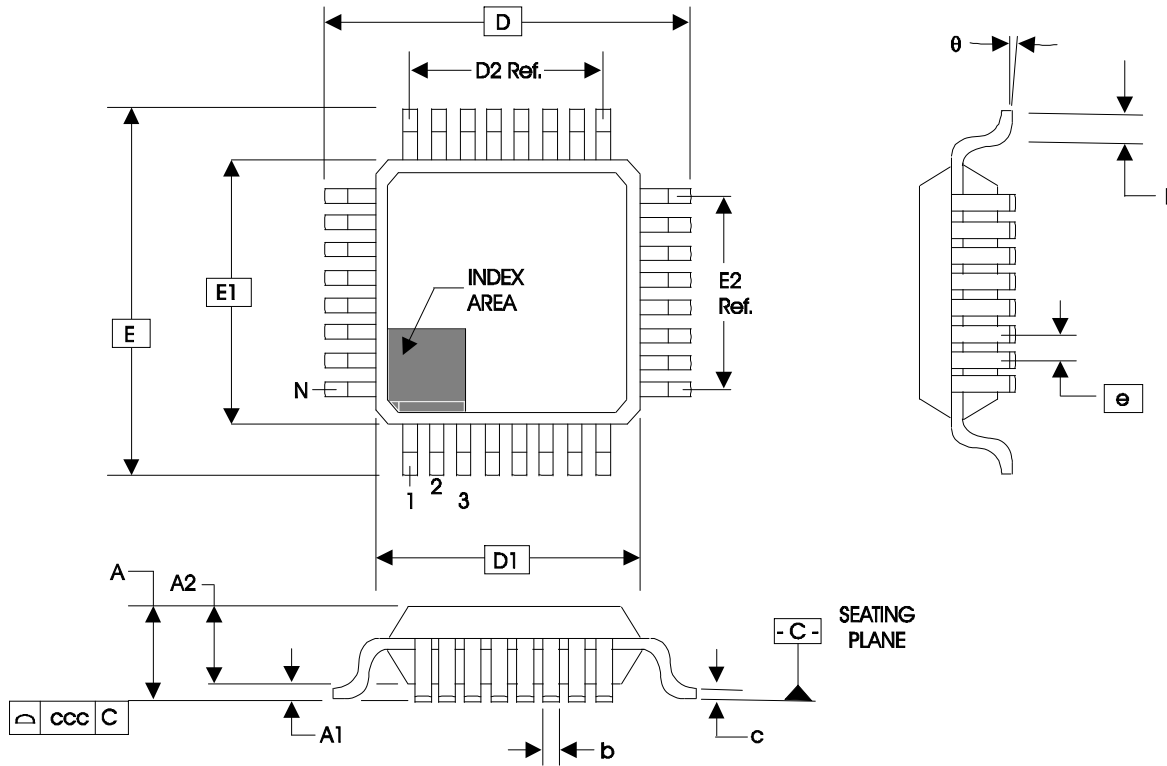


Table 9. Package Dimensions for 32 Lead LQFP

| JEDEC Variation: BBC - HD     |            |         |         |
|-------------------------------|------------|---------|---------|
| All Dimensions in Millimeters |            |         |         |
| Symbol                        | Minimum    | Nominal | Maximum |
| <b>N</b>                      | 32         |         |         |
| <b>A</b>                      |            |         | 1.60    |
| <b>A1</b>                     | 0.05       | 0.10    | 0.15    |
| <b>A2</b>                     | 1.35       | 1.40    | 1.45    |
| <b>b</b>                      | 0.30       | 0.37    | 0.45    |
| <b>c</b>                      | 0.09       |         | 0.20    |
| <b>D &amp; E</b>              | 9.00 Basic |         |         |
| <b>D1 &amp; E1</b>            | 7.00 Basic |         |         |
| <b>D2 &amp; E2</b>            | 5.60 Ref.  |         |         |
| <b>e</b>                      | 0.80 Basic |         |         |
| <b>L</b>                      | 0.45       | 0.60    | 0.75    |
| <b>θ</b>                      | 0°         |         | 7°      |
| <b>ccc</b>                    |            |         | 0.10    |

Reference Document: JEDEC Publication 95, MS-026



## Ordering Information

Table 10. Ordering Information

| Part/Order Number | Marking      | Package                  | Shipping Packaging | Temperature |
|-------------------|--------------|--------------------------|--------------------|-------------|
| 84021BYLF         | ICS84021BYLF | "Lead-Free" 32 Lead LQFP | Tray               | 0°C to 70°C |
| 84021BYLFT        | ICS84021BYLF | "Lead-Free" 32 Lead LQFP | 1000 Tape & Reel   | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

| Rev | Table                             | Page   | Description of Change   | Date    |
|-----|-----------------------------------|--|---|---------|
| B   | T2                                | 4<br>12  | Pin Characteristics Table - added R <sub>OUT</sub> rows.<br>Added Schematic Layout.<br>Changed XTAL naming convention to XTAL_IN/XTAL_OUT throughout the data sheet.  | 1/5/04  |
| C   | T6<br>T10                         | 1<br>2<br>7<br>15  | Features Section - added Lead-Free bullet.<br>Updated Parallel & Serial Load Operations Diagram.<br>Crystal Characteristics Table - added Drive Level.<br>Ordering Information Table - added Lead-Free package.   | 6/9/05  |
| D   | T4A<br>T6<br>T7A - T7C<br><br>T10 | 1<br>6<br>6<br>7<br>8 - 10<br>11<br>12<br>13<br>13<br>14<br>17 | Features section - updated RMS period jitter spec in bullet; added RMS phase jitter bullet.<br>Block Diagram - added pullups/pulldowns to input pins and added "N" in output divider box.<br>Absolute Maximum Ratings - updated Inputs, V <sub>I</sub> .<br>Power Supply DC Characteristics - updated V <sub>DDA</sub> , I <sub>DD</sub> , I <sub>DDA</sub> and I <sub>DDO</sub> specs.<br>Crystal Characteristics - deleted Drive Level row.<br>Updated Period Jitter, Output Rise/Fall Time and Output Duty Cycle specs. Added thermal note.<br>Parameter Measurement Information - corrected Output Load AC Test Circuit diagrams to coincide with 15Ω V <sub>DDA</sub> .<br>Added Recommendations for Unused Input & Output Pins.<br>Deleted Power Supply Filtering Techniques section, added to schematic layout.<br>Added Overdriving the XTAL Interface section.<br>Updated Layout Guideline and diagram.<br>Ordering Information Table - updated Part/Order Numbers and Marking to revision "B".<br>Converted datasheet format. | 1/5/11  |
| E   | T7A                               | 8<br>13  | AC Characteristics Table - corrected Period Jitter N = 4 spec, from 32.2ps max. to 34.2ps max.<br>Deleted Crystal Input Interface section, added to the schematic.  | 8/18/11 |
| E   | T10                               | 17   | Ordering Information - removed leaded device.   | 9/23/15 |



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