FEATURES

- **Nonlinearity ..... ±1/2 LSB Max**
- **Settling Time ..... 1.5µs Typ**
- **No Laser Trimming Used in Fabrication**
- **Internal Range and Offset Scaling Resistors**
- **Guaranteed Monotonicity Over Temperature**
- **TTL or CMOS Logic Input Compatibility, Pin Selectable**
- **Low Power Consumption ..... 130mW Typ**
- **Directly Pin Compatible with AD562**
- **Available in Die Form**

ORDERING INFORMATION †

NONLINEARITY @25°C (LSB)	PACKAGE	TEMPERATURE RANGE
±1/2	PM562HV	0°C to +70°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

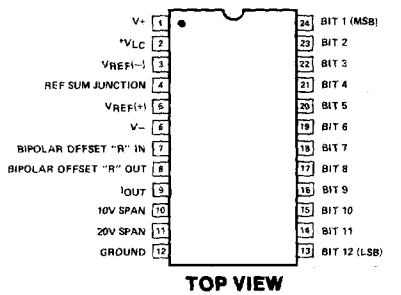
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

The PM-562 is a 12-bit monolithic multiplying digital-to-analog converter consisting of a reference current amplifier, an R-2R ladder network, range and offset scaling resistors, and 12 high-speed current switches. Improvements provided by the PM-562 include greater negative power supply range and increased output resistance. The PM-562 is pin compatible with the AD562.

A highly stable trim method; selective shorting of zener diodes, provides 13-bit accuracy without the need for laser trimming. Reliability of this trimming method has been proven in several other PMI products with many years of reliability history. Internal scaling resistors plus an external op amp simplifies construction in voltage output applications, while maintaining accuracy over wide operating temperature ranges. The PM-562 is recommended for 12-bit accuracy D/A applications where single-chip reliability, small size and low cost are primary considerations.

PIN CONNECTIONS

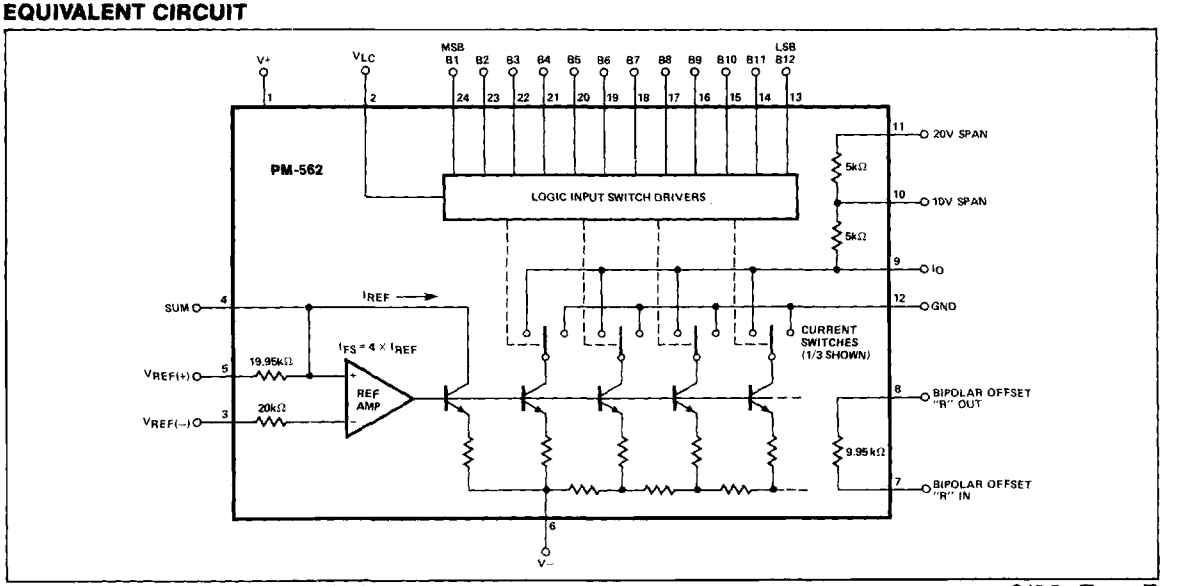


TOP VIEW

24-PIN HERMETIC DIP

*Connect V_{LC} to V+ for CMOS logic inputs. Leave V_{LC} open circuit or grounded for TTL inputs.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Supply Voltage (V+) ..... +18V
Supply Voltage (V–) ..... –18V
V+ to V– 36V
Logic Inputs ..... V– to (V– plus 36V)
Summing Junction (Pin 4) ..... V– to V+
CMOS/TTL Threshold (Pin 2) ..... V– to V+
I_{OUT} (Pin 9) ..... –5V to +18V
Span Resistors 36V

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
24-Pin Hermetic DIP (V)	57	10	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at V+ = 5V, V– = –15V, V_{REF} (+) = +10.0000V, V_{REF} (–) = 0V, T_A = +25°C, unless otherwise noted.

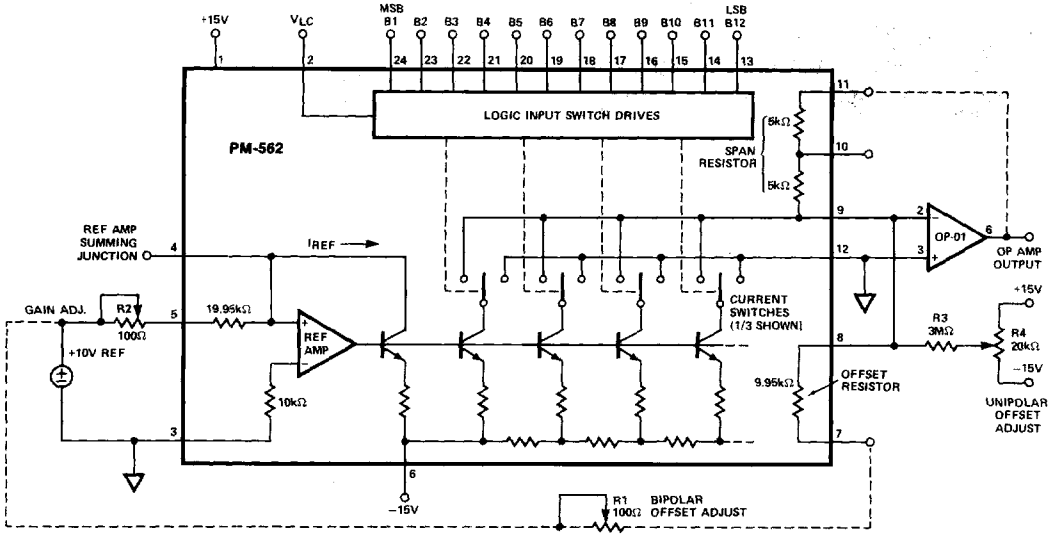
			PM-562H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N	T_A = Full Range	12	—	—	Bits
Monotonicity		T_A = Full Range	12	—	—	Bits
Nonlinearity	NL		—	—	±1/2	LSB
Differential Nonlinearity	DNL		—	—	±1/2	LSB
Settling Time	t_S	To ±1/2 LSB, all bits ON or OFF	—	1.5	—	µs
Output Voltage Compliance	V_{OC}		—	+10/–1.5	—	V
Full-Scale Output Current Range	I_{FR}	V_{REF} (+) = +10.0000V Unipolar R_2 = 50Ω Bipolar	–1.6 ±0.8	–2.0 ±1.0	–2.4 ±1.2	mA
Zero-Scale Current	I_{ZS}	*All bits OFF*	—	.005	0.05	%FS
Output Resistance	R_O		—	2	—	MΩ
Output Capacitance	C_O		—	30	—	pF
Reference Input Impedance	Z_{IN}	Pin 5	—	20	—	kΩ
Gain Error	I_{FSE}	R_2 = 50Ω, (Note 1)	—	±0.2	—	%FS
Bipolar Zero-Scale Error	I_{BZSE}	R_1 = 50Ω, (Note 1)	—	±0.1	—	%FS
Full-Scale Gain Adjustment Range	ΔI_{FSR}	R_2 = 100Ω Trimpot, (Note 1)	—	±0.25	—	%FS
Bipolar Zero-Scale Adjustment Range	ΔI_{BZSR}	R_1 = 100Ω Trimpot, (Note 1)	—	±0.25	—	%FS
Power Supply Gain Sensitivity	$+P_{SS}$ $-P_{SS}$	V+ = 5V or V+ ≈ 15V V– = –15V	— —	— —	2 6	ppmFS/%
Supply Current	I+ I–	V+ = 4.75V to 15.8V V– = –15V ± 10%	— —	5 –7	18 –25	mA
TTL Logic Input Voltage	V_{IH} V_{IL}	Pin 2 I_{IH} = 100nA Open Circuit I_{IL} = –100µA	2.0 —	— —	— 0.8	V
CMOS Voltage Logic Input	V_{IH} V_{IL}	Pin 2 I_{IH} = 100nA tied to Pin 1 I_{IL} = –100µA	70 —	— —	— 30	%V+

ELECTRICAL CHARACTERISTICS at V+ = 5V, V− = −15V, V_{REF} (+) = +10.0000V, V_{REF} (−) = 0V, 0°C ≤ T_A ≤ +70°C for PM-562H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562H MIN	TYP	MAX	UNITS
Zero-Scale Temperature Coefficient	TCI_{ZS}	Unipolar Leakage Current Change (Note 2)	—	—	2	ppmFS/°C
Bipolar Zero-Scale Temperature Coefficient	TCI_{BZS}	Bipolar (Note 2)	—	—	4	ppmFS/°C
Full-Scale Gain Temperature Coefficient	TCI_{FS}	Excludes V_{REF} (Note 2)	—	—	5	ppmFS/°C
Differential Nonlinearity Temperature Coefficient	TC_{DNL}	(Note 2)	—	2	—	ppmFS/°C

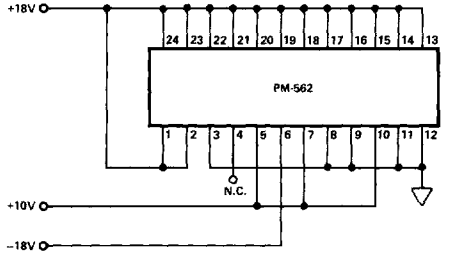
NOTES:
1. See connection diagram.
2. Guaranteed by design.

CONNECTION DIAGRAM

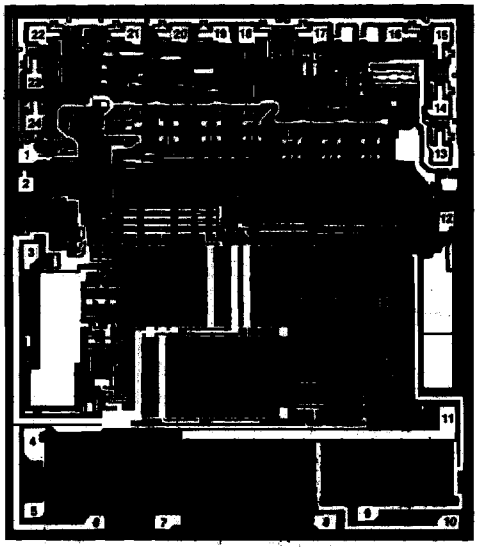


NOTE:
Set V_{LC} = V+ for CMOS logic inputs. Leave V_{LC} open circuit or grounded for TTL inputs.

BURN-IN CONFIGURATION



DICE CHARACTERISTICS



DIE SIZE 0.163 × 0.142 inch, 23,146 sq. mils
(4.140 × 3.607 mm, 14.933 sq. mm)

1. V+
2. V_{LC}
3. V_{REF} (–)
4. REF SUM JUNCTION
5. V_{REF} (+)
6. V–
7. BIPOLAR OFFSET "R" IN
8. BIPOLAR OFFSET "R" OUT
9. I_{OUT}
10. 10V SPAN
11. 20V SPAN
12. GROUND
13. BIT 12 (LSB)
14. BIT 11
15. BIT 10
16. BIT 9
17. BIT 8
18. BIT 7
19. BIT 6
20. BIT 5
21. BIT 4
22. BIT 3
23. BIT 2
24. BIT 1 (MSB)

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at V+ = 5V, V– = –15V, V_{REF} = 10.0000V, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562G LIMITS	UNITS
Nonlinearity	NL		±1/2	LSB
Differential Nonlinearity	DNL		±1/2	LSB
Zero-Scale Current	I_{ZS}	All Bits OFF	0.05	%FS
Full-Scale Output Current Range	I_{FR}	I_{REF} = 0.5mA Unipolar	–1.6/–2.4	mA
Logic Input High	V_{IH}	I_{IH} = 100nA	2	V
Logic Input Low	V_{IL}	I_{IL} = –100μA	0.8	V
Positive Supply Current	I+	V+ = 4.75 to 15.8V	18	mA
Negative Supply Current	I–	V– = –13.5 to –16.5V	–25	mA

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to varitions in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications bases on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 5V, V– = –15V, V_{REF} = 10.0000V, T_A = 25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562G TYPICAL	UNITS
Settling Time	t_S	to ±1/2 LSB, V_O = 0V	1.5	μs
Full-Scale Gain Temperature Coefficient	TCI_{FS}	Excludes V_{REF}	5	ppmFS/° C
Output Voltage Compliance	V_{OC}		–1.5/+10	V
Output Resistance	R_O		2	MΩ
Output Capacitance	C_O		30	pF
Power Supply Gain Sensitivity	$+P_{SS}$	V+ = +5V or +15V	2	ppmFS/%
Power Supply Gain Sensitivity	$-P_{SS}$	V– = –15V	6	ppmFS/%

APPLICATIONS INFORMATION

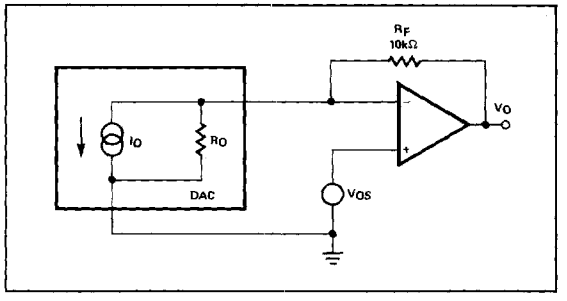
R_O EFFECT ON ACCURACY

The D/A converter equivalent circuit and output voltage equations show that a low output resistance (R_O) can provide a significant error term due to V_{OS} drift of the output amplifier. Note that the higher R_O (2MΩ) offered by the PM-562 gives an apparent V_{OS} drift that is one-half as large as that resulting from the 6.6kΩ R_O of the standard AD562 when using a 10kΩ span resistor (R_F).

$$\Delta V_O = \Delta I_O R_F + \Delta V_{OS}$$

Since: $\Delta I_O = \Delta V_{OS}/R_O$

Then: $\Delta V_O = \Delta V_{OS}(R_F/R_O + 1)$



LAYOUT SUGGESTIONS

Good layout practice appropriate for a 12-bit resolution analog system provides the overriding guideline. Power supplies should have small high frequency noise content. The V− (−15V) supply should be the cleanest since it has the most direct effect on I_{OUT}. The PM-562 should have bypass capacitors on both V+ and V− supplies. A tantulum or electrolytic 1 to 10 micro Farad in parallel with a ceramic 0.01 micro Farad bypass capacitor adequately attenuate high frequency supply noise.

The ground line between Pin-3 and Pin-12 should not conduct any other current paths. Placing the common ground point at Pin-12 provides good results. Pin-9 is the most sensitive node to high frequency noise pickup. Keep the signal path between Pin-9 and the current-to-voltage converter (op amp or resistor) as short as possible.

LOGIC INTERFACING (TTL OR CMOS)

The PM-562 digital inputs (BIT 1 through BIT 12) can be programmed by the V_{LC} (Pin-2) for TTL or CMOS logic input compatibility.

For TTL input compatibility leave Pin-2 open circuit or ground it to Pin-12. The logic threshold trip point stays at 1.4V for V+ set anywhere from 4.75 to 15.8V.

For CMOS input compatibility tie V_{LC} (Pin-2) to V+. This establishes the CMOS Logic threshold trip point at 1/2 of V+. Therefore V+ should be set to the same V_{DD} voltage used by the CMOS driving logic.

MULTIPLYING MODE

The output current of the PM-562 is the product of the reference voltage input and the number represented by the digital input code divided by 4096. The reference voltage $V_{REF\,(+)}$ must be positive with respect to $V_{REF\,(-)}$. The PM-562 typically maintains 12-bit linearity with reference voltages as small as one volt. Reference signal feedthrough is typically 60dB down at 10kHz with a digital input of zero. The DAC output typically takes 20 microseconds to settle to within 1/2 LSB for a 5 volt step on the reference input. The small signal bandwidth for a 100mVpp reference input signal is typically 65kHz, and the typical large signal bandwidth for a 5Vpp reference input signal is 20kHz.

UNIPOLAR OPERATION (0 to +10V OUTPUT)

Figure 1 shows the simplest unipolar setup for 0 to +10V operation. The output should be buffered since the output resistance is 5kΩ. The digital input code is complemented in this configuration. That is, binary "0" in produces +10V full-scale out. And all binary one's in produces 0V out.

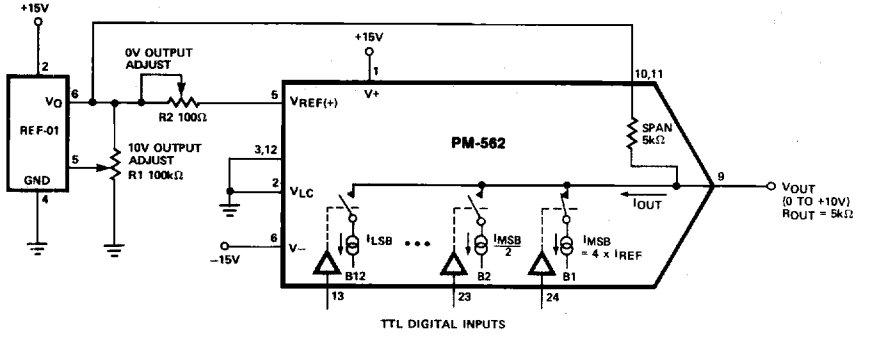
Figure 2 shows the best configuration to achieve a 0V to 10V output digital-to-analog converter. In this configuration digital "0" in produces 0V out. All one's in produces 10V out.

Calibration of Figure 2 is accomplished by placing digital "0" on all input bits and adjusting R1 until 0V appears at V_{OUT}. Next the span (or full-scale) is adjusted by R2 for an output voltage of 9.9976V.

BIPOLAR OPERATION (±10V OUTPUT)

The bipolar configuration of Figure 3 provides positive and negative output voltage under control of one's complement digital input coding. Calibration is accomplished by turning all bits OFF (digital zero input code) and adjusting trimmer R1 for −10.000V output. Next turn ON the MSB (digital 1000 0000 0000 input code) and adjust R2 for 0.0000V.

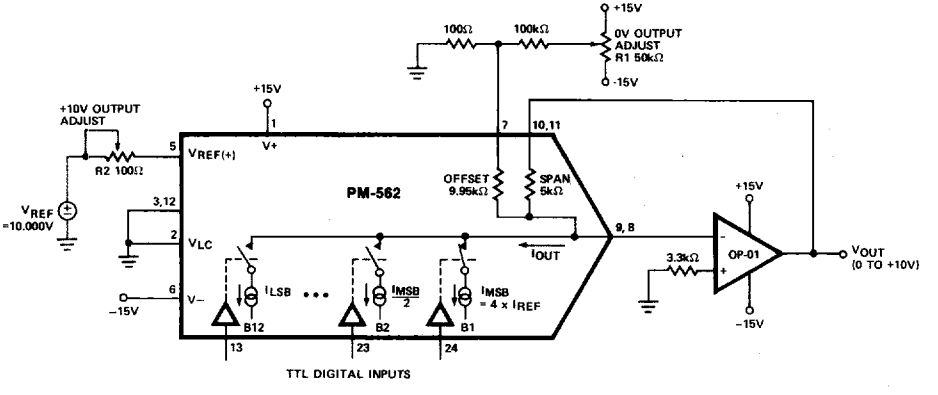
This circuit can easily be converted to ±5V output by connecting Pin-10 to the OP-01 output, making the span resistor 5kΩ.



NOTES:

1. This simple configuration presents a high output resistance of 5kΩ.
2. Calibration Procedure: First set digital inputs B_1 thru B_{12} to digital zero and adjust R_1 until $V_{OUT} = 10.0000V$. Next set digital inputs B_1 thru B_{12} to digital one's and adjust R_2 until $V_{OUT} = 0.0000V$. Use a high input resistance DVM to calibrate to avoid resistor divider error.
3. Bypass V+ and V– supplies with 0.01μF in parallel with 1μF capacitors.

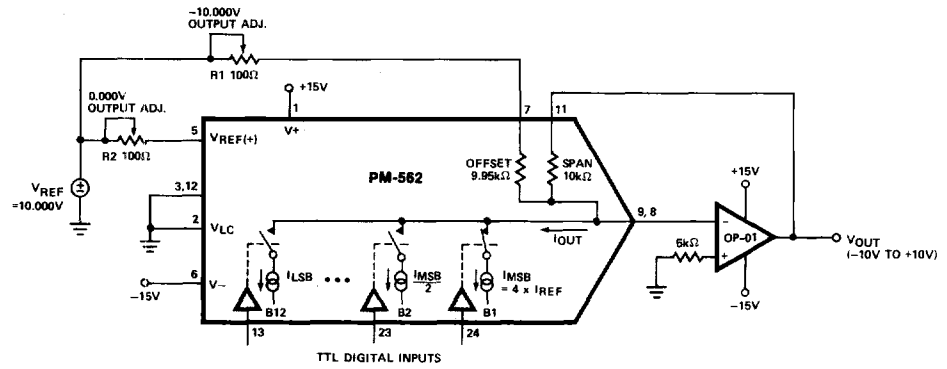
FIGURE 1: Unbuffered Unipolar 0 to +10V Output



NOTES:

1. Calibration Procedure: First set digital inputs B_1 thru B_{12} to digital zero and adjust R_1 until $V_{OUT} = 0.0000V$. Next set digital inputs B_1 thru B_{12} to digital one's and adjust R_2 until $V_{OUT} = 9.9976V$.
2. Bypass V+ and V– supplies with 0.01μF in parallel with 1μF capacitors.

FIGURE 2: +10V Unipolar Voltage Output

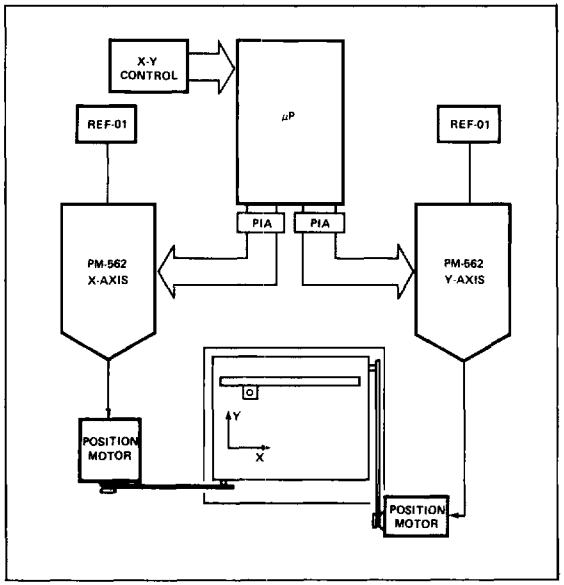


NOTES:

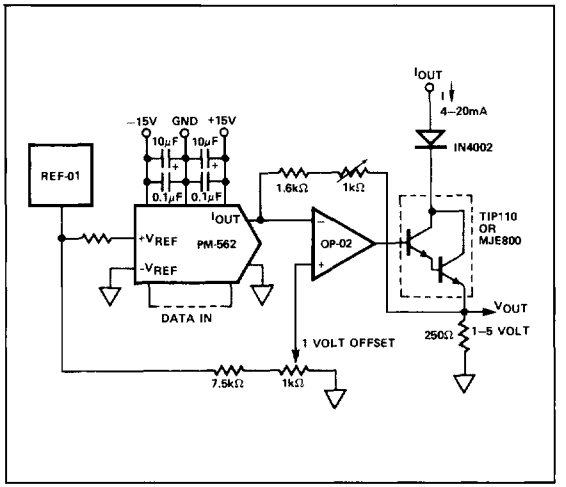
1. Calibration Procedure: Set $V_{REF} = 10.0000V$. Next set digital inputs B_1 thru B_{12} to digital zero and adjust R_1 until $V_{OUT} = -10.0000V$. Set digital inputs B_1 thru B_{12} to 1000 0000 0000 (i.e. only turn ON MSB) and adjust R_2 until $V_{OUT} = 0.0000V$.
2. Bypass V+ and V− supplies with 0.01μF in parallel with 1μF capacitors.

FIGURE 3: ±10V Bipolar Voltage Output

PRECISION X-Y POSITIONING SYSTEM



4-20mA TRANSMITTER



DIGITALLY CONTROLLED R.F. OSCILLATOR