SN74AVC2T45 2-Bit, Dual Supply, Bus Transceiver With Configurable Level-Shifting and Translation

1 Features

- Available in the Texas Instruments NanoFree™ Package
- V_{CC} Isolation Feature: If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Dual Supply Rail Design
- I/Os Are 4.6-V Over Voltage Tolerant
- I_{off} Supports Partial-Power-Down Mode Operation
- Max Data Rates
  - 500 Mbps (1.8 V to 3.3 V)
  - 320 Mbps (<1.8 V to 3.3 V)
  - 320 Mbps (Level-Shifting to 2.5 V or 1.8 V)
  - 280 Mbps (Level-Shifting to 1.5 V)
  - 240 Mbps (Level-Shifting to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22

2 Applications

- Smartphones
- Servers
- Desktop PCs and Notebooks
- Other Portable Devices

3 Description

This 2-bit non-inverting bus transceiver uses two separate configurable power-supply rails. The A ports are designed to track V_{CCA} and accepts any supply voltage from 1.2 V to 3.6 V. The B ports are designed to track V_{CCB} and accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

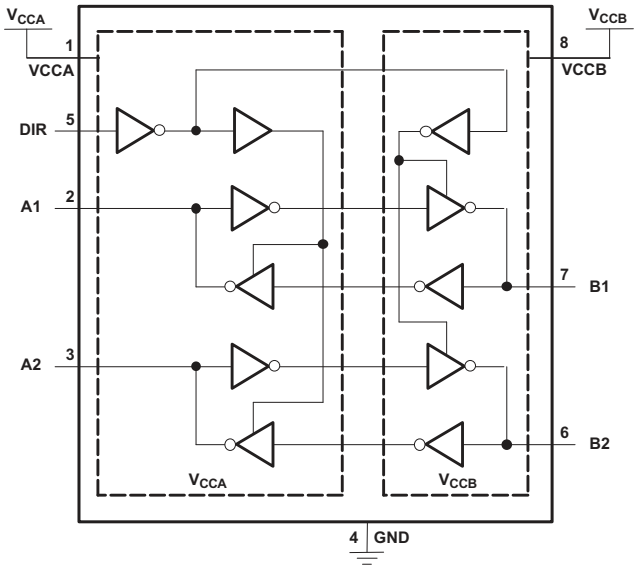
The SN74AVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR pin) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess leakage current on the internal CMOS structure.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC2T45DCT	SM8 (8)	2.95 mm × 2.80 mm
SN74AVC2T45DCU	VSSOP (8)	2.30 mm × 2.00 mm
SN74AVC2T45YZP	DSBGA (8)	1.89 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



(1) Pin numbers are for the DCT and DCU packages only.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (April 2015) to Revision L — **Page**

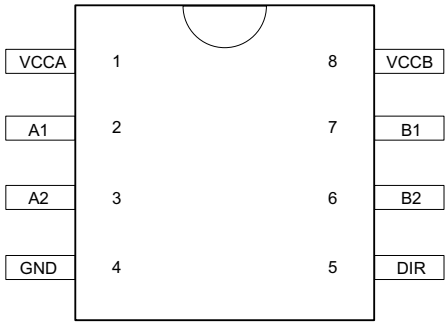
- Changed data sheet title ... 1
- Changed YZP package pinout diagram to bottom view ... 3
- Added Type column to *Pin Functions* table ... 3
- Added Junction temperature, T_J ... 4
- Added *Receiving Notification of Documentation Updates* and *Community Resources* ... 19

Changes from Revision J (June 2007) to Revision K — **Page**

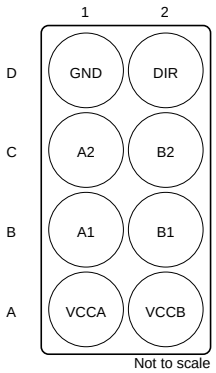
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DCT or DCU Package
8-Pin SM8 or VSSOP
Top View



YZP Package
8-Pin DSBGA
Bottom View



Not to scale

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO. (SM8, VSSOP)	NO. (DSBGA)		
VCCA	1	A1	—	Supply Voltage A
VCCB	8	A2	—	Supply Voltage B
GND	4	D1	—	Ground
A1	2	B1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
A2	3	C1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
B1	7	B2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
B2	6	C2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
DIR	5	D2	I	Direction Pin, Connect to GND or to VCCA

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	IO ports (A port)	–0.5	4.6	V
		IO ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model (MM), Per JEDEC specification JESD22-A115-A	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1) (2) (3)

			V_{CCI} (4)	V_{CCO} (5)	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs (2)	1.2 V to 1.95 V		V_{CCI} (4) × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs (2)	1.2 V to 1.95 V			V_{CCI} (4) × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA}) (3)	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA}) (3)	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO} (5)	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(3) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.
(4) V_{CCI} is the voltage associated with the input port supply VCCA or VCCB.
(5) V_{CCO} is the voltage associated with the output port supply VCCA or VCCB.

6.4 Thermal Information

THERMAL METRIC[1]		SN74AVC2T45			UNIT
		DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194.4	199.3	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.7	76.2	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.8	80.6	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	49.8	7.1	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	105.8	80.1	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1] [2]

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to +85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH} [3]		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2 V		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL} [3]		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.25				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	DIR	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V		0 V	0 to 3.6 V		±0.1	±1		±5	µA
	B port			0 to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ} [3]	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND		0 V	3.6 V		±0.5	±2.5		±5	µA
	A port			3.6 V	0 V		±0.5	±2.5		±5	
I_{CCA} [3]		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					10	µA
				0 V	3.6 V					–2	
				3.6 V	0 V					10	
I_{CCB} [3]		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					10	µA
				0 V	3.6 V					10	
				3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$ (see Table 1)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					20	µA
C_I	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		2.5				pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6				pF

(1) V_{CCO} is the voltage associated with the output port supply VCCA or VCCB.
(2) V_{CCI} is the voltage associated with the input port supply VCCA or VCCB.
(3) V_{OH}: Output High Voltage; V_{OL}: Output Low Voltage; I_{OZ}: Hi-Z Output Current; I_{CCA}: Supply A Current; I_{CCB}: Supply B Current

6.6 Switching Characteristics: V_{CCA} = 1.2 V

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH} (1)	A	B	3.1	2.6	2.4	2.2	2.2	ns
t_{PHL} (1)			3.1	2.6	2.4	2.2	2.2	
t_{PLH} (1)	B	A	3.4	3.1	3	2.9	2.9	ns
t_{PHL} (1)			3.4	3.1	3	2.9	2.9	
t_{PHZ} (1)	DIR	A	5.2	5.2	5.1	5	4.8	ns
t_{PLZ} (1)			5.2	5.2	5.1	5	4.8	
t_{PHZ} (1)	DIR	B	5	4	3.8	2.8	3.2	ns
t_{PLZ} (1)			5	4	3.8	2.8	3.2	
t_{PZH} (1) (2)	DIR	A	8.4	7.1	6.8	5.7	6.1	ns
t_{PZL} (1) (2)			8.4	7.1	6.8	5.7	6.1	
t_{PZH} (1) (2)	DIR	B	8.3	7.8	7.5	7.2	7	ns
t_{PZL} (1) (2)			8.3	7.8	7.5	7.2	7	

(1) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay
(2) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

6.7 Switching Characteristics: V_{CCA} = 1.5 V ±0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (1)	A	B	2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	ns
t_{PHL} (1)			2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	
t_{PLH} (1)	B	A	2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	ns
t_{PHL} (1)			2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	
t_{PHZ} (1)	DIR	A	3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	ns
t_{PLZ} (1)			3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	
t_{PHZ} (1)	DIR	B	4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	ns
t_{PLZ} (1)			4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	
t_{PZH} (1) (2)	DIR	A	7.4		12.4		12.1		11.8		11.8	ns
t_{PZL} (1) (2)			7.4		12.4		12.1		11.8		11.8	
t_{PZH} (1) (2)	DIR	B	6.7		13.9		12.4		11.4		11.1	ns
t_{PZL} (1) (2)			6.7		13.9		12.4		11.4		11.1	

(1) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay
(2) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

6.8 Switching Characteristics: V_{CCA} = 1.8 V ±0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (1)	A	B	2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1	ns
t_{PHL} (1)			2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1	
t_{PLH} (1)	B	A	2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8	ns
t_{PHL} (1)			2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8	
t_{PHZ} (1)	DIR	A	3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2	ns
t_{PLZ} (1)			3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2	
t_{PHZ} (1)	DIR	B	4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9	ns
t_{PLZ} (1)			4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9	
t_{PZH} (1) (2)	DIR	A	6.8		10.5		10.3		9.7		9.7	ns
t_{PZL} (1) (2)			6.8		10.5		10.3		9.7		9.7	
t_{PZH} (1) (2)	DIR	B	6.4		13.3		11.2		8.7		8.3	ns
t_{PZL} (1) (2)			6.4		13.3		11.2		8.7		8.3	

(1) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay
(2) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

6.9 Switching Characteristics: V_{CCA} = 2.5 V ±0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (1)	A	B	2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6	ns
t_{PHL} (1)			2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6	
t_{PLH} (1)	B	A	2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8	ns
t_{PHL} (1)			2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8	
t_{PHZ} (1)	DIR	A	2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3	ns
t_{PLZ} (1)			2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3	
t_{PHZ} (1)	DIR	B	3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1	ns
t_{PLZ} (1)			3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1	
t_{PZH} (1) (2)	DIR	A	5.9		8.5		7.7		7.2		6.9	ns
t_{PZL} (1) (2)			5.9		8.5		7.7		7.2		6.9	
t_{PZH} (1) (2)	DIR	B	5		12.8		10.4		8		6.9	ns
t_{PZL} (1) (2)			5		12.8		10.4		8		6.9	

(1) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay
(2) The enable time is a calculated value, derived using the formula shown in the *Enable Times* section.

6.10 Switching Characteristics: V_{CCA} = 3.3 V ±0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} (1)	A	B	2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4	ns
t_{PHL} (1)			2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4	
t_{PLH} (1)	B	A	2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4	ns
t_{PHL} (1)			2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4	
t_{PHZ} (1)	DIR	A	2.9	1.1	8	1	6.5	1.3	4.7	1.2	4	ns
t_{PLZ} (1)			2.9	1.1	8	1	6.5	1.3	4.7	1.2	4	
t_{PHZ} (1)	DIR	B	3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2	ns
t_{PLZ} (1)			3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2	
t_{PZH} (1) (2)	DIR	A	5.5		10.2		8.7		7.2		6.6	ns
t_{PZL} (1) (2)			5.5		10.2		8.7		7.2		6.6	
t_{PZH} (1) (2)	DIR	B	5.4		12.7		10.3		7.5		6.4	ns
t_{PZL} (1) (2)			5.4		12.7		10.3		7.5		6.4	

(1) t_{PLH}: Low-to-high Propagation Delay; t_{PHL}: High-to-Low Propagation Delay; t_{PHZ}: High-to-Hi-Z Propagation Delay; t_{PLZ}: Low-to-Hi-Z Propagation Delay; t_{PZH}: Hi-Z-to-High Propagation Delay; t_{PZL}: Hi-Z-to-Low Propagation Delay
(2) The enable time is a calculated value, derived using the formula shown in the section.

6.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r (2) = t_f (2) = 1 ns	3	3	3	3	4	pF
	B-port input, A-port output		12	13	13	14	15	
C_{pdB} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r (2) = t_f (2) = 1 ns	12	13	13	14	15	pF
	B-port input, A-port output		3	3	3	3	4	

(1) Power-dissipation capacitance per transceiver
(2) t_r: Rise time; t_f: Fall time

6.12 Typical Characteristics

Table 1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

6.12.1 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.2 V

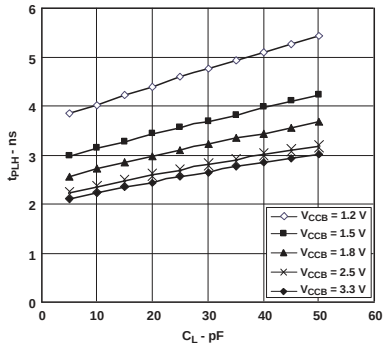


Figure 1. Typical A-to-B Propagation Delay, Low to High

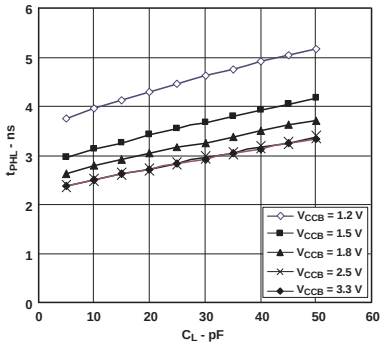


Figure 2. Typical A-to-B Propagation Delay, High to Low

6.12.2 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.5 V

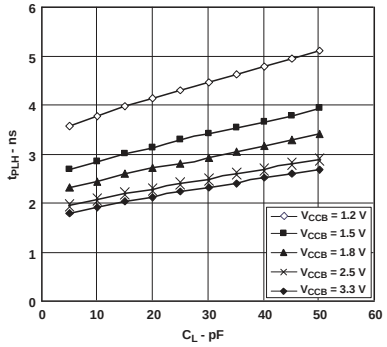


Figure 3. Typical A-to-B Propagation Delay, Low to High

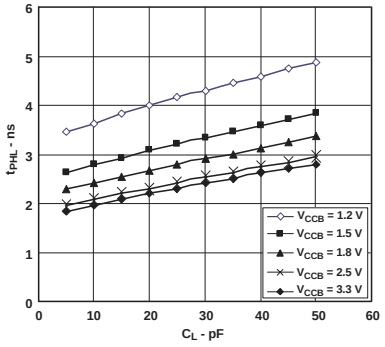


Figure 4. Typical A-to-B Propagation Delay, High to Low

6.12.3 Typical Propagation Delay (A-to-B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 1.8 V

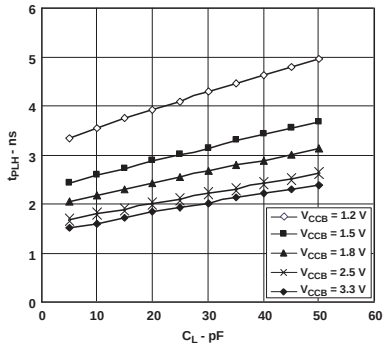


Figure 5. Typical A-to-B Propagation Delay, Low to High

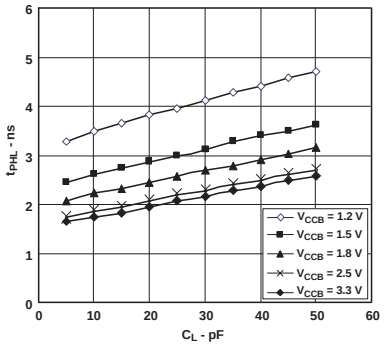


Figure 6. Typical A-to-B Propagation Delay, High to Low

6.12.4 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 2.5 V

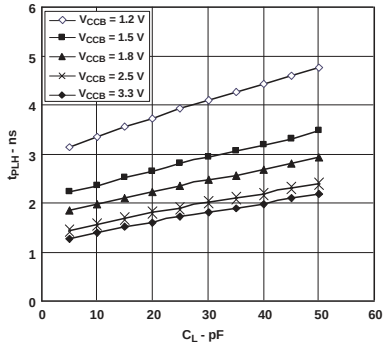


Figure 7. Typical A-to-B Propagation Delay, Low to High

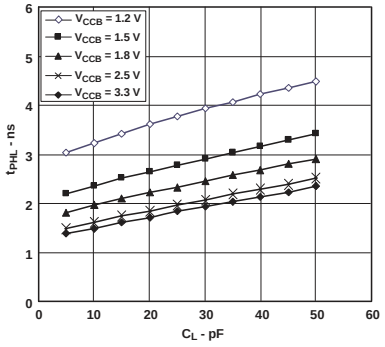


Figure 8. Typical A-to-B Propagation Delay, High to Low

6.12.5 Typical Propagation Delay (A to B) vs Load Capacitance, T_A = 25°C, V_{CCA} = 3.3 V

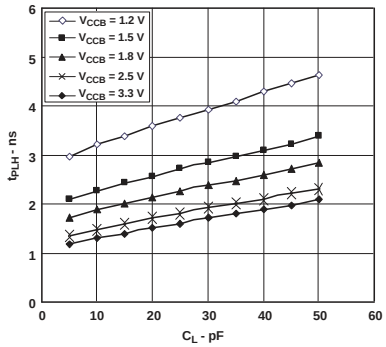


Figure 9. Typical A-to-B Propagation Delay, Low to High

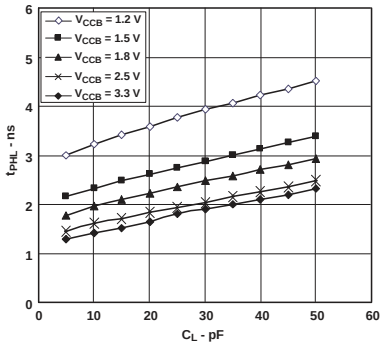
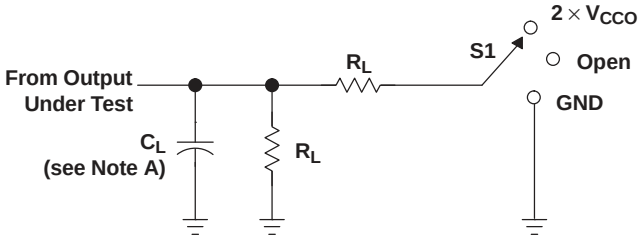


Figure 10. Typical A-to-B Propagation Delay, High to Low

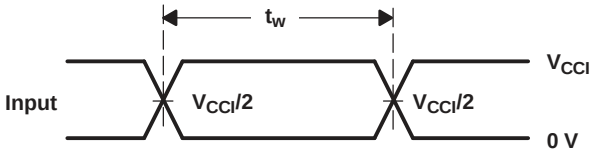
7 Parameter Measurement Information



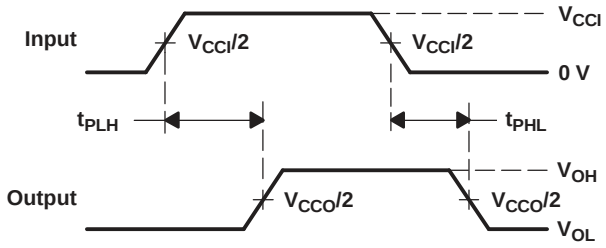
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

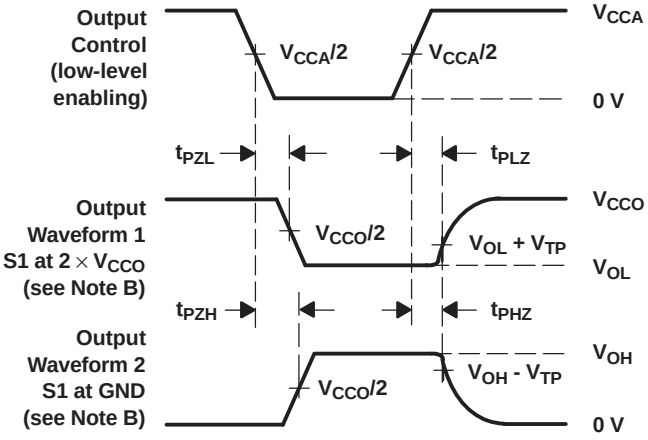
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} and accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} and accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

The SN74AVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

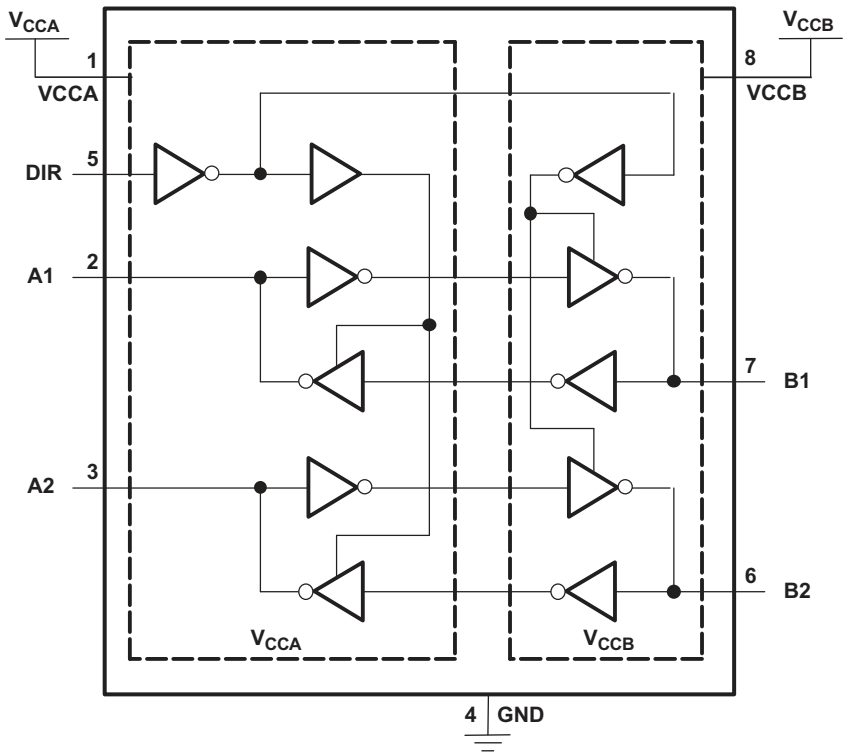
The SN74AVC2T45 is designed so that the DIR input is powered by supply voltage from VCCA.

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either VCC input is at GND, both ports are put in a high-impedance state. This will prevent a false high or low logic being presented at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

8.2 Functional Block Diagram



Pin numbers are for the DCT and DCU packages only.

Figure 12. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 VCC Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ} shown in *Electrical Characteristics*). This prevents false logic levels from being presented to either bus.

8.3.2 2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2 V to 3.6 V power-supply range.

8.3.3 IO Ports are 4.6-V Tolerant

The IO ports are up to 4.6 V tolerant.

8.3.4 Partial-Power-Down Mode

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.4 Device Functional Modes

Table 2 shows the functional modes of the SN74AVC2T45.

Table 2. Function Table(1)
(Each Transceiver)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data IOs always are active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

9.2 Typical Applications

9.2.1 Unidirectional Logic Level-Shifting Application

Figure 13 is an example circuit of the SN74AVC2T45 used in a unidirectional logic level-shifting application.

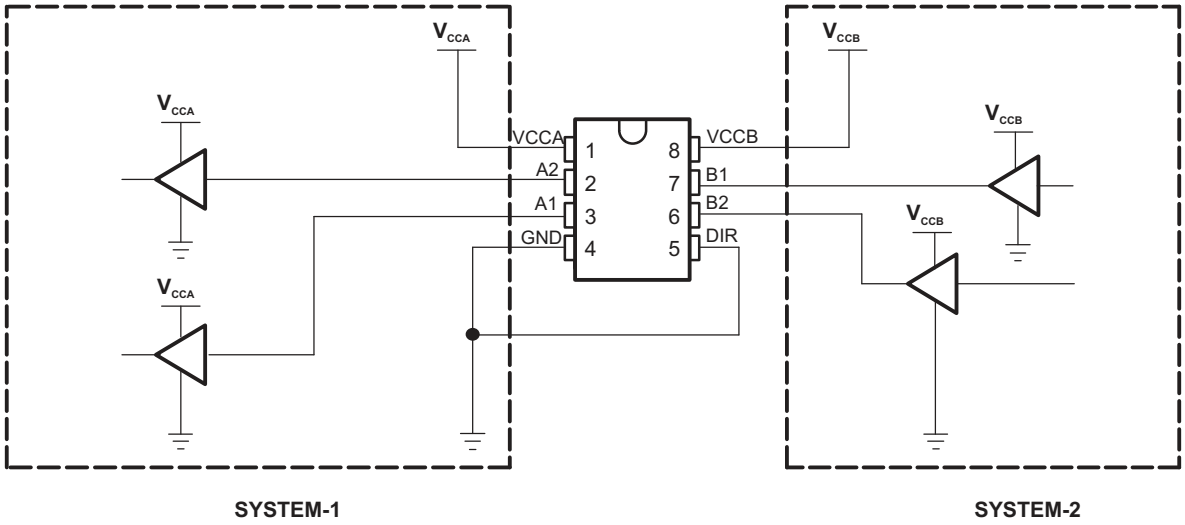


Figure 13. Unidirectional Logic Level-Shifting Application

9.2.1.1 Design Requirements

Table 3 lists the pins and pin descriptions of the SN74AVC2T45 connections with SYSTEM-1 and SYSTEM-2.

Table 3. SN74AVC2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

PIN	NAME	DESCRIPTION
1	VCCA	SYSTEM-1 supply voltage (1.2 V to 3.6 V)
2	A1	Output level depends on V_{CCA}.
3	A2	Output level depends on V_{CCA}.
4	GND	Device GND
5	DIR	The GND (low-level) determines B-port to A-port direction.
6	B2	Input threshold value depends on V_{CCB}.
7	B1	Input threshold value depends on V_{CCB}.
8	VCCB	SYSTEM-2 supply voltage (1.2 V to 3.6 V)

9.2.1.2 Detailed Design Procedure

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Make sure to tie any unused input and output ports directly to ground.

9.2.1.3 Application Curve

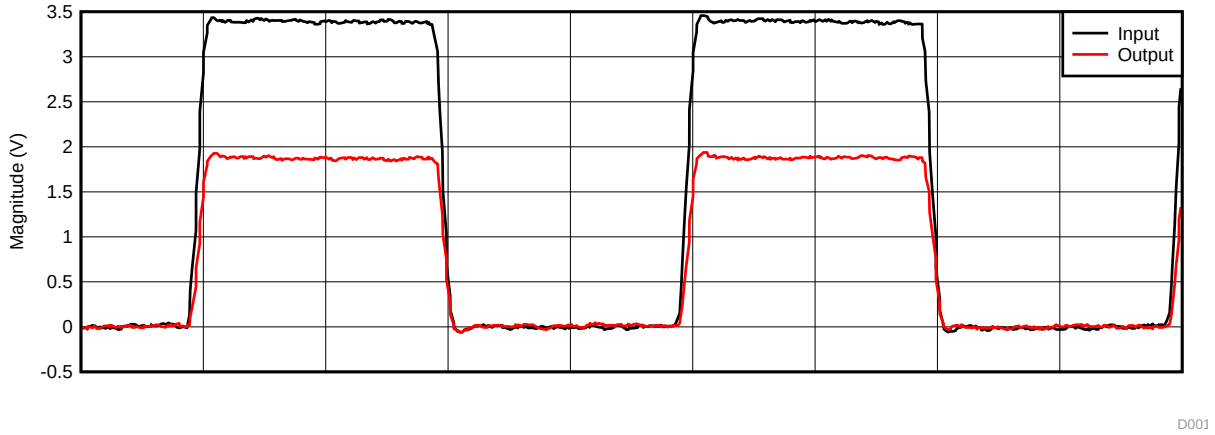


Figure 14. 3.3 V to 1.8 V Level-Shifting With 1-MHz Square Wave

9.2.2 Bidirectional Logic Level-Shifting Application

Figure 15 shows the SN74AVC2T45 used in a bidirectional logic level-shifting application.

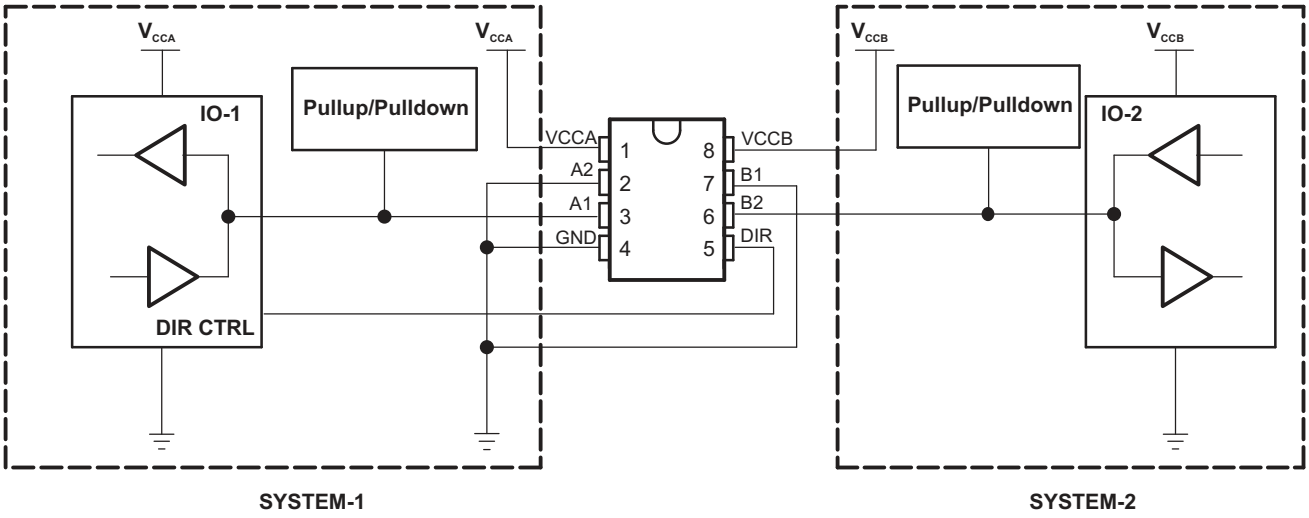


Figure 15. Bidirectional Logic Level-Shifting Application

9.2.2.1 Design Requirements

The SN74AVC2T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

9.2.2.2 Detailed Design Procedure

Table 4 shows a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

Table 4. Data Transmission Sequence

STATE	DIR CTRL	IO-1	IO-2	DESCRIPTION
1	H	Output	Input	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. IO-1 and IO-2 are disabled. The bus-line state depends on pullup or pulldown.(1)
3	L	Hi-Z	Hi-Z	DIR bit is flipped. IO-1 and IO-2 still are disabled. The bus-line state depends on pullup or pulldown.(1)
4	L	Input	Output	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

9.2.2.2.1 Enable Times

Calculate the enable times for the SN74AVC2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

10 Power Supply Recommendations

A proper power-up sequence always should be followed to avoid excessive current on the supply pin, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

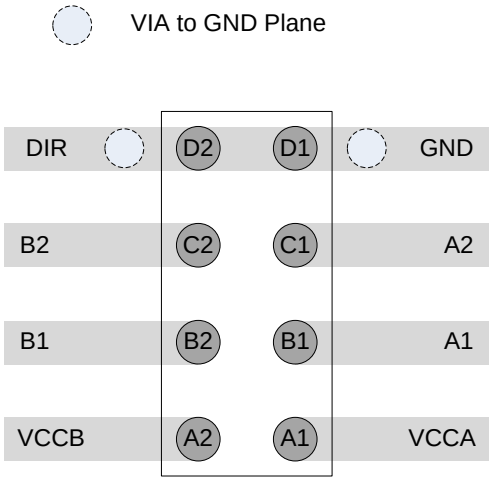


Figure 16. Layout Example for YZP Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC2T45DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z	Samples
SN74AVC2T45DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z	Samples
SN74AVC2T45DCTT	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z	Samples
SN74AVC2T45DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ	Samples
SN74AVC2T45DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R	Samples
SN74AVC2T45DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R	Samples
SN74AVC2T45DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R	Samples
SN74AVC2T45YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TDN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

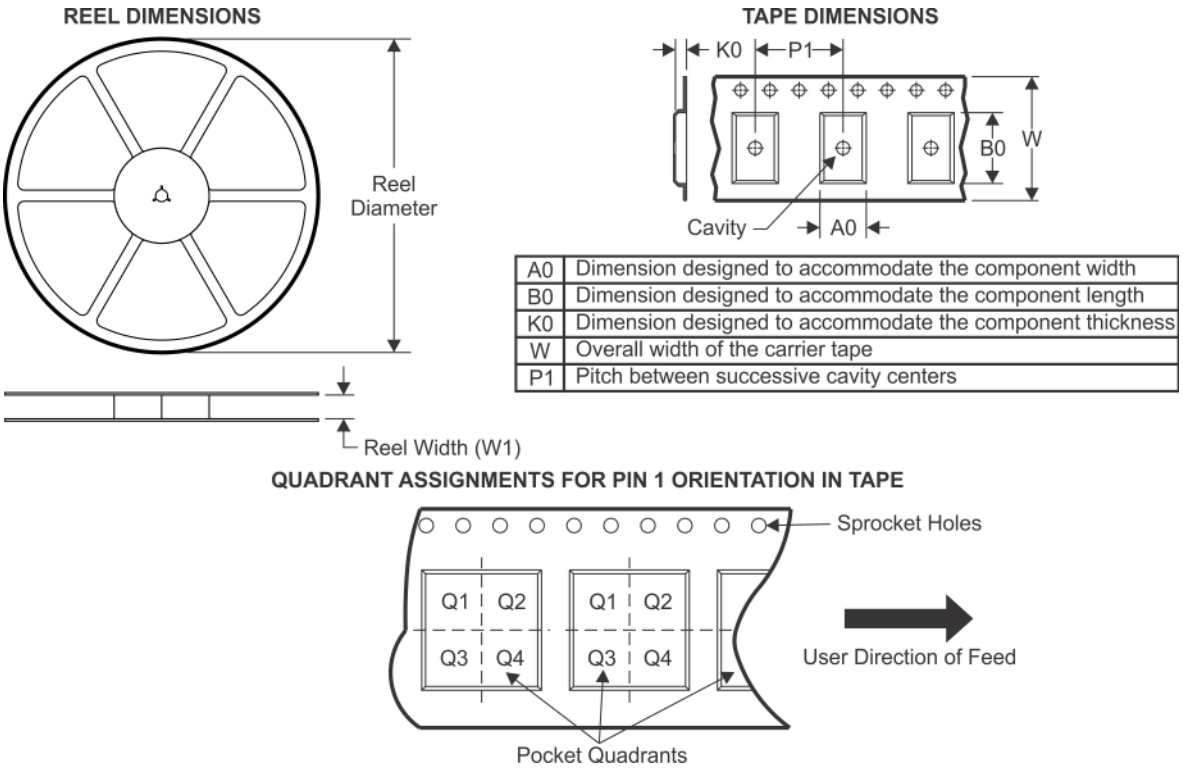
OTHER QUALIFIED VERSIONS OF SN74AVC2T45 :

- Automotive : SN74AVC2T45-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

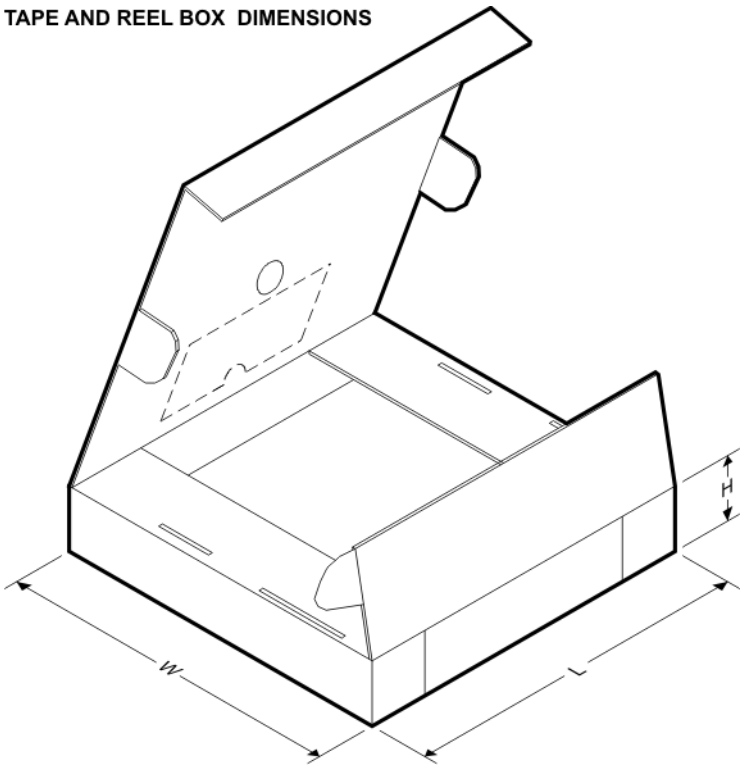


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T45DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

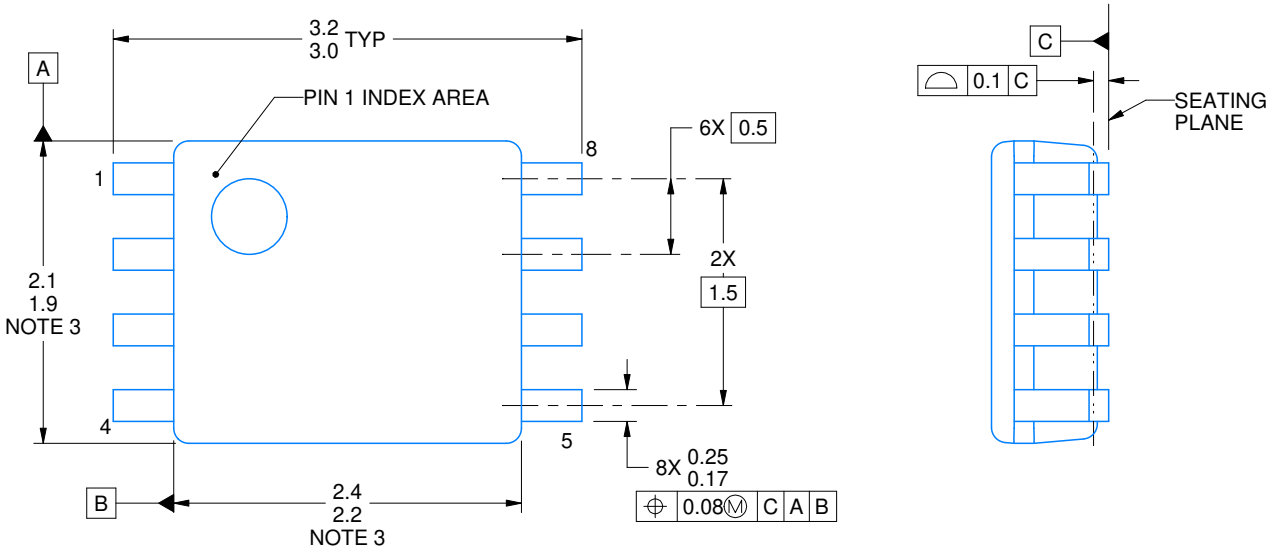
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T45DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74AVC2T45DCTT	SM8	DCT	8	250	182.0	182.0	20.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

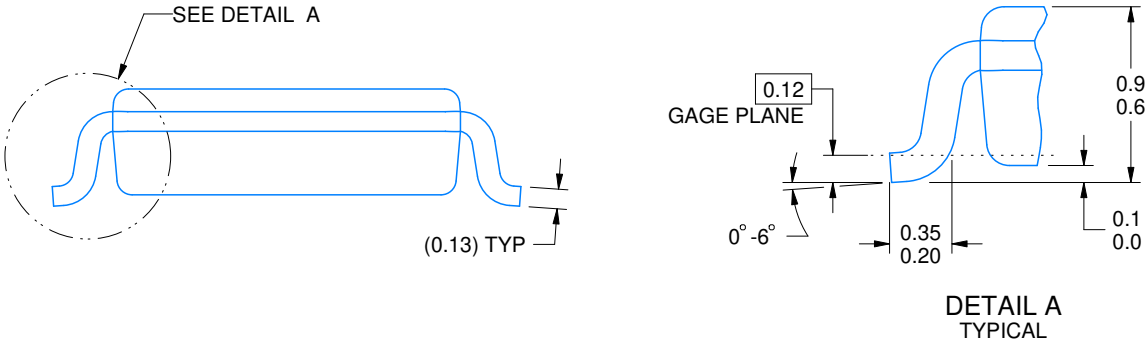
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

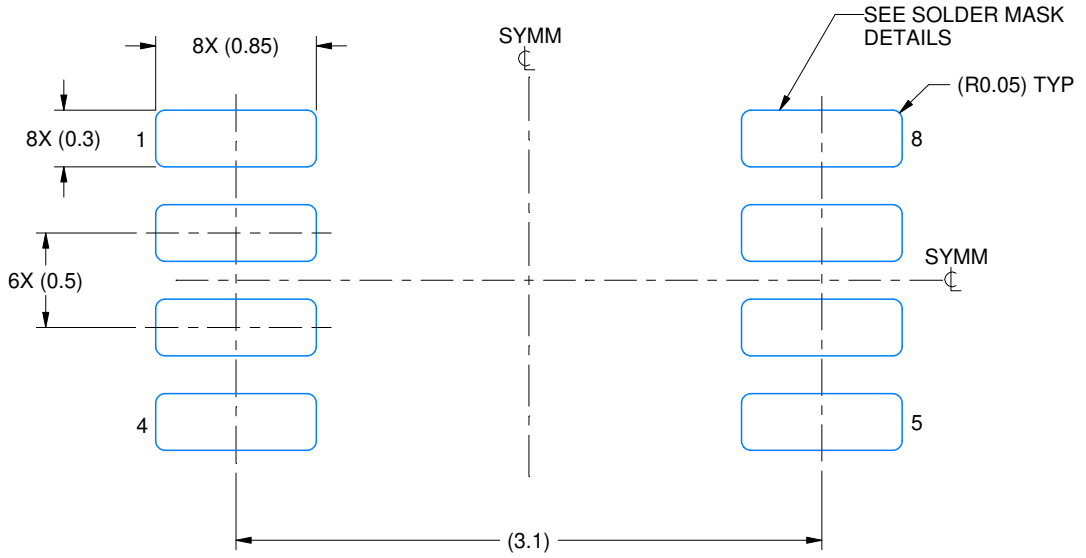




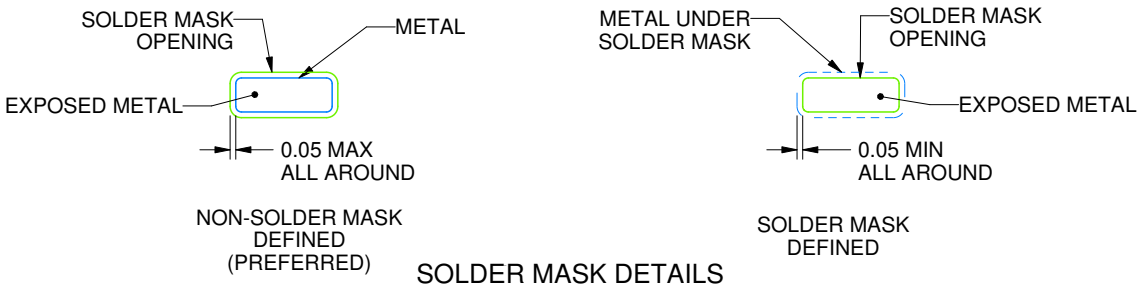
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

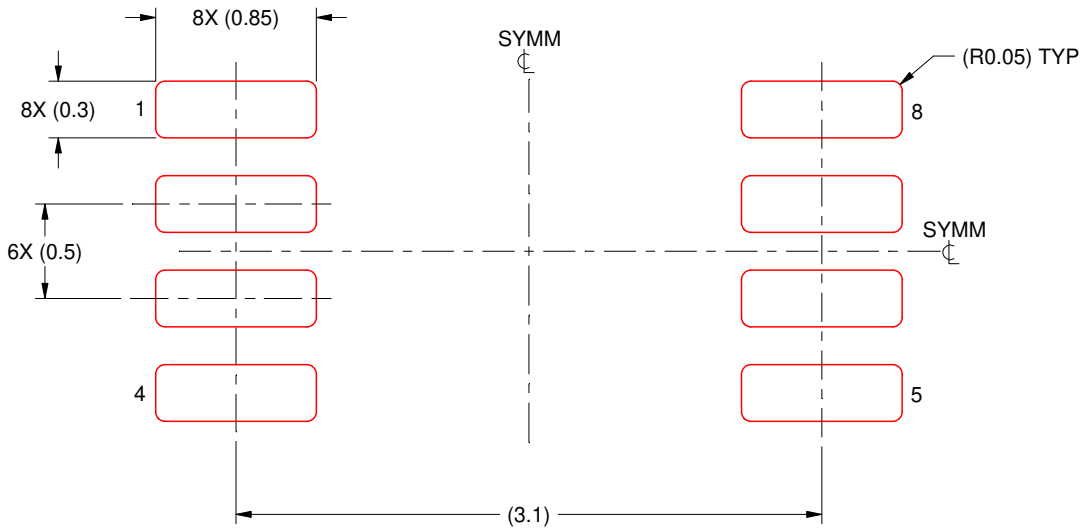


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

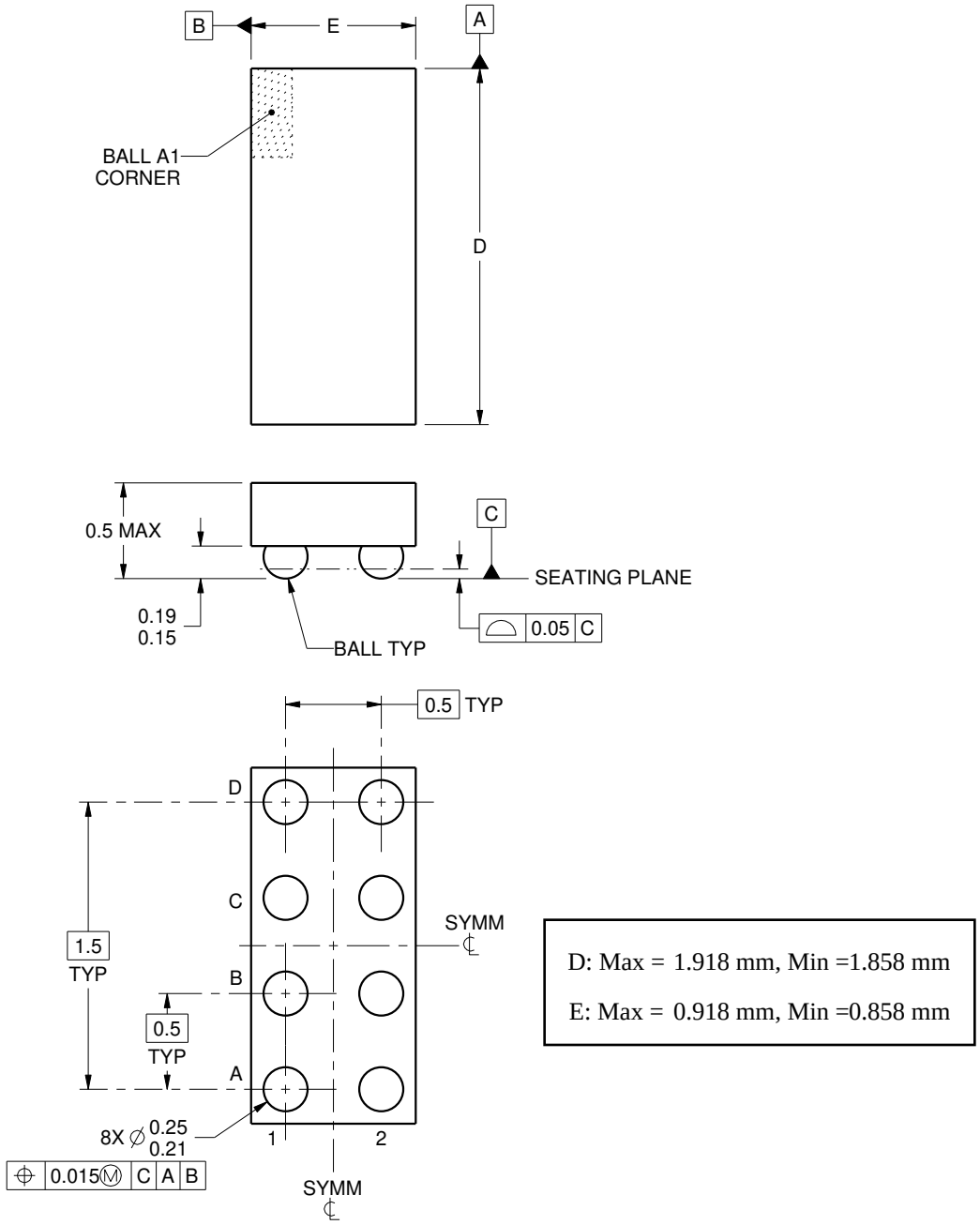
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

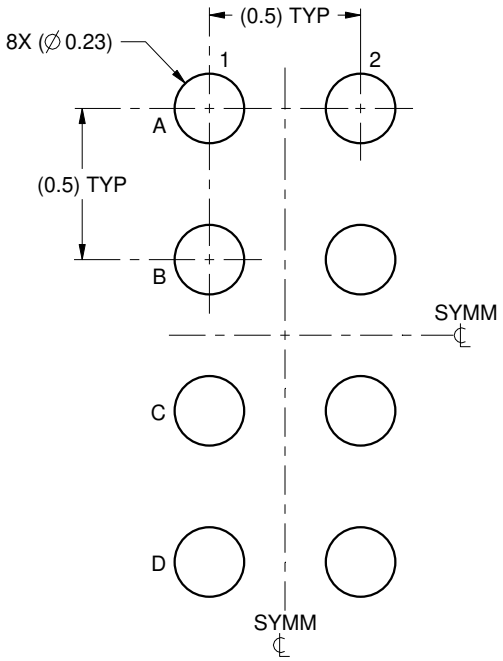
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

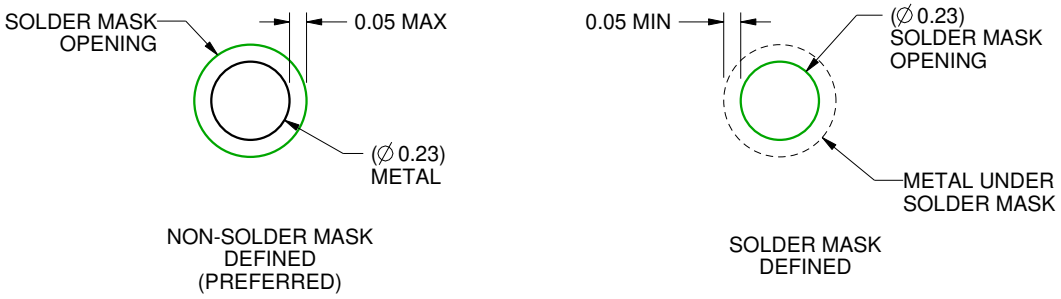


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

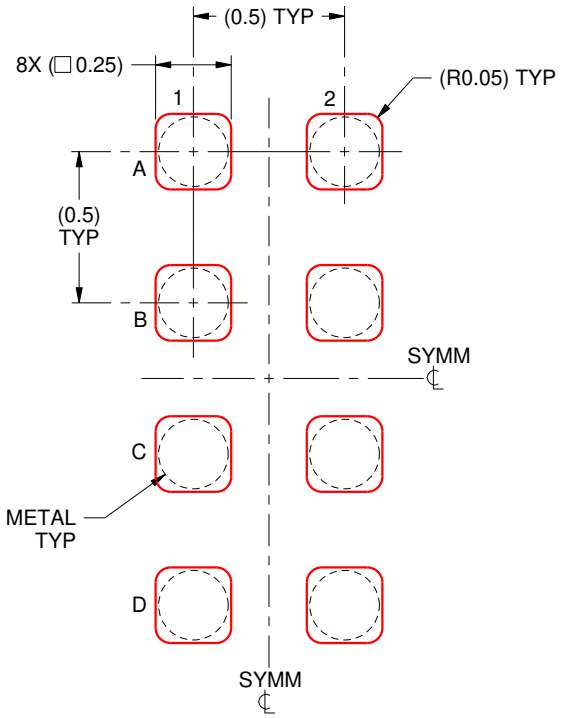


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

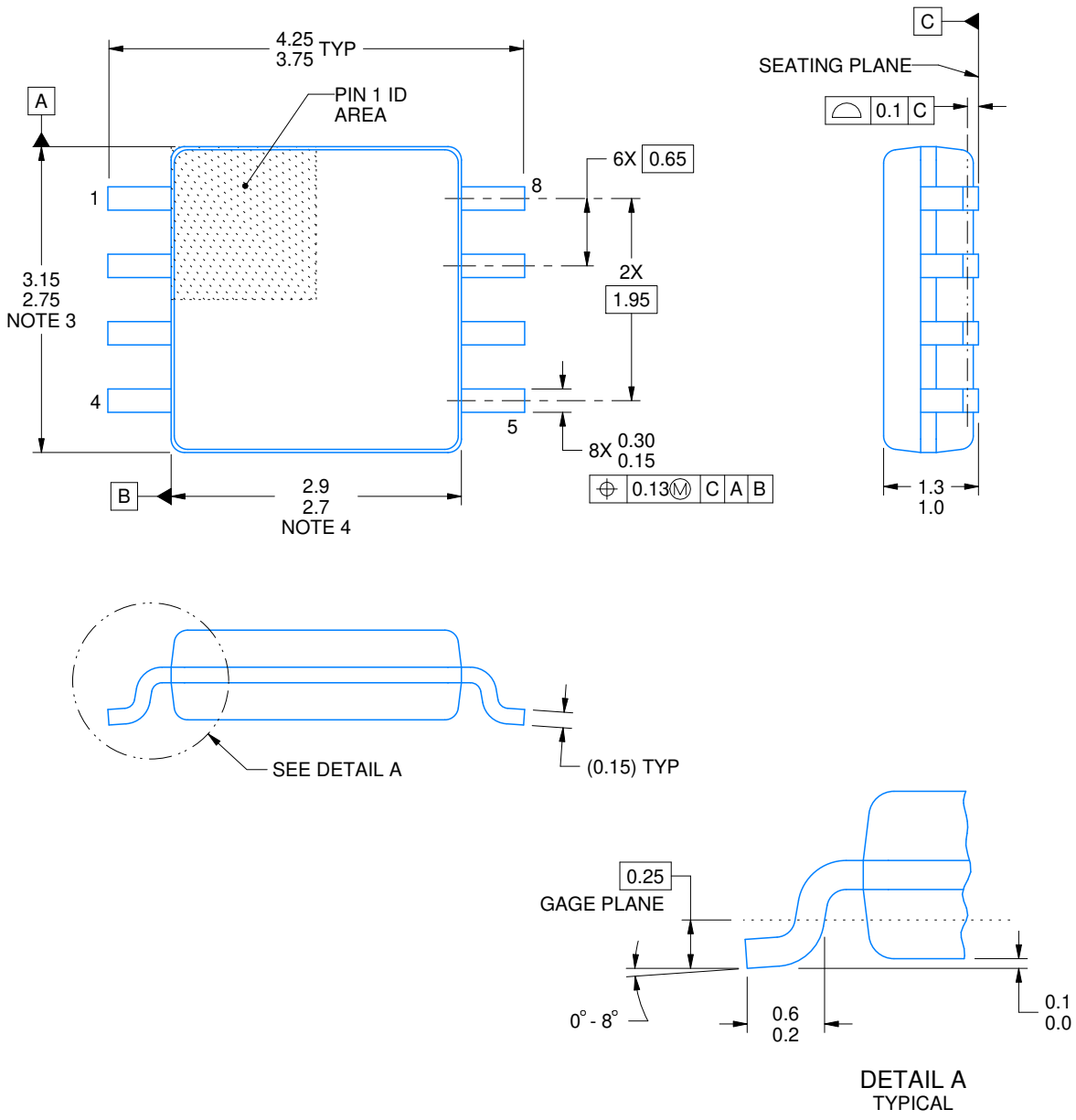
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

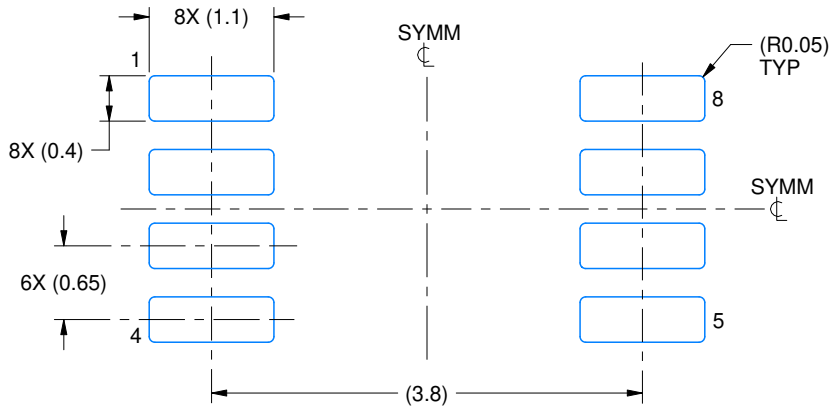
SMALL OUTLINE PACKAGE



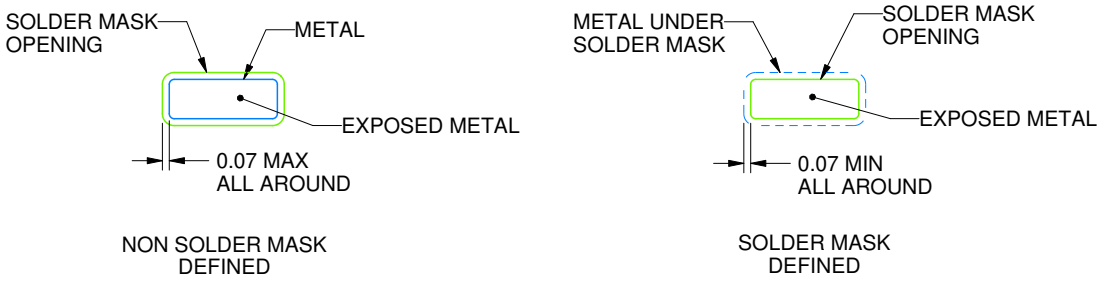
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

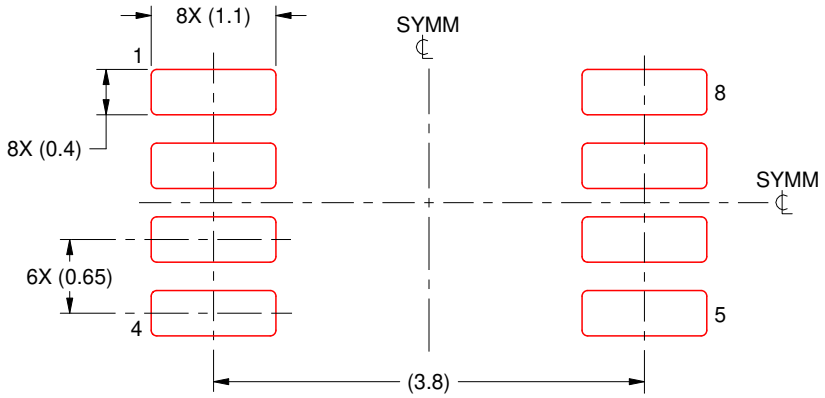


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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