

DATA SHEET

74F821

10-bit bus interface register, non-inverting
(3-State)

Product data sheet
Replaces data sheet 74F821/822/823/824/825/826
of 1996 Jan 05

2004 Jul 22

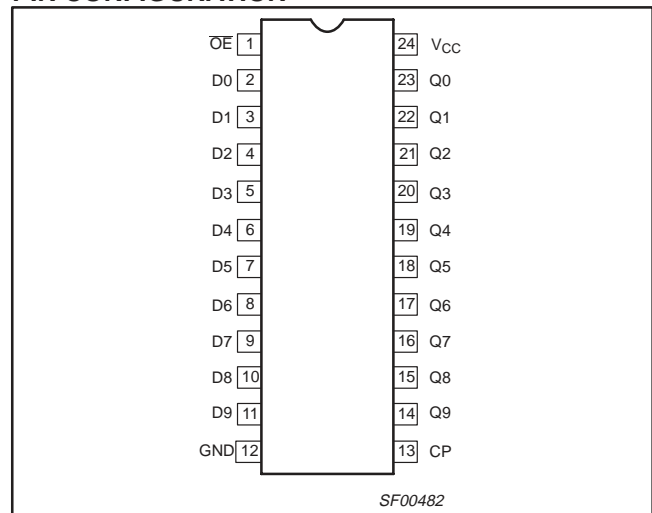
10-bit bus interface register, non-inverting (3-State)

74F821

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- High performance bus interface buffering for wide data/address paths or buses carrying parity
- High-impedance PNP base inputs for reduced loading (20 μ A in HIGH and LOW states)
- I_{IL} is 20 μ A versus 1000 μ A for AM29821 series
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessor
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29821
- Outputs sink 64 mA and source 24 mA

PIN CONFIGURATION



DESCRIPTION

The 74F821 bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74F821 is a buffered 10-bit wide version of the popular 74F374/74F534 functions.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F821	180 MHz	75 mA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/1.0	20 μ A/0.6 mA
CP	Clock input	1.0/1.0	20 μ A/0.6 mA
\overline{OE}	Output enable input (active-LOW)	1.0/3.0	20 μ A/1.8 mA
Qn	Data outputs	1200/106.7	24 mA/64 mA

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the HIGH state and 0.6 mA in the LOW state.

ORDERING INFORMATION

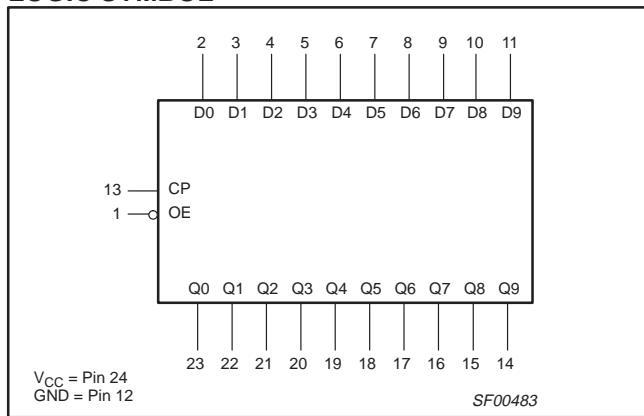
Commercial range: $V_{CC} = 5 V \pm 10\%$; $T_{amb} = 0^\circ C$ to $+70^\circ C$

Type number	Package		
	Name	Description	Version
N74F821D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
N74F821N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1

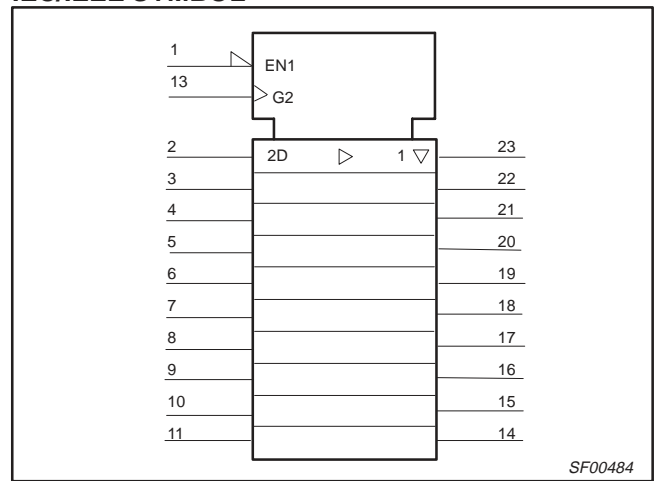
10-bit bus interface register, non-inverting (3-State)

74F821

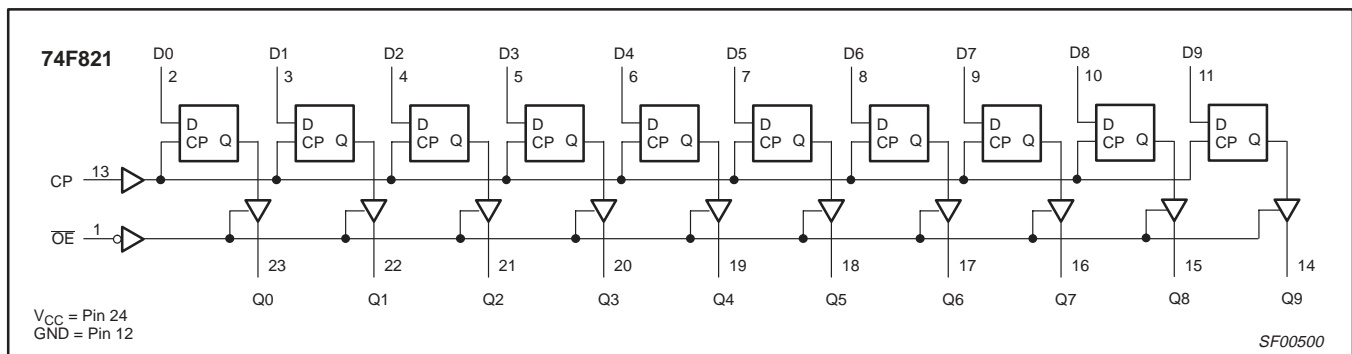
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
OE	CP	Dn	Q	
L	↑	l	L	Load and read data
L	↑	h	H	
L	↑̄	X	NC	Hold
H	X	X	Z	High-impedance

- H = HIGH-voltage level
- h = HIGH state must be present one setup time before the LOW-to-HIGH clock transition
- L = LOW-voltage level
- l = LOW state must be present one setup time before the LOW-to-HIGH clock transition
- NC= No change
- X = Don't care
- Z = High-impedance "off" state
- ↑ = LOW-to-HIGH clock transition
- ↑̄ = Not LOW-to-HIGH clock transition

10-bit bus interface register, non-inverting (3-State)

74F821

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in LOW output state	128	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	HIGH-level input voltage	2.0	-	-	V
V _{IL}	LOW-level input voltage	-	-	0.8	V
I _{IK}	Input clamp current	-	-	-18	mA
I _{OH}	HIGH-level output current	-	-	-24	mA
I _{OL}	LOW-level output current	-	-	64	mA
T _{amb}	Operating free-air temperature range	0	-	+70	°C

10-bit bus interface register, non-inverting (3-State)

74F821

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹		LIMITS			UNIT	
				MIN	TYP ²	MAX		
V _{OH}	HIGH-level output voltage	V _{CC} = MIN; V _{IL} = MAX; V _{IH} = MIN	I _{OH} = -15 mA	± 10 %V _{CC}	2.4	–	–	V
				± 5 %V _{CC}	2.4	–	–	V
			I _{OH} = -24 mA	± 10 %V _{CC}	2.0	–	–	V
				± 5 %V _{CC}	2.0	–	–	V
V _{OL}	LOW-level output voltage	V _{CC} = MIN; V _{IL} = MAX; V _{IH} = MIN	I _{OL} = MAX	± 10 %V _{CC}	–	–	0.55	V
				± 5 %V _{CC}	–	0.42	0.55	V
V _{IK}	Input clamp voltage	V _{CC} = MIN; I _I = I _{IK}		–	-0.73	-1.2	V	
I _I	Input current at maximum input voltage	V _{CC} = 0 V; V _I = 7.0 V		–	–	100	μA	
I _{IH}	HIGH-level input current	V _{CC} = MAX; V _I = 2.7 V		–	–	20	μA	
I _{IL}	LOW-level input current	V _{CC} = MAX; V _I = 0.5 V		–	–	-20	μA	
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX; V _O = 2.7 V		–	–	50	μA	
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX; V _O = 0.5 V		–	–	-50	μA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		-100	–	-225	mA	
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX	–	75	105	mA	
		I _{CCL}		–	75	105	mA	
		I _{CCZ}		–	75	115	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

10-bit bus interface register, non-inverting (3-State)

74F821

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V C _L = 50 pF, R _L = 500 Ω			T _{amb} = 0 °C to +70 °C V _{CC} = +5.0 V ± 10 % C _L = 50 pF, R _L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{max}	Maximum clock frequency	Waveform 1	150	180	–	140	–	ns
t _{PLH} t _{PHL}	Propagation delay CP to Qn	Waveform 1	4.0	6.5	8.5	4.0	9.5	ns
t _{PZH} t _{PZL}	Output enable time OE _n to Qn	Waveform 3 Waveform 4	2.0	4.5	8.0	2.0	9.0	ns
t _{PHZ} t _{PLZ}	Output disable time OE _n to Qn	Waveform 3 Waveform 4	1.5	3.5	6.5	1.5	7.5	ns

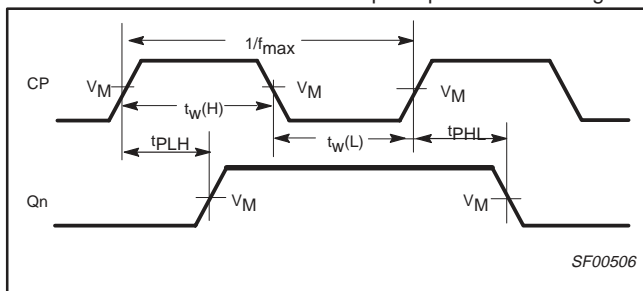
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25 °C V _{CC} = +5.0 V C _L = 50 pF, R _L = 500 Ω			T _{amb} = 0 °C to +70 °C V _{CC} = +5.0 V ± 10 % C _L = 50 pF, R _L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{su} (H) t _{su} (L)	Setup time, HIGH or LOW Dn to CP	Waveform 2	1.0	–	–	1.0	–	ns
t _h (H) t _h (L)	Hold time, HIGH or LOW Dn to CP	Waveform 2	2.0	–	–	2.0	–	ns
t _w (H) t _w (L)	CP Pulse width, HIGH or LOW	Waveform 1	3.5	–	–	4.0	–	ns

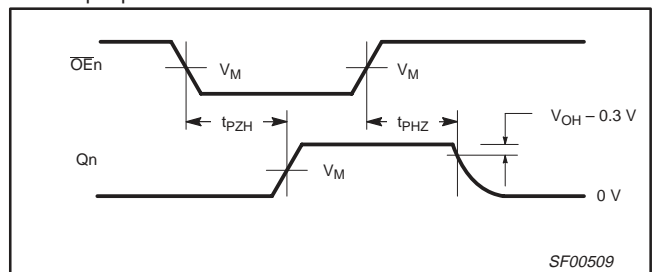
AC WAVEFORMS

For all waveforms, V_M = 1.5 V.

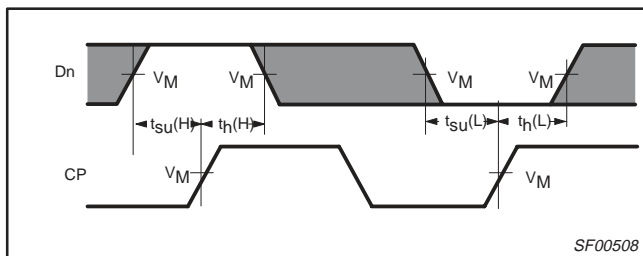
The shaded areas indicate when the input is permitted to change for predictable output performance.



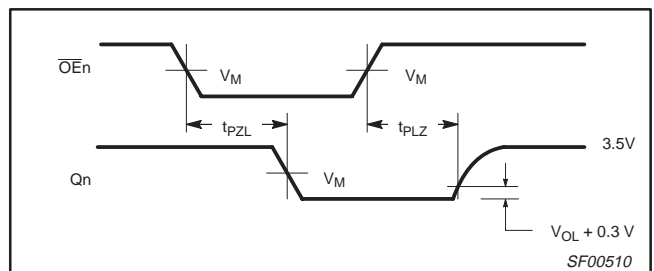
Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



Waveform 3. 3-State output enable time to HIGH level and output disable time from HIGH level



Waveform 2. Data setup time and hold times

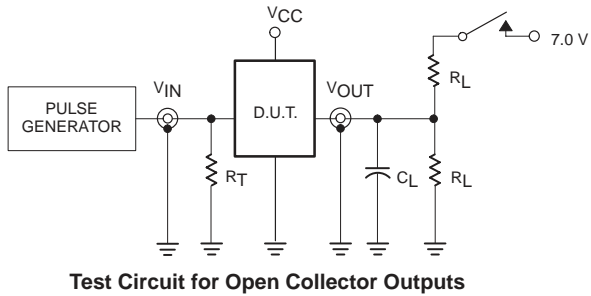


Waveform 4. 3-State output enable time to LOW level and output disable time from LOW level

10-bit bus interface register, non-inverting (3-State)

74F821

TEST CIRCUIT AND WAVEFORMS

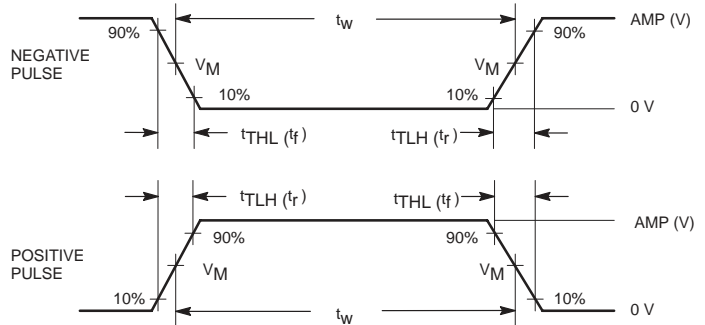


SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

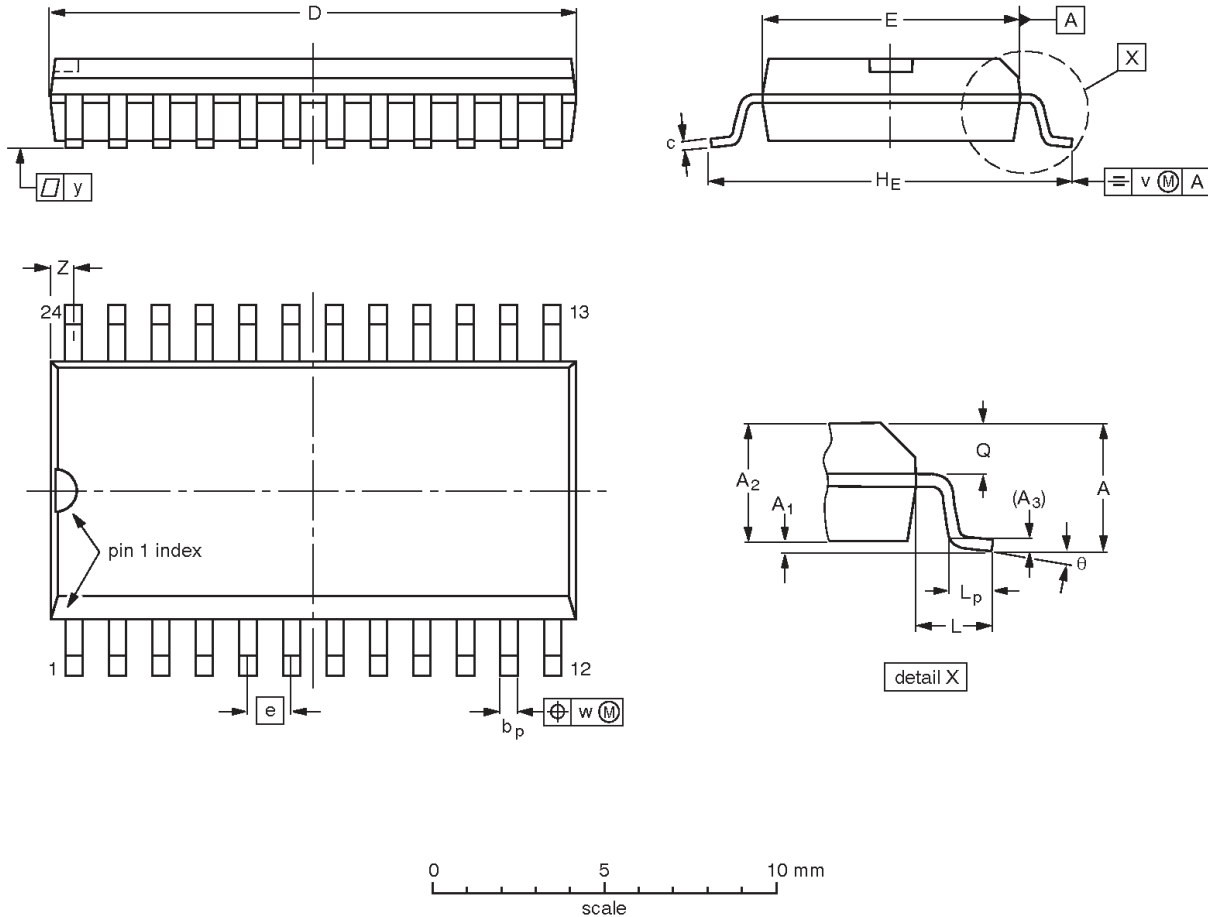
SF00128

10-bit bus interface register, non-inverting (3-State)

74F821

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

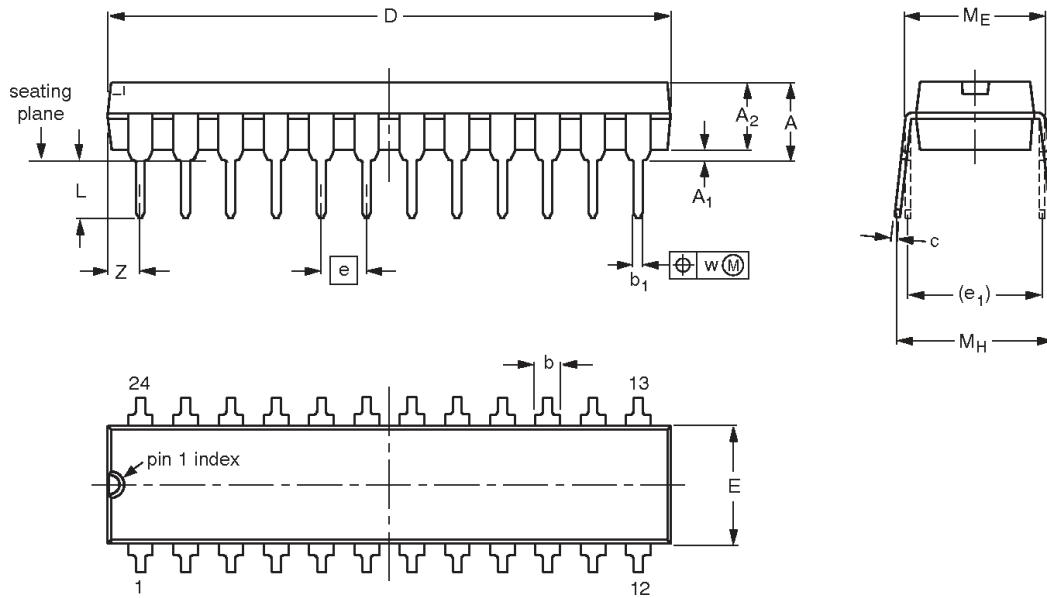
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				-99-12-27 03-02-19

10-bit bus interface register, non-inverting (3-State)

74F821

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				99-12-27 03-03-12

10-bit bus interface register, non-inverting (3-State)

74F821

REVISION HISTORY

Rev	Date	Description
_3	20040722	(74F821_3) Product data sheet (9397 750 13819). Replaces data sheet 74F821/822/823/824/825/826 of 1996 Jan 05 (9397 750 05185). Modifications: <ul style="list-style-type: none"> Remove part numbers 74F822/823/824/825/826 and references to them.
_2	19960105	(74F821–74F826_2) Product specification (9397 750 05185). ECN 853-1304 16195 of 05 January 1996.

Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data sheet	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data sheet	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

© Koninklijke Philips Electronics N.V. 2004
 All rights reserved. Printed in U.S.A.

Date of release: 07-04

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com

Document order number:

9397 750 13819

Let's make things better.