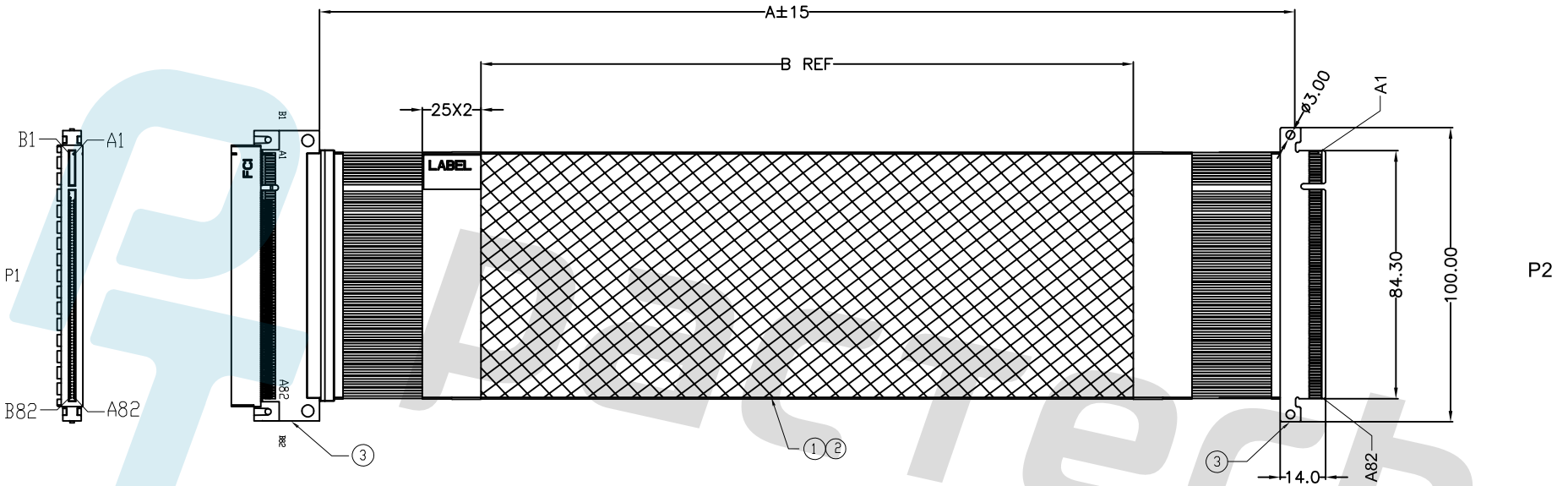
NOTICE: RoHS ✓ ALL PARTS MUST MEET TO RoHS REQUIREMENTS

REV.	DESCRIPTION	DRAWN	APPROVED	DATE
X1	NEW DRAWING	A. ZAN	Z. YING	2022.05.17

NOTE:
1. ELECTRICAL PERFORMANCE SHOULD MEET THE PCIe Gen5 STANDARD.
2. ALL SOLDERED POINTS SHALL BE COVERED WITH UV GLUE.



TABLE

ITEM	PART NO.	DIM"A"(mm)	DIM"B"(mm)
1	PC-PCIE-16X-G5-400	400	300
2	PC-PCIE-16X-G5-500	500	400
3	PC-PCIE-16X-G5-700	700	600
4	PC-PCIE-16X-G5-1000	1000	900

ITEM	DESCRIPTION	QTY
8	164 PIN PCIE X16 DUST COVER	1
7	LABEL PP 57*26mm	1
6	PCIE 16X PCB inner	A/R
5	W=55, PET	A/R
4	IPS PCI EXPRESS 5.0 SMT 16X CONNECTOR W/PCB	1
3	IPS PCI EXPRESS 5.0 16X ADD-IN CARD	1
2	30AWG DIFFERENTIAL CABLE(85Ohm)	A/R
1	30AWG ELECTRICAL CABLE(BROWN)	A/R

1. .* ±0.1
2. .** ±0.1
3. .*** ±0.05
4. FRACT. ±1/32"
5. ANGULAR ±1/2°

PART NO. PC-PCIE-16X-G5-LLL

APPROVED	Z. YING
CHECKED	Z. YING
DRAWN	A. ZAN
DATE	2022-05-17

pactech

TITLE: 164 PIN PCIe X16 Gen5 Cable Assembly

UNIT	SCALE	SHEET	REV
MM	NONE	1/2	X1

NOTICE: RoHS ALL PARTS MUST MEET TO RoHS REQUIREMENTS

WIRE DIAGRAM

P1	DESCRIPTION	REMARK	P2
B1	+12V	12 V power	B1
B2	+12V	12 V power	B2
B3	+12V	12 V power	B3
B4	GND	Ground	B4
B5	SMCLK	SMBus (System Management Bus) clock	B5
B6	SMDAT	SMBus (System Management Bus) data	B6
B7	GND	Ground	B7
B8	+3.3V	3.3 V power	B8
B9	JTAG1	TRST# (Test Reset) resets the JTAG interface	B9
B10	3.3Vaux	3.3 V auxiliary power	B10
B11	WAKE#	Signal for Link reactivation	B11
B12	RSVD	Reserved	B12
B13	GND	Ground	B13
B14	PETp0	Transmitter differential pair,	B14
B15	PETn0	Lane 0	B15
B16	GND	Ground	B16
B17	PRSNT2#	Hot-Plug presence detect	B17
B18	GND	Ground	B18
B19	PETp1	Transmitter differential pair,	B19
B20	PETn1	Lane 1	B20
B21	GND	Ground	B21
B22	GND	Ground	B22
B23	PETp2	Transmitter differential pair,	B23
B24	PETn2	Lane 2	B24
B25	GND	Ground	B25
B26	GND	Ground	B26
B27	PETp3	Transmitter differential pair,	B27
B28	PETn3	Lane 3	B28
B29	GND	Ground	B29
B30	RSVD	Reserved	B30
B31	PRSNT2#	Hot-Plug presence detect	B31
B32	GND	Ground	B32
B33	PETp4	Transmitter differential pair,	B33
B34	PETn4	Lane 4	B34
B35	GND	Ground	B35
B36	GND	Ground	B36
B37	PETp5	Transmitter differential pair,	B37
B38	PETn5	Lane 5	B38
B39	GND	Ground	B39
B40	GND	Ground	B40
B41	PETp6	Transmitter differential pair,	B41
B42	PETn6	Lane 6	B42
B43	GND	Ground	B43
B44	GND	Ground	B44
B45	PETp7	Transmitter differential pair,	B45
B46	PETn7	Lane 7	B46
B47	GND	Ground	B47
B48	PRSNT2	Hot-Plug presence detect	B48
B49	GND	Ground	B49

P1	DESCRIPTION	REMARK	P2
A1	PRSNT1#	Hot-Plug presence detect	A1
A2	+12V	12 V power	A2
A3	+12V	12 V power	A3
A4	GND	Ground	A4
A5	JTAG2	TCK (Test Clock), clock input for JTAG interface	A5
A6	JTAG3	TDI (Test Data Input)	A6
A7	JTAG4	TDO (Test Data Output)	A7
A8	JTAG5	TMS (Test Mode Select)	A8
A9	+3.3V	3.3 V power	A9
A10	+3.3V	3.3 V power	A10
A11	PERST#	Fundamental reset	A11
A12	GND	Ground	A12
A13	REFCLK+	Reference clock (differential pair)	A13
A14	REFCLK-		A14
A15	GND	Ground	A15
A16	PERp0	Receiver differential pair, Lane 0	A16
A17	PERn0		A17
A18	GND	Ground	A18
A19	RSVD		A19
A20	GND	Ground	A20
A21	PERp1	Receiver differential pair, Lane 1	A21
A22	PERn1		A22
A23	GND	Ground	A23
A24	GND	Ground	A24
A25	PERp2	Receiver differential pair, Lane 2	A25
A26	PERn2		A26
A27	GND	Ground	A27
A28	GND	Ground	A28
A29	PERp3	Receiver differential pair, Lane 3	A29
A30	PERn3		A30
A31	GND	Ground	A31
A32	RSVD	Reserved	A32
A33	RSVD	Reserved	A33
A34	GND	Ground	A34
A35	PERp4	Receiver differential pair, Lane 4	A35
A36	PERn4		A36
A37	GND	Ground	A37
A38	GND	Ground	A38
A39	PERp5	Receiver differential pair, Lane 5	A39
A40	PERn5		A40
A41	GND	Ground	A41
A42	GND	Ground	A42
A43	PERp6	Receiver differential pair, Lane 6	A43
A44	PERn6		A44
A45	GND	Ground	A45
A46	GND	Ground	A46
A47	PERp7	Receiver differential pair, Lane 7	A47
A48	PERn7		A48
A49	GND	Ground	A49

P1	DESCRIPTION	REMARK	P2
B50	PETp8	Transmitter differential pair,	B50
B51	PETn8	Lane 8	B51
B52	GND	Ground	B52
B53	GND	Ground	B53
B54	PETp9	Transmitter differential pair,	B54
B55	PETn9	Lane 9	B55
B56	GND	Ground	B56
B57	GND	Ground	B57
B58	PETp10	Transmitter differential pair,	B58
B59	PETn10	Lane 10	B59
B60	GND	Ground	B60
B61	GND	Ground	B61
B62	PETp11	Transmitter differential pair,	B62
B63	PETn11	Lane 11	B63
B64	GND	Ground	B64
B65	GND	Ground	B65
B66	PETp12	Transmitter differential pair,	B66
B67	PETn12	Lane 12	B67
B68	GND	Ground	B68
B69	GND	Ground	B69
B70	PETp13	Transmitter differential pair, Lane 13	B70
B71	PETn13		B71
B72	GND	Ground	B72
B73	GND	Ground	B73
B74	PETp14	Transmitter differential pair, Lane 14	B74
B75	PETn14		B75
B76	GND	Ground	B76
B77	GND	Ground	B77
B78	PETp15	Transmitter differential pair, Lane 15	B78
B79	PETn15		B79
B80	GND	Ground	B80
B81	PRSNT2#	Hot-Plug presence detect	B81
B82	RSVD	Reserved	B82

P1	DESCRIPTION	REMARK	P2
A50	RSVD	Reserved	A50
A51	GND	Ground	A51
A52	PERp8	Receiver differential pair, Lane 8	A52
A53	PERn8		A53
A54	GND	Ground	A54
A55	GND	Ground	A55
A56	PERp9	Receiver differential pair, Lane 9	A56
A57	PERn9		A57
A58	GND	Ground	A58
A59	GND	Ground	A59
A60	PERp10	Receiver differential pair, Lane 10	A60
A61	PERn10		A61
A62	GND	Ground	A62
A63	GND	Ground	A63
A64	PERp11	Receiver differential pair, Lane 11	A64
A65	PERn11		A65
A66	GND	Ground	A66
A67	GND	Ground	A67
A68	PERp12	Receiver differential pair, Lane 12	A68
A69	PERn12		A69
A70	GND	Ground	A70
A71	GND	Ground	A71
A72	PERp13	Receiver differential pair, Lane 13	A72
A73	PERn13		A73
A74	GND	Ground	A74
A75	GND	Ground	A75
A76	PERp14	Receiver differential pair, Lane 14	A76
A77	PERn14		A77
A78	GND	Ground	A78
A79	GND	Ground	A79
A80	PERp15	Receiver differential pair, Lane 15	A80
A81	PERn15		A81
A82	GND	Ground	A82

1. .* ±0.1
2. .** ±0.1
3. .*** ±0.05
4. FRACT. ±1/32”
5. ANGULAR ±1/2°

PART NO. PC-PCIE-16X-G5-XXXX

APPROVED	Z. YING
CHECKED	Z. YING
DRAWN	A. ZAN
DATE	2022-05-17

pactech

TITLE: 164 PIN PCIe X16 Gen5 Cable Assembly

UNIT	SCALE	SHEET	REV
MM	NONE	2/2	X1