# 16-bit Proprietary Microcontroller

**CMOS**

# F²MC-16LX MB90800 Series

# MB90802/802S/803/803S/F804/V800

## ■ DESCRIPTION

The MB90800 series is a general-purpose 16-bit microcontroller that has been developed for high-speed real-time processing required for industrial and office automation equipment and process control, etc. The LCD controller of 48 segment four common is built into.

Instruction set has taken over the same AT architecture as in the F²MC-8L and F²MC-16L, and is further enhanced to support high level languages, extend addressing mode, enhanced divide/multiply instructions with sign and enrichment of bit processing. In addition, long word processing is now available by introducing a 32-bit accumulator.

## ■ FEATURES

- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Operating clock (PLL clock) : divided-by-2 of oscillation (at oscillation of 6.25 MHz) or
    1 to 4 times the oscillation (at oscillation of 6.25 MHz to 25 MHz).
  - Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock, operation at Vcc = 3.3 V)
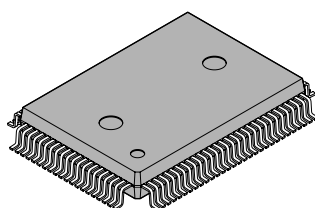
- **The maximum memory space:16 MB**
  - 24-bit internal addressing
  - Bank addressing

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## ■ PACKAGE

100-pin plastic QFP

(FPT-100P-M06)

FUJITSU

*(Continued)*

- **Optimized instruction set for controller applications**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - High code efficiency
  - Enhanced high-precision computing with 32-bit accumulator
  - Enhanced Multiply/Divide instructions with sign and the RETI instruction

- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Instruction set has symmetry and barrel shift instructions

- **Program Patch Function (2 address pointer)**

- **4-byte instruction queue**

- **Interrupt function**
  - The priority level can be set to programmable.
  - Interrupt function with 32 factors

- **Data transfer function**
  - Expanded intelligent I/O service function (EI$^2$OS): Maximum of 16 channels

- **Low Power Consumption Mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Time-base timer mode (a mode that operates oscillation clock and time-base timer)
  - Watch mode (mode in which only the subclock and watch timers operate)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU blocking mode (operating CPU at each set cycle)

- **Package**
  - QFP-100 (FPT-100P-M06:0.65 mm pin pitch)

- **Process : CMOS technology**

## ■ PRODUCT LINEUP

| Part number | | MB90V800 | MB90F804-101/201 | MB90802/S | MB90803/S |
|---|---|---|---|---|---|
| Type | | Evaluation product | FLASH MEMORY products | Mask ROM products | |
| System clock | | On-chip PLL clock multiplication method( $\times$ 1, $\times$ 2, $\times$ 3, $\times$ 4, 1/2 when PLL stops) Minimum instruction execution time of 40.0 ns (at oscillation of 6.25 MHz, four times the PLL clock) | | | |
| ROM capacity | | No | 256 KB | 128 KB | |
| RAM capacity | | 28 KB | 16 KB | 2 KB | 4 KB |
| CPU functions | | Number of basic instructions : 351<br>Minimum instruction execution time : 40.0 ns/6.25 MHz oscillator<br>(When four times is used : machine clock 25 MHz, Power supply voltage : 3.3 V $\pm$ 0.3 V)<br>Addressing type : 23 types<br>Program Patch Function : 2 address pointers<br>The maximum memory space : 16MB | | | |
| Ports | | I/O port (CMOS) 68 ports (shared with resources), (70 ports when the subclock is not used) | | | |
| LCD controller/driver | | Segment driver that can drive the LCD panel (liquid crystal display) directly, and common driver 48 SEG $\times$ 4 COM | | | |
| 16-bit input/ output timer | 16-bit free-run timer | 1 channel<br>Overflow interrupt | | | |
| | Output compare (OCU) | 2 channels<br>Pin input factor: matching of the compare register | | | |
| | Input capture (ICU) | 2 channels<br>Rewriting a register value upon a pin input (rising edge, falling edge, or both edges) | | | |
| 16-bit Reload Timer | | 16-bit reload timer operation (toggle output, single shot output selectable)<br>The event count function is optional. The event count function is optional.<br>Three channels are built in. | | | |
| 16-bit PPG timer | | Output pin $\times$ 2 ports<br>Operating clock frequency : fcp, fcp/22, fcp/24, fcp/26<br>Two channels are built in. | | | |
| Timebase timer | | 1 channel | | | |
| Watchdog timer | | 1 channel | | | |
| Timer clock output circuit | | Clock with a frequency of external input clock divided by 16/32/64/128 can be output externally. | | | |
| I$^2$C bus | | I$^2$C Interface. 1 channel is built-in. | | | |
| 8/10-bit A/D converter | | 12 channels (input multiplex)<br>The 8-bit resolution or 10-bit resolution can be set.<br>Conversion time : 5.9 $\mu$s (When machine clock 16.8 MHz works). | | | |
| UART | | Full-duplex double buffer<br>Asynchronous/synchronous transmit (with start/stop bits) are supported.<br>Two channels are built in. | | | |
| Extended I/O serial interface | | Two channels are built in. | | | |
| Interrupt delay interrupt | | Four channel independence (A/D input and using combinedly)<br>Interrupt causes : "L"→"H" edge/"H"→"L" edge/"L" level/"H" level selectable | | | |

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*(Continued)*

| Part number | MB90V800 | MB90F804-101/201 | MB90803/S |
|---|---|---|---|
| DTP/External interrupt | 8 channels (The 8 channels include with the shared A/D input) Interrupt causes : "L"→"H" edge/"H"→"L" edge/"L" level/"H" level selectable | | |
| Low Power Consumption Mode | Sleep mode/Time-base timer mode/Watch mode/Stop mode/CPU intermittent mode | | |
| Process | CMOS | | |
| Operating voltage | 2.7 V to 3.6 V | | |

## ■ PIN ASSIGNMENT

(TOP VIEW)

Top pins (100–81):
P23/SEG31 (100), P22/SEG30 (99), P21/SEG29 (98), P20/SEG28 (97), P17/SEG27 (96), P16/SEG26 (95), P15/SEG25 (94), X0 (93), X1 (92), Vss (91), Vcc (90), P14/SEG24 (89), P13/SEG23 (88), P12/SEG22 (87), P11/SEG21 (86), P10/SEG20 (85), P07/SEG19 (84), P06/SEG18 (83), P05/SEG17 (82), P04/SEG16 (81)

Left pins (1–30):
| Pin | Name |
|---|---|
| 1 | P24/SEG32 |
| 2 | P25/SEG33 |
| 3 | P26/SEG34 |
| 4 | P27/SEG35 |
| 5 | P30/SEG36/SO3 |
| 6 | P31/SEG37/SC3 |
| 7 | P32/SEG38/SI3 |
| 8 | P33/SEG39/TMCK |
| 9 | P34/SEG40/IC0 |
| 10 | P35/SEG41/IC1 |
| 11 | P36/SEG42/OCU0 |
| 12 | P37SEG43/OCU1 |
| 13 | X0A/P90 |
| 14 | X1A/P91 |
| 15 | Vcc |
| 16 | Vss |
| 17 | P40/LED0 |
| 18 | P41/LED1 |
| 19 | P42/LED2 |
| 20 | P43/LED3 |
| 21 | P44/LED4 |
| 22 | P45/LED5/TOT0 |
| 23 | P46/LED6/TOT1 |
| 24 | P47/LED7/TOT2 |
| 25 | P50/SEG44/TIN0 |
| 26 | P51/SEG45/TIN1 |
| 27 | P52/SEG46/TIN2/PPG0 |
| 28 | P53/SEG47/PPG1 |
| 29 | P54/SI0 |
| 30 | P55/SC0 |

Right pins (80–51):
| Pin | Name |
|---|---|
| 80 | P03/SEG15 |
| 79 | P02/SEG14 |
| 78 | P01/SEG13 |
| 77 | P00/SEG12 |
| 76 | SEG11 |
| 75 | SEG10 |
| 74 | SEG9 |
| 73 | SEG8 |
| 72 | SEG7 |
| 71 | SEG6 |
| 70 | SEG5 |
| 69 | SEG4 |
| 68 | SEG3 |
| 67 | SEG2 |
| 66 | Vss |
| 65 | Vcc |
| 64 | SEG1 |
| 63 | SEG0 |
| 62 | P84/COM3 |
| 61 | P83/COM2 |
| 60 | COM1 |
| 59 | COM0 |
| 58 | V3 |
| 57 | V2/P82 |
| 56 | V1/P81 |
| 55 | V0/P80 |
| 54 | RST |
| 53 | MD0 |
| 52 | MD1 |
| 51 | MD2 |

Bottom pins (31–50):
P56/SO0 (31), AVcc (32), P57/SI1 (33), P76 (34), AVss (35), P60/AN0 (36), P61/AN1 (37), P62/AN2 (38), P63/AN3 (39), P64/AN4 (40), P65/AN5/INT0 (41), P66/AN6/INT1 (42), P67/AN7/INT2 (43), Vss (44), P70/AN8/INT3 (45), P71/AN9/SC1 (46), P72/AN10/SO1 (47), P73/AN11/SI2 (48), P74/SDA/SC2 (49), P75/SCL/SO2 (50)

(FPT-100P-M06)

# MB90800 Series

## ■ PIN DESCRIPTION

| Pin No. | Pin Name | I/O Circuit Type* | Status/function at reset | Function |
|---|---|---|---|---|
| 92, 93 | X0, X1 | A | Oscillation status | It is a terminal which connects the oscillator.<br>When connecting an external clock, leave the x1 pin unconnected. |
| 13, 14 | X0A, X1A | B | Oscillation status | It is 32 kHz oscillation pin.<br>(Dual-line model) |
| | P90, P91 | G | Port input (High-Z) | General purpose input/output port.<br>(Single-line model) |
| 51 | MD2 | M | Mode Pins | Input pin for selecting operation mode.<br>Connect directly to Vss. |
| 52, 53 | MD1, MD0 | L | Mode Pins | Input pin for selecting operation mode.<br>Connect directly to Vcc. |
| 54 | RST | K | Reset input | External reset input pin. |
| 63, 64, 67 to 76 | SEG0 to SEG11 | D | LCD SEG output | A segment output terminal of the LCD controller/driver. |
| 77 to 84 | SEG12 to SEG19 | E | Port input (High-Z) | A segment output terminal of the LCD controller/driver. |
| | P00 to P07 | | | General purpose input/output port. |
| 85 to 89, 94 to 96 | SEG20 to SEG27 | E | Port input (High-Z) | A segment output terminal of the LCD controller/driver. |
| | P10 to P17 | | | General purpose input/output port. |
| 97 to 100, 1 to 4 | SEG28 to SEG35 | E | Port input (High-Z) | A segment output terminal of the LCD controller/driver. |
| | P20 to P27 | | | General purpose input/output port. |
| 5 | SEG36 | E | Port input (High-Z) | A segment output terminal of the LCD controller/driver. |
| | P30 | | | General purpose input/output port. |
| | SO3 | | | Serial data output pin of serial I/O ch.3.<br>Valid when serial data output of serial I/O ch.3 is enabled. |
| 6 | SEG37 | E | Port input (High-Z) | A segment output terminal of the LCD controller/driver. |
| | P31 | | | General purpose input/output port. |
| | SC3 | | | Serial clock I/O pin of serial I/O ch.3.<br>Valid when serial clock output of serial I/O ch.3 is enabled. |

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| Pin No. | Pin Name | I/O Circuit Type* | Status/function at reset | Function |
|---|---|---|---|---|
| 7 | SEG38 | E | | A segment output terminal of the LCD controller/driver. |
| | P32 | | | General purpose input/output port. |
| | SI3 | | | Serial data input pin of serial I/O ch.3.<br>This pin may be used during serial I/O ch.3 in input mode, so it cannot use as other pin function. |
| 8 | SEG39 | E | | A segment output terminal of the LCD controller/driver. |
| | P33 | | | General purpose input/output port. |
| | TMCK | | | Timer clock output pin.<br>It is effective when permitting the power output. |
| 9, 10 | SEG40, SEG41 | E | | A segment output terminal of the LCD controller/driver. |
| | P34, P35 | | | General purpose input/output port. |
| | IC0, IC1 | | | External trigger input pin of input capture ch.0/ch.1. |
| 11, 12 | SEG42, SEG43 | E | Port input (High-Z) | A segment output terminal of the LCD controller/driver. |
| | P36, P37 | | | General purpose input/output port. |
| | OCU0, OCU1 | | | Output terminal for the Output Compares. |
| 17 to 21 | LED0 to LED4 | F | | It is a output terminal for LED ($I_{OL}$ = 15 mA). |
| | P40 to P44 | | | General purpose input/output port. |
| 22 to 24 | LED5 to LED7 | F | | It is a output terminal for LED ($I_{OL}$ = 15 mA). |
| | P45 to P47 | | | General purpose input/output port. |
| | TOT0 to TOT2 | | | External event output pin of reload timer ch.0 to ch.2.<br>It is effective when permitting the external event output. |
| 25, 26 | SEG44, SEG45 | E | | A segment output terminal of the LCD controller/driver. |
| | P50, P51 | | | General purpose input/output port. |
| | TIN0, TIN1 | | | External clock input pin of reload timer ch.0, ch.1.<br>It is effective when permitting the external clock input. |

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| Pin No. | Pin Name | I/O Circuit Type* | Status/function at reset | Function |
|---|---|---|---|---|
| 27 | SEG46 | E | Port input (High-Z) | A segment output terminal of the LCD controller/driver. |
| | P52 | | | General purpose input/output port. |
| | TIN2 | | | External clock input pin of reload timer ch.2. It is effective when permitting the external clock input. |
| | PPG0 | | | PPG timer (ch.0) output pin. |
| 28 | SEG47 | E | | A segment output terminal of the LCD controller/driver. |
| | P53 | | | General purpose input/output port. |
| | PPG1 | | | PPG (ch.1) timer output pin. |
| 29 | SIO | G | | Serial data input pin of UART ch.0. This pin may be used during UART ch.0 in receiving mode, so it cannot use as other pin function. |
| | P54 | | | General purpose input/output port. |
| 30 | SC0 | G | | Serial clock input/output pin of UART ch.0. It is effective when permitting the serial clock output of UART ch.0. |
| | P55 | | | General purpose input/output port. |
| 31 | SO0 | G | | Serial data output pin of UART ch.0. It is effective when permitting the serial clock output of UART ch.0. |
| | P56 | | | General purpose input/output port. |
| 33 | SI1 | G | | Serial data input pin of UART ch.1. This pin may be used during UART ch.1 in receiving mode, so it cannot use as other pin function. |
| | P57 | | | General purpose input/output port. |
| 34 | P76 | G | | General purpose input/output port. |
| 36 to 40 | AN0 to AN4 | I | | Analog input pin ch.0 to ch.4 of A/D converter. Enabled when analog input setting is " enabled "(set by ADER). |
| | P60 to P64 | | | General purpose input/output port. |

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| Pin No. | Pin Name | I/O Circuit Type* | Status/function at reset | Function |
|---|---|---|---|---|
| 41 to 43 | AN5 to AN7 | I | Analog input (High-Z) | Analog input pin ch.5 to ch.7 of A/D converter. Enabled when analog input setting is " enabled ". |
| | P65 to P67 | | | General purpose input/output port. |
| | INT0 to INT2 | | | Functions as an external interrupt ch.0 to ch.2 input pin. |
| 45 | AN8 | I | | Analog input pin ch.8 of A/D converter. Enabled when analog input setting is " enabled ". |
| | P70 | | | General purpose input/output port. |
| | INT3 | | | Functions as an external interrupt ch.3 input pin. |
| 46 | AN9 | I | Port input (High-Z) | Analog input pin ch.9 of A/D converter. Enabled when analog input setting is " enabled ". |
| | P71 | | | General purpose input/output port. |
| | SC1 | | | Serial clock input/output pin of UART ch.1. It is effective when permitting the serial clock output of UART ch.1. |
| 47 | AN10 | I | | Analog input pin ch.10 of A/D converter. Enabled when analog input setting is " enabled ". |
| | P72 | | | General purpose input/output port. |
| | SO1 | | | Serial data output pin of serial I/O ch.1. Valid when serial data output of serial I/O ch.1 is enabled. |
| 48 | AN11 | I | | Analog input pin ch.11 of A/D converter. Enabled when analog input setting is " enabled ". |
| | P73 | | | General purpose input/output port. |
| | SI2 | | | Serial data input pin of serial I/O ch.2. This pin may be used during serial I/O ch.2 in input mode, so it cannot use as other pin function. |

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| Pin No. | Pin Name | I/O Circuit Type* | Status/function at reset | Function |
|---------|----------|-------------------|--------------------------|----------|
| 49 | SDA | H | Port input (High-Z) | Data input/output pin of I$^2$C Interface.<br>This pin is enabled when the I$^2$C interface is operated.<br>While the I$^2$C interface is running, the port must be set for input use. |
|  | P74 |  |  | General purpose input/output port.<br>(N-ch open-drain, withstand voltage of 5 V.) |
|  | SC2 |  |  | Serial clock input pin of serial I/O ch.2.<br>Valid when serial clock output of serial I/O ch.2 is enabled. |
| 50 | SCL | H |  | Clock input/output pin of I$^2$C Interface.<br>This pin is enabled when the I$^2$C interface is operated.<br>While the I$^2$C interface is running, the port must be set for input use. |
|  | P75 |  |  | General purpose input/output port.<br>(N-ch open-drain, withstand voltage of 5 V.) |
|  | SO2 |  |  | Serial data output pin of serial I/O ch.2.<br>Valid when serial data output of serial I/O ch.2 is enabled. |
| 55 to 57 | V0 to V2 | J | LCD drive power supply input | LCD controller/driver.<br>Reference power terminals of LCD controller/driver. |
|  | P80 to P82 |  |  | General purpose input/output port. |
| 59, 60 | COM0, COM1 | D | LCD COM output | A common output terminal of the LCD controller/driver. |
| 61, 62 | P83, P84 | E | Port input (High-Z) | General purpose input/output port. |
|  | COM2, COM3 |  |  | A common output terminal of the LCD controller/driver. |
| 32 | AV$_{CC}$ | C | Power supply | A/D converter exclusive power supply input pin. |
| 35 | AV$_{SS}$ | C |  | A/D converter-exclusive GND power supply pin. |
| 58 | V3 | J |  | LCD controller/driver<br>Reference power terminals of LCD controller/driver. |
| 15, 65, 90 | V$_{CC}$ | — |  | These are power supply input pins. |
| 16, 44, 66, 91 | V$_{SS}$ | — |  | GND power supply pin. |

* : Refer to "■ I/O CIRCUIT TYPE" for I/O circuit type.

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A | X1 / P-ch N-ch / X0 — Clock input / Standby control signal | Oscillation feedback resistance : 1 MΩ approx. |
| B | X1A / P-ch N-ch / X0A — Clock input / Standby control signal | Low-rate oscillation feedback resistor, approx.10 MΩ |
| C | P-ch / N-ch — AVP | Analog power supply input protection circuit |
| D | P-ch / N-ch — R — LCDC output | LCDC output |
| E | P-ch / N-ch / R — LCDC output / R — Input signal / Standby control signal | • CMOS output<br>• LCDC output<br>• Hysteresis input (With input interception function at standby) |
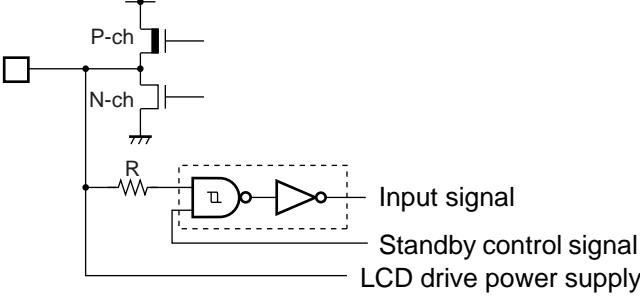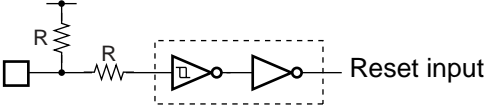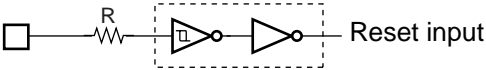
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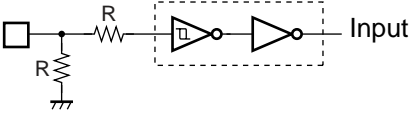| Type | Circuit | Remarks |
|------|---------|---------|
| F | P-ch<br>N-ch<br>R<br>Input signal<br>Standby control signal | • CMOS output<br>  (Heavy-current $I_{OL}$ =15 mA for LED drive)<br>• Hysteresis input<br>  (With input interception function at standby) |
| G | P-ch<br>N-ch<br>R<br>Input signal<br>Standby control signal | • CMOS output<br>• CMOS hysteresis input<br>  (With input interception function at standby)<br><br>Notes : • The I/O port and internal resources share one output buffer for their outputs.<br> • The I/O port and internal resources share one input buffer for their input. |
| H | N-ch   Nout<br>R<br>Input signal<br>Standby control signal | • Hysteresis input<br>  (With input interception function at standby)<br>• N-ch open drain output |
| I | P-ch<br>N-ch<br>R<br>Input signal<br>Standby control signal<br>A/D converter<br>Analog input | • CMOS output<br>• CMOS hysteresis input<br>  (With input interception function at standby)<br>• Analog input<br>  (If the bit of analog input enable register = 1, the analog input of A/D converter is enabled.)<br><br>Notes : • The I/O port and internal resources share one output buffer for their outputs.<br> • The I/O port and internal resources share one input buffer for their input. |

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| Type | Circuit | Remarks |
|---|---|---|
| J |  | • CMOS output<br>• CMOS hysteresis input<br>(With input interception function at standby)<br>• LCD drive power supply input |
| K |  | CMOS hysteresis input with pull-up resistor. |
| L |  | CMOS hysteresis input |
| M |  | CMOS hysteresis input with pull-down resistor |

## ■ HANDLING DEVICES

### 1. Preventing Latch-up, Turning on Power Supply

Latch-up may occur on CMOS IC under the following conditions:

• If a voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input and output pins,

• A voltage higher than the rated voltage is applied between $V_{CC}$ pin and $V_{SS}$ pin.

• If the $AV_{CC}$ power supply is turned on before the $V_{CC}$ voltage.

Ensure that you apply a voltage to the analog power supply at the same time as $V_{CC}$ or after you turn on the digital power supply (when you perform power-off, turn off the analog power supply first or at the same time as $V_{CC}$ and the digital power supply).

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using CMOS IC, take great care to prevent the occurrence of latch-up.

### 2. Treatment of unused pins

If unused input pins are left open, they may cause abnormal operation or latch-up which may lead to permanent damage to the semiconductor. Any such pins should be pulled up or pulled down through resistance of at least 2 kΩ.

Any unused input/output pins should be left open in output status, or if found set to input status, they should be treated in the same way as input pins.
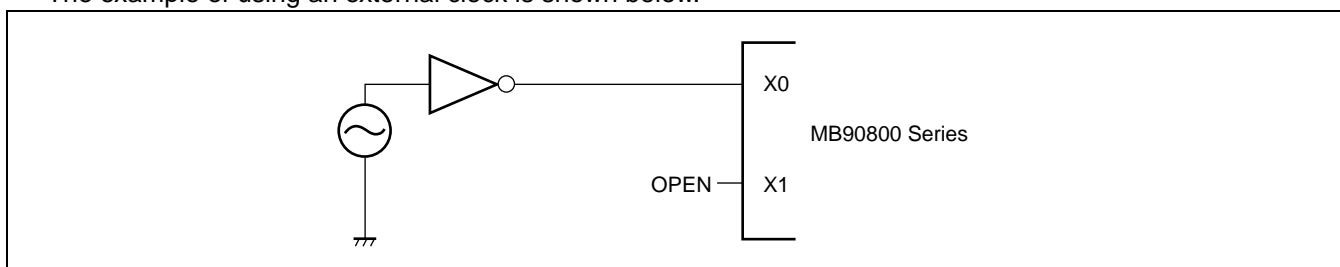
Any unused output pins should be left open.

### 3. Treatment of A/D converter power supply pins

Even if the A/D converter is not used, pins should be connected so that $AV_{CC} = V_{CC}$, and $AV_{SS} = V_{SS}$.

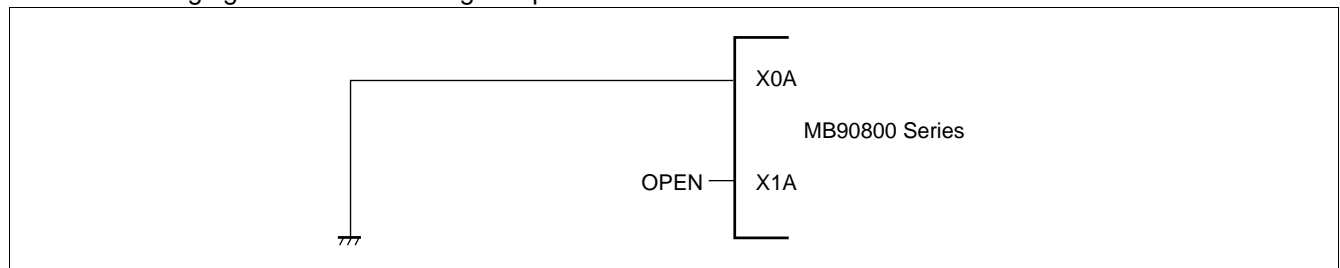### 4. About the attention when the external clock is used

In using an external clock, drive pin X0 only and leave pin X1 open.
The example of using an external clock is shown below.



Please set X0A = GND and X1A = open without subclock mode.
The following figure shows the using sample.

## 5.  Treatment of power supply pins ($V_{CC}/V_{SS}$)

In products with multiple $V_{CC}$ or $V_{SS}$ pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect all power supply pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the $V_{CC}$ and $V_{SS}$ pins of this device at the low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 $\mu$F as a bypass capacitor between $V_{CC}$ and $V_{SS}$ near this device.

## 6.  About Crystal oscillators circuit

Noise near the X0/X1 pins and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1 pins and X0A/X1A pins, the crystal oscillator (or the ceramic oscillator) and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0/X1 pins and X0A/X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

## 7.  Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.

## 8.  Stabilization of Supply Power Supply

A sudden change in the supply voltage may cause the device to malfunction even within the $V_{CC}$ supply voltage operating range.Therefore, the $V_{CC}$ supply voltage should be stabilized. For reference, the supply voltage should be controlled so that $V_{CC}$ ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard $V_{CC}$ supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

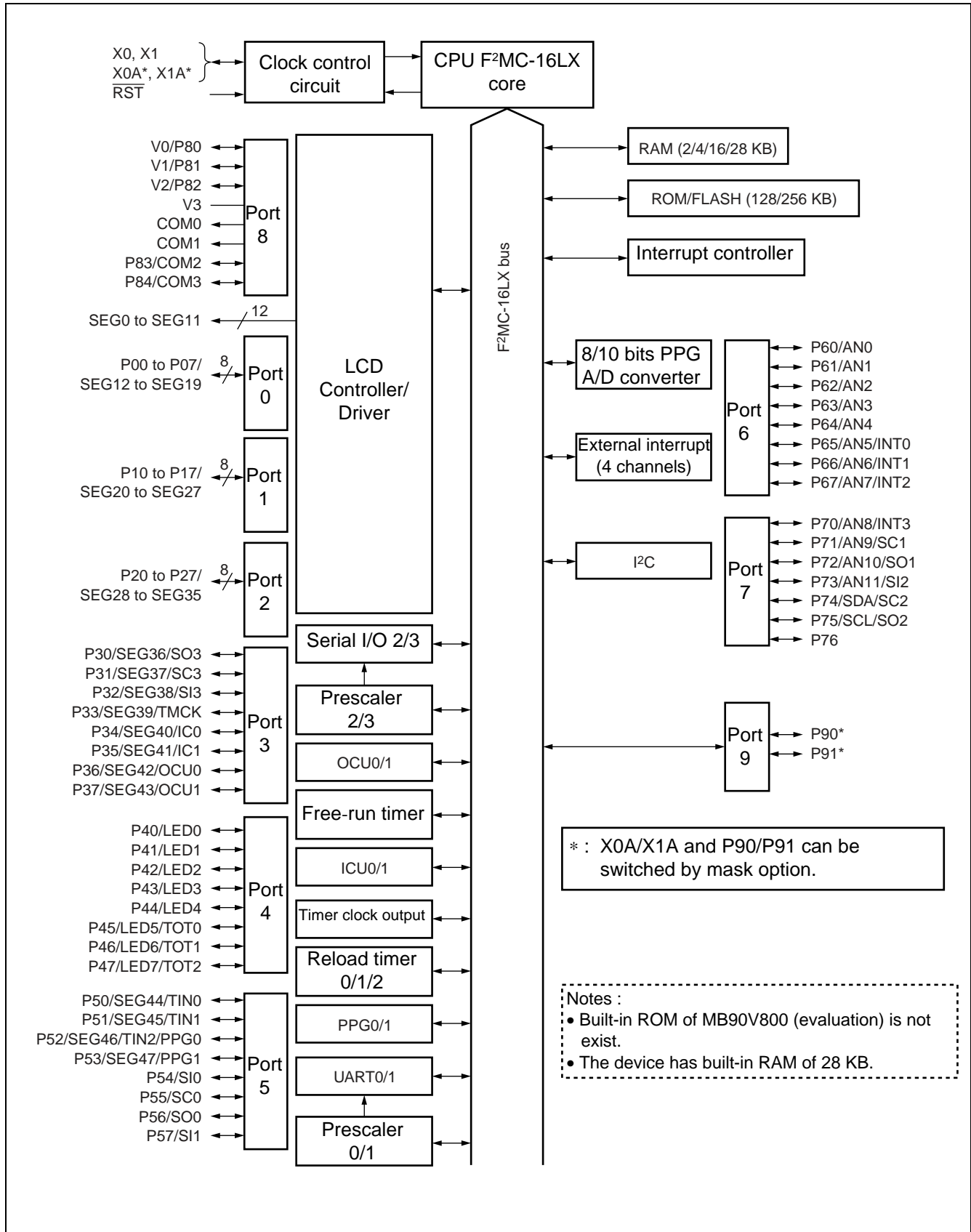## 9.  Note on Using the two-subsystem product as one-subsystem product

If you are using only one subsystem of the MB90800 series that come in one two-subsystem product, use it with X0A = $V_{SS}$ and X1A = OPEN.

## 10.  Write to FLASH

Ensure that you must write to FLASH at the operating voltage $V_{CC} = 3.0$ V to 3.6 V.

# MB90800 Series

## ■ BLOCK DIAGRAM

X0, X1
X0A*, X1A*
$\overline{RST}$

Clock control circuit

CPU F$^2$MC-16LX core

RAM (2/4/16/28 KB)

ROM/FLASH (128/256 KB)

Interrupt controller

F$^2$MC-16LX bus

V0/P80
V1/P81
V2/P82
V3
COM0
COM1
P83/COM2
P84/COM3

Port 8

SEG0 to SEG11 /12

LCD Controller/ Driver

P00 to P07/ SEG12 to SEG19 — 8 — Port 0

P10 to P17/ SEG20 to SEG27 — 8 — Port 1

P20 to P27/ SEG28 to SEG35 — 8 — Port 2

P30/SEG36/SO3
P31/SEG37/SC3
P32/SEG38/SI3
P33/SEG39/TMCK
P34/SEG40/IC0
P35/SEG41/IC1
P36/SEG42/OCU0
P37/SEG43/OCU1

Port 3

Serial I/O 2/3

Prescaler 2/3

OCU0/1

Free-run timer

P40/LED0
P41/LED1
P42/LED2
P43/LED3
P44/LED4
P45/LED5/TOT0
P46/LED6/TOT1
P47/LED7/TOT2

Port 4

ICU0/1

Timer clock output

Reload timer 0/1/2

P50/SEG44/TIN0
P51/SEG45/TIN1
P52/SEG46/TIN2/PPG0
P53/SEG47/PPG1
P54/SI0
P55/SC0
P56/SO0
P57/SI1

Port 5

PPG0/1

UART0/1

Prescaler 0/1

8/10 bits PPG A/D converter

External interrupt (4 channels)

I$^2$C

Port 6
- P60/AN0
- P61/AN1
- P62/AN2
- P63/AN3
- P64/AN4
- P65/AN5/INT0
- P66/AN6/INT1
- P67/AN7/INT2

Port 7
- P70/AN8/INT3
- P71/AN9/SC1
- P72/AN10/SO1
- P73/AN11/SI2
- P74/SDA/SC2
- P75/SCL/SO2
- P76

Port 9
- P90*
- P91*

∗ : X0A/X1A and P90/P91 can be switched by mask option.

Notes :
- Built-in ROM of MB90V800 (evaluation) is not exist.
- The device has built-in RAM of 28 KB.

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# ■ MEMORY MAP

ROM mirror function

FFFFFFH

ROM area

Address #2

00FFFFH

ROM mirror area

008000H

007917H

Extended I/O area 2

007900H

Address #2

RAM area

Register

000100H

0000CFH
0000C0H

Extended I/O area 1

0000BFH

I/O area

000000H

| Part number | Address #1 | Address #2 |
|---|---|---|
| MB90802 | 0008FFH | FE0000H |
| MB90803 | 0010FFH | FE0000H |
| MB90F804 | 0040FFH | FC0000H |
| MB90V800 | 0070FFH | F80000H* |

* : ROM is not built into MB90V800.
    F80000H is ROM decipherment region on the tool side.

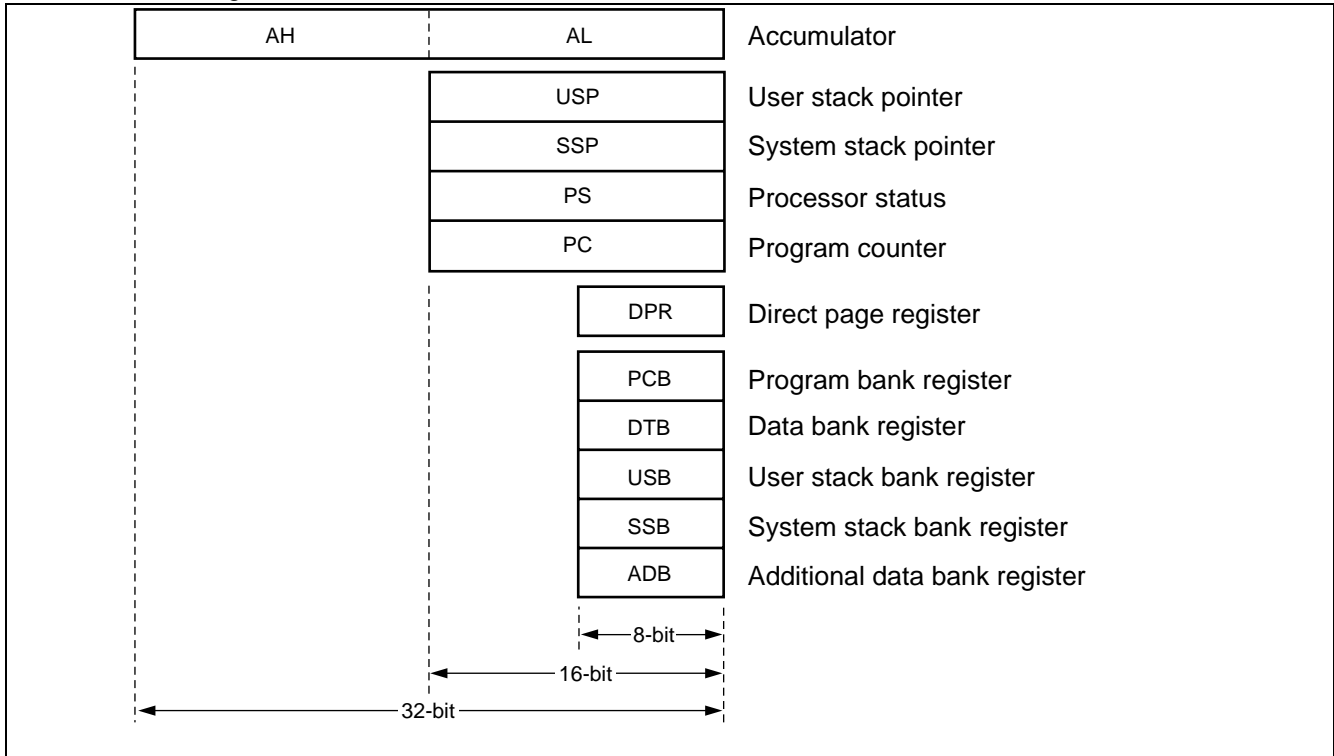Memory Map of MB90800 Series

Notes :  • When the ROM mirror function register has been set, the mirror image data at higher addresses
    ( "FF4000H to FFFFFFH" ) of bank FF is visible from the higher addresses ( " 008000H to 00FFFFH " ) of
    bank 00.
  • The ROM mirror function is for using the C compiler small model.
  • The lower 16-bit addresses of bank FF are equivalent to those of bank 00. Note that because the ROM
    area of bank FF exceeds
    32 KB, all data in the ROM area cannot be shown in mirror image in bank 00.
  • When the C compiler small model is used, the data table can be shown as mirror image at " 008000H to
    00FFFFH " by storing the data table at " FF8000H to FFFFFFH. Therefore, data tables in the ROM area
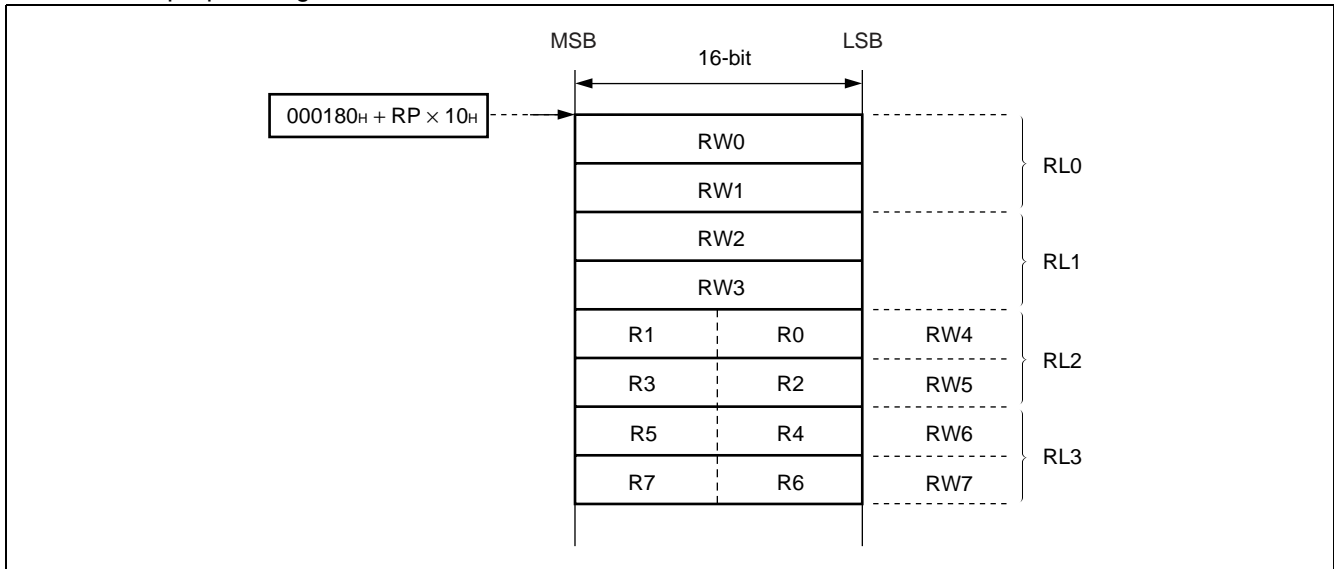    can be referenced without declaring the far addressing with the pointer.

## ■ F2MC-16L CPU Programming model

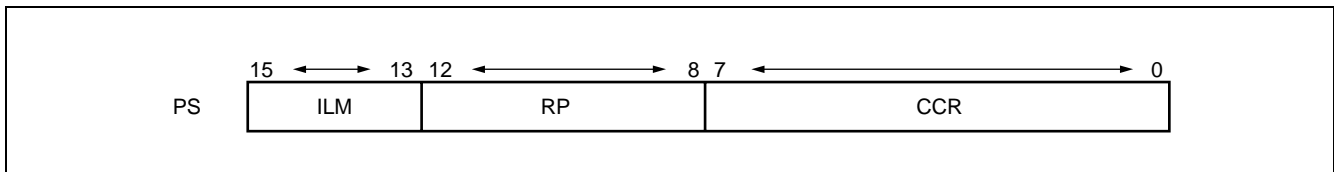• Dedicated Registers

| AH | AL | Accumulator |

| | USP | User stack pointer |
| | SSP | System stack pointer |
| | PS | Processor status |
| | PC | Program counter |

| | DPR | Direct page register |

| | PCB | Program bank register |
| | DTB | Data bank register |
| | USB | User stack bank register |
| | SSB | System stack bank register |
| | ADB | Additional data bank register |

8-bit
16-bit
32-bit

• General purpose registers

MSB    16-bit    LSB

$000180_H + RP \times 10_H$

| RW0 | RL0 |
| RW1 | |
| RW2 | RL1 |
| RW3 | |
| R1 / R0 — RW4 | RL2 |
| R3 / R2 — RW5 | |
| R5 / R4 — RW6 | RL3 |
| R7 / R6 — RW7 | |

• Processor status

15 ↔ 13 12 ↔ 8 7 ↔ 0

| PS | ILM | RP | CCR |

## ■ I/O MAP

| Address | Register abbreviation | Register | Read/Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 000000$_H$ | PDR0 | Port 0 data register | R/W | Port 0 | XXXXXXXX$_B$ |
| 000001$_H$ | PDR1 | Port 1 data register | R/W | Port 1 | XXXXXXXX$_B$ |
| 000002$_H$ | PDR2 | Port 2 data register | R/W | Port 2 | XXXXXXXX$_B$ |
| 000003$_H$ | PDR3 | Port 3 data register | R/W | Port 3 | XXXXXXXX$_B$ |
| 000004$_H$ | PDR4 | Port 4 data register | R/W | Port 4 | XXXXXXXX$_B$ |
| 000005$_H$ | PDR5 | Port 5 data register | R/W | Port 5 | XXXXXXXX$_B$ |
| 000006$_H$ | PDR6 | Port 6 data register | R/W | Port 6 | XXXXXXXX$_B$ |
| 000007$_H$ | PDR7 | Port 7 data register | R/W | Port 7 | - XXXXXXX$_B$ |
| 000008$_H$ | PDR8 | Port 8 data register | R/W | Port 8 | - - - XXXXX$_B$ |
| 000009$_H$ | PDR9 | Port 9 data register | R/W | Port 9 | - - - - - - XX$_B$ |
| 00000A$_H$ to 00000F$_H$ | | Prohibited | | | |
| 000010$_H$ | DDR0 | Port 0 direction register | R/W | Port 0 | 0 0 0 0 0 0 0 0$_B$ |
| 000011$_H$ | DDR1 | Port 1 direction register | R/W | Port 1 | 0 0 0 0 0 0 0 0$_B$ |
| 000012$_H$ | DDR2 | Port 2 direction register | R/W | Port 2 | 0 0 0 0 0 0 0 0$_B$ |
| 000013$_H$ | DDR3 | Port 3 direction register | R/W | Port 3 | 0 0 0 0 0 0 0 0$_B$ |
| 000014$_H$ | DDR4 | Port 4 direction register | R/W | Port 4 | 0 0 0 0 0 0 0 0$_B$ |
| 000015$_H$ | DDR5 | Port 5 direction register | R/W | Port 5 | 0 0 0 0 0 0 0 0$_B$ |
| 000016$_H$ | DDR6 | Port 6 direction register | R/W | Port 6 | 0 0 0 0 0 0 0 0$_B$ |
| 000017$_H$ | DDR7 | Port 7 direction register | R/W | Port 7 | - 0 0 0 0 0 0 0$_B$ |
| 000018$_H$ | DDR8 | Port 8 direction register | R/W | Port 8 | - - - 0 0 0 0 0$_B$ |
| 000019$_H$ | DDR9 | Port 9 direction register | R/W | Port 9 | - - - - - - 0 0$_B$ |
| 00001A$_H$ to 00001D$_H$ | | Prohibited | | | |
| 00001E$_H$ | ADER0 | Analog input enable 0 | R/W | Port 6, A/D | 1 1 1 1 1 1 1 1$_B$ |
| 00001F$_H$ | ADER1 | Analog input enable 1 | R/W | Port 7, A/D | - - - - 1 1 1 1$_B$ |
| 000020$_H$ | SMR0 | Serial mode register | R/W | UART0 | 0 0 0 0 0 - 0 0$_B$ |
| 000021$_H$ | SCR0 | Serial control register | R/W | | 0 0 0 0 0 1 0 0$_B$ |
| 000022$_H$ | S1DR0/ SODR0 | Serial input/output register | R/W | | XXXXXXXX$_B$ |
| 000023$_H$ | SSR0 | Serial data register | R/W | | 0 0 0 0 10 0 0$_B$ |
| 000024$_H$ | | Prohibited | | | |
| 000025$_H$ | CDCR0 | Communication prescaler control register | R/W | Prescaler 0 | 0 0 - - 0 0 0 0$_B$ |
| 000026$_H$, 000027$_H$ | | Prohibited | | | |

*(Continued)*

| Address | Register abbreviation | Register | Read/Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| 000028H | SMR1 | Serial mode register | R/W | UART1 | 0 0 0 0 0 - 0 0B |
| 000029H | SCR1 | Serial control register | R/W, W | | 0 0 0 0 0 1 0 0B |
| 00002AH | SIDR1/ SODR1 | Serial input/output register | R/W | | XXXXXXXXB |
| 00002BH | SSR1 | Serial data register | R/W, R | | 0 0 0 0 1 0 0 0B |
| 00002CH | | Prohibited | | | |
| 00002DH | CDCR1 | Communication prescaler control register | R/W | Prescaler 1 | 0 0 - - 0 0 0 0B |
| 00002EH | | Prohibited | | | |
| 00002FH | | | | | |
| 000030H | ENIR | Interrupt/DTP enable | R/W | External interrupt | - - - - 0 0 0 0B |
| 000031H | EIRR | Interrupt/DTP source | R/W | | - - - - XXXXB |
| 000032H | ELVR | Request level set register | R/W | | 0 0 0 0 0 0 0 0B |
| 000033H | | Prohibited | | | |
| 000034H | ADCS0 | Control status register (lower) | R/W | A/D converter | 0 0 - - - - - - B |
| 000035H | ADCS1 | Control status register (upper) | W, R/W | | 0 0 0 0 0 0 0 0B |
| 000036H | ADCR0 | Data register (lower) | R | | XXXXXXXXB |
| 000037H | ADCR1 | Data register (upper) | R, W | | 0 0 1 0 1 - XXB |
| 000038H | | Prohibited | | | |
| 000039H | ADMR | A/D conversion channel set register | R/W | A/D converter | 0 0 0 0 0 0 0 0B |
| 00003AH | CPCLR | Compare clear register | R/W | 16-bit free-run timer | XXXXXXXXB |
| 00003BH | | | | | XXXXXXXXB |
| 00003CH | TCDT | Timer counter data register | R/W | | 0 0 0 0 0 0 0 0B |
| 00003DH | | | | | 0 0 0 0 0 0 0 0B |
| 00003EH | TCCSL | Timer counter control/status register (lower) | R/W | | 0 0 0 0 0 0 0 0B |
| 00003FH | TCCSH | Timer counter control/status register (upper) | R/W | | 0 - - 0 0 0 0 0B |
| 000040H to 000043H | | Prohibited | | | |
| 000044H | IPCP0 | Input capture data register 0 | R | Input Capture 0/1 | XXXXXXXXB |
| 000045H | | | | | XXXXXXXXB |
| 000046H | IPCP1 | Input capture data register 1 | | | XXXXXXXXB |
| 000047H | | | | | XXXXXXXXB |
| 000048H | ICS01 | Control status register | R/W | | 0 0 0 0 0 0 0 0B |
| 000049H | | Prohibited | | | |
| 00004AH | OCCP0 | Compare register 0 | R/W | Output compare 0 | 0 0 0 0 0 0 0 0B |
| 00004BH | | | | | 0 0 0 0 0 0 0 0B |
| 00004CH | OCCP1 | Compare register 1 | R/W | Output compare 1 | 0 0 0 0 0 0 0 0B |
| 00004DH | | | | | 0 0 0 0 0 0 0 0B |

*(Continued)*

| Address | Register abbreviation | Register | Read/Write | Resource name | Initial Value |
|---------|----------------------|----------|------------|---------------|---------------|
| 00004E$_H$ | OCSL | Control register (lower) | R/W | Output Compare 0/1 | 0 0 0 0 - - 0 0$_B$ |
| 00004F$_H$ | OCSH | Control register (upper) | R/W | | - - - 0 0 0 0 0$_B$ |
| 000050$_H$ | TMCSR0L | Timer control status register (lower) | R/W | 16-bit reload timer 0 | 0 0 0 0 0 0 0 0$_B$ |
| 000051$_H$ | TMCSR0H | Timer control Status register (upper) | R/W | | - - - - 0 0 0 0$_B$ |
| 000052$_H$ | TMR0/ TMRLR0 | 16-bit timer register/Reload register | R/W | | XXXXXXXX$_B$ |
| 000053$_H$ | | | | | XXXXXXXX$_B$ |
| 000054$_H$ | TMCSR1L | Timer control status register (lower) | R/W | 16-bit reload timer 1 | 0 0 0 0 0 0 0 0$_B$ |
| 000055$_H$ | TMCSR1H | Timer control status register (upper) | R/W | | - - - - 0 0 0 0$_B$ |
| 000056$_H$ | TMR1/ TMRLR1 | 16-bit timer register/Reload register | R/W | | XXXXXXXX$_B$ |
| 000057$_H$ | | | | | XXXXXXXX$_B$ |
| 000058$_H$ | TMCSR2L | Timer control status register (lower) | R/W | 16-bit reload timer 2 | 0 0 0 0 0 0 0 0$_B$ |
| 000059$_H$ | TMCSR2H | Timer control status register (upper) | R/W | | - - - - 0 0 0 0$_B$ |
| 00005A$_H$ | TMR2/ TMRLR2 | 16-bit timer register/Reload register | R/W | | XXXXXXXX$_B$ |
| 00005B$_H$ | | | | | XXXXXXXX$_B$ |
| 00005C$_H$ | LCRL | LCD control register (lower) | R/W | LCD controller/ driver | 0 0 0 1 0 0 0 0$_B$ |
| 00005D$_H$ | LCRH | LCD control register (upper) | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 00005E$_H$ | LCRR | LCD range register | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 00005F$_H$ | | Prohibited | | | |
| 000060$_H$ | SMCS0 | Serial mode control status register | R, R/W | SIO (Extended Serial I/O) | 0 0 0 0 0 0 1 0$_B$ |
| 000061$_H$ | | | R/W | | - - - - 0 0 0 0$_B$ |
| 000062$_H$ | SDR0 | Serial Data Register | R/W | | XXXXXXXX$_B$ |
| 000063$_H$ | SDCR0 | Communication prescaler control register | R/W | Communication prescaler (SIO) | 0 - - - 0 0 0 0$_B$ |
| 000064$_H$ | SMCS1 | Serial mode control status register | R, R/W | SIO (Extended Serial I/O) | 0 0 0 0 0 0 1 0$_B$ |
| 000065$_H$ | | | R/W | | - - - - 0 0 0 0$_B$ |
| 000066$_H$ | SDR1 | Serial Data Register | R/W | | XXXXXXXX$_B$ |
| 000067$_H$ | SDCR1 | Communication prescaler control register | R/W | Communication prescaler (SIO) | 0 - - - 0 0 0 0$_B$ |
| 000068$_H$ | | Prohibited | | | |
| 000069$_H$ | | | | | |
| 00006A$_H$ | IBSR | I$^2$C status register | R | I$^2$C | 0 0 0 0 0 0 0 0$_B$ |
| 00006B$_H$ | IBCR | I$^2$C control register | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 00006C$_H$ | ICCR | I$^2$C clock selection register | R/W | | XX0XXXXX$_B$ |
| 00006D$_H$ | IADR | I$^2$C address register | R/W | | XXXXXXXX$_B$ |
| 00006E$_H$ | IDAR | I$^2$C data register | R/W | | XXXXXXXX$_B$ |
| 00006F$_H$ | ROMM | ROM mirror function select register | R/W, W | ROM mirror | XXXXXXX1$_B$ |

*(Continued)*

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| Address | Register abbreviation | Register | Read/ Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| $000070_H$ | PDCRL0 | PDCRL0/PDCRH0 PPG down counter register | R | 16-bit PPG0 | 1 1 1 1 1 1 1 $1_B$ |
| $000071_H$ | PDCRH0 | | | | 1 1 1 1 1 1 1 $1_B$ |
| $000072_H$ | PCSRL0 | PCSRL0/PCSRH0 PPG cycle set register | W | | $XXXXXXXX_B$ |
| $000073_H$ | PCSRH0 | | | | $XXXXXXXX_B$ |
| $000074_H$ | PDUTL0 | PDUTL0/PDUTH0 PPG duty setting register | W | | $XXXXXXXX_B$ |
| $000075_H$ | PDUTH0 | | | | $XXXXXXXX_B$ |
| $000076_H$ | PCNTL0 | PCNTL0/PCNTH0 PPG control status register | R/W | | - - 0 0 0 0 0 $0_B$ |
| $000077_H$ | PCNTH0 | | | | 0 0 0 0 0 0 0 $-_B$ |
| $000078_H$ | PDCRL1 | PDCRL1/PDCRH1 PPG down counter register | R | 16-bit PPG1 | 1 1 1 1 1 1 1 $1_B$ |
| $000079_H$ | PDCRH1 | | | | 1 1 1 1 1 1 1 $1_B$ |
| $00007A_H$ | PCSRL1 | PCSRL1/PCSRH1 PPG cycle set register | W | | $XXXXXXXX_B$ |
| $00007B_H$ | PCSRH1 | | | | $XXXXXXXX_B$ |
| $00007C_H$ | PDUTL1 | PDUTL1/PDUTH1 PPG duty setting register | W | | $XXXXXXXX_B$ |
| $00007D_H$ | PDUTH1 | | | | $XXXXXXXX_B$ |
| $00007E_H$ | PCNTL1 | PCNTL1/PCNTH1 PPG control status register | R/W | | - - 0 0 0 0 0 $0_B$ |
| $00007F_H$ | PCNTH1 | | | | 0 0 0 0 0 0 0 $-_B$ |
| $000080_H$ to $000095_H$ | | (Reserved) | | | |
| $000096_H$ | | Prohibited | | | |
| $000097_H$ | | (Reserved) | | | |
| $000098_H$ to $00009D_H$ | | Prohibited | | | |
| $00009E_H$ | PACSR | ROM correction control register | R/W | ROM Correction | 0 0 0 0 0 0 0 $0_B$ |
| $00009F_H$ | DIRR | Delayed interrupt source generated/ release register | R/W | Delayed interrupt | - - - - - - - $0_B$ |
| $0000A0_H$ | LPMCR | Low power consumption mode control register | R/W, W | Low power consumption control circuit | 0 0 0 1 1 0 0 $0_B$ |
| $0000A1_H$ | CKSCR | Clock selector register | R/W, R | | 1 1 1 1 1 1 0 $0_B$ |
| $0000A2_H$ to $0000A7_H$ | | Prohibited | | | |
| $0000A8_H$ | WDTC | Watchdog timer control | R, W | Watchdog timer | XXXXX 1 1 $1_B$ |
| $0000A9_H$ | TBTC | Time-base timer control register | R/W, W | Time-base timer | 1 - - 0 0 1 0 $0_B$ |
| $0000AA_H$ | WTC | Watch timer control register | R/W, R | Watch timer (Sub clock) | 1 X0 1 1 0 0 $0_B$ |
| $0000AB_H$ to $0000AD_H$ | | Prohibited | | | |

*(Continued)*

*(Continued)*

| Address | Register abbreviation | Register | Read/Write | Resource name | Initial Value |
|---|---|---|---|---|---|
| $0000AE_H$ | FMCS | Flash control register | R/W | Flash I/F | 0 0 0 X 0 0 0 $0_B$ |
| $0000AF_H$ | TMCS | Timer clock output control register | R/W | Timer clock divide | XXXXX 0 0 $0_B$ |
| $0000B0_H$ | ICR00 | Interrupt control register 00 | R/W, W, R | Interrupt controller | 0 0 0 0 0 1 1 $1_B$ |
| $0000B1_H$ | ICR01 | Interrupt control register 01 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B2_H$ | ICR02 | Interrupt control register 02 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B3_H$ | ICR03 | Interrupt control register 03 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B4_H$ | ICR04 | Interrupt control register 04 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B5_H$ | ICR05 | Interrupt control register 05 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B6_H$ | ICR06 | Interrupt control register 06 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B7_H$ | ICR07 | Interrupt control register 07 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B8_H$ | ICR08 | Interrupt control register 08 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000B9_H$ | ICR09 | Interrupt control register 09 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000BA_H$ | ICR10 | Interrupt control register 10 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000BB_H$ | ICR11 | Interrupt control register 11 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000BC_H$ | ICR12 | Interrupt control register 12 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000BD_H$ | ICR13 | Interrupt control register 13 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000BE_H$ | ICR14 | Interrupt control register 14 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $0000BF_H$ | ICR15 | Interrupt control register 15 | R/W, W, R | | 0 0 0 0 0 1 1 $1_B$ |
| $001FF0_H$ | PADR0 | Program address detection register 0 | R/W | Address matching detection function | $XXXXXXXX_B$ |
| $001FF1_H$ | | | | | $XXXXXXXX_B$ |
| $001FF2_H$ | | | | | $XXXXXXXX_B$ |
| $001FF3_H$ | PADR1 | Program address detection register 1 | R/W | | $XXXXXXXX_B$ |
| $001FF4_H$ | | | | | $XXXXXXXX_B$ |
| $001FF5_H$ | | | | | $XXXXXXXX_B$ |
| $007900_H$ to $007917_H$ | VRAM | LCD display RAM | R/W | LCD controller/driver | $XXXXXXXX_B$ |

- Read/Write
  - R/W : Readable and Writable
  - R : Read only
  - W : Write only

- Initial values
  - 0 : Initial Value is "0".
  - 1 : Initial Value is "1".
  - X : Initial Value is Indeterminate.
  - - : Unused bit

## ■ INTERRUPT SOURCES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTERS

| Interrupt source | EI$^2$OS readiness | Interrupt vector | | Interrupt control register | | Priority |
|---|---|---|---|---|---|---|
| | | Number* | Address | ICR | Address | |
| Reset | × | #08 | 08$_H$ | FFFFDC$_H$ | — | — | High |
| INT 9 instruction | × | #09 | 09$_H$ | FFFFD8$_H$ | — | — | |
| Exceptional treatment | × | #10 | 0A$_H$ | FFFFD4$_H$ | — | — | |
| DTP/External interrupt ch.0 | ○ | #11 | 0B$_H$ | FFFFD0$_H$ | ICR00 | 0000B0$_H$ | |
| DTP/External interrupt ch.1 | ○ | #13 | 0D$_H$ | FFFFC8$_H$ | ICR01 | 0000B1$_H$ | |
| Serial I/O ch.2 | × | #15 | 0F$_H$ | FFFFC0$_H$ | ICR02 | 0000B2$_H$ | |
| DTP/External interrupt ch.2/ch.3 | ○ | #16 | 10$_H$ | FFFFBC$_H$ | | | |
| Serial I/O ch.3 | × | #17 | 11$_H$ | FFFFB8$_H$ | ICR03 | 0000B3$_H$ | |
| 16-bit free-run timer | ○ | #18 | 12$_H$ | FFFFB4$_H$ | | | |
| Watch timer | × | #19 | 13$_H$ | FFFFB0$_H$ | ICR04 | 0000B4$_H$ | |
| 16-bit Reload Timer ch.2 | ○ | #21 | 15$_H$ | FFFFA8$_H$ | ICR05 | 0000B5$_H$ | |
| 16-bit Reload Timer ch.0 | △ | #23 | 17$_H$ | FFFFA0$_H$ | ICR06 | 0000B6$_H$ | |
| 16-bit Reload Timer ch.1 | △ | #24 | 18$_H$ | FFFF9C$_H$ | | | |
| Input capture ch.0 | △ | #25 | 19$_H$ | FFFF98$_H$ | ICR07 | 0000B7$_H$ | |
| Input capture ch.1 | △ | #26 | 1A$_H$ | FFFF94$_H$ | | | |
| PPG timer ch.0 counter-borrow | ○ | #27 | 1B$_H$ | FFFF90$_H$ | ICR08 | 0000B8$_H$ | |
| Output compare match | ○ | #29 | 1D$_H$ | FFFF88$_H$ | ICR09 | 0000B9$_H$ | |
| PPG timer ch.1 counter-borrow | ○ | #31 | 1F$_H$ | FFFF80$_H$ | ICR10 | 0000BA$_H$ | |
| Time-base timer | × | #33 | 21$_H$ | FFFF78$_H$ | ICR11 | 0000BB$_H$ | |
| UART0 reception end | ◎ | #35 | 23$_H$ | FFFF70$_H$ | ICR12 | 0000BC$_H$ | |
| UART0 transmission end | △ | #36 | 24$_H$ | FFFF6C$_H$ | | | |
| A/D converter conversion termination | ○ | #37 | 25$_H$ | FFFF68$_H$ | ICR13 | 0000BD$_H$ | |
| I$^2$C Interface | × | #38 | 26$_H$ | FFFF64$_H$ | | | |
| UART1 : Reception | ◎ | #39 | 27$_H$ | FFFF60$_H$ | ICR14 | 0000BE$_H$ | |
| UART1 : Transmission | △ | #40 | 28$_H$ | FFFF5C$_H$ | | | |
| Flash memory status | × | #41 | 29$_H$ | FFFF58$_H$ | ICR15 | 0000BF$_H$ | |
| Delayed interrupt output module | × | #42 | 2A$_H$ | FFFF54$_H$ | | | Low |

○ : Available
× : Unavailable
◎ : Available EI$^2$OS function is provided.
△ : Available when a cause of interrupt sharing a same ICR is not used.

* : When interrupts of the same level are output at the same time, the interrupt with the smallest interrupt vector number has the priority.
- For a resource that has two interrupt causes in the same interrupt control register (ICR), use of EI$^2$OS is enabled, EI$^2$OS is started upon detection of one of the interrupt causes. As interrupts other than the start cause are masked during EI$^2$OS start, masking one of the interrupt causes is recommended when using EI$^2$OS.
- For a resource that has two interrupt causes in the same interrupt control register (ICR), the interrupt flag is cleared by an EI$^2$OS interrupt clear signal.

## ■ PERIPHERAL RESOURCES

### 1. I/O port

The I/O ports function to output data from the CPU to I/O pins by setting their port data register (PDR) and send signals input to I/O pins to the CPU. In addition, the port can randomly set the direction of the input/output of the port in bit by the port direction register (DDR).

The MB90800 series has 68 (70 ports when the subclock is not used) input/output pins. Port0 to port8 (port0 to port9 when product without the subclock is used) are input/output port.

### (1) Port data register

| | | | | | | | | | Initial Value | Access |
|---|---|---|---|---|---|---|---|---|---|---|
| PDR0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Address : 000000H | P07 | P06 | P05 | P04 | P03 | P02 | P01 | P00 | Indeterminate | R/W* |
| PDR1 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
| Address : 000001H | P17 | P16 | P15 | P14 | P13 | P12 | P11 | P10 | Indeterminate | R/W* |
| PDR2 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Address : 000002H | P27 | P26 | P25 | P24 | P23 | P22 | P21 | P20 | Indeterminate | R/W* |
| PDR3 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
| Address : 000003H | P37 | P36 | P35 | P34 | P33 | P32 | P31 | P30 | Indeterminate | R/W* |
| PDR4 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Address : 000004H | P47 | P46 | P45 | P44 | P43 | P42 | P41 | P40 | Indeterminate | R/W* |
| PDR5 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
| Address : 000005H | P57 | P56 | P55 | P54 | P53 | P52 | P51 | P50 | Indeterminate | R/W* |
| PDR6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Address : 000006H | P67 | P66 | P65 | P64 | P63 | P62 | P61 | P60 | Indeterminate | R/W* |
| PDR7 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
| Address : 000007H | — | P76 | P75 | P74 | P73 | P72 | P71 | P70 | Indeterminate | R/W* |
| PDR8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| Address : 000008H | — | — | — | P84 | P83 | P82 | P81 | P80 | Indeterminate | R/W* |
| PDR9 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
| Address : 000009H | — | — | — | — | — | — | P91 | P90 | Indeterminate | R/W* |

- : Unused

\* : R/W access to I/O ports is a bit different in behavior from R/W access to memory as follows
- Input mode
    - When reading : Read the corresponding pin level.
    - When writing : Write into the latch for the output.
- Output mode
    - When reading : Read the value of the data register latch.
    - When writing : Write into the corresponding pin.

**(2) Port direction register**

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR0 Address : 000010H | | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D 00 | 00000000B | R/W |

| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR1 Address : 000011H | | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00000000B | R/W |

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR2 Address : 000012H | | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | 00000000B | R/W |

| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR3 Address : 000013H | | D37 | D36 | D35 | D34 | D33 | D32 | D31 | D30 | 00000000B | R/W |

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR4 Address : 000014H | | D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 | 00000000B | R/W |

| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR5 Address : 000015H | | D57 | D56 | D55 | D54 | D53 | D52 | D51 | D50 | 00000000B | R/W |

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR6 Address : 000016H | | D67 | D66 | D65 | D64 | D63 | D62 | D61 | D60 | 00000000B | R/W |

| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR7 Address : 000017H | | — | D76 | D75 | D74 | D73 | D72 | D71 | D70 | - 0000000B | R/W |

| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR8 Address : 000018H | | — | — | — | D84 | D83 | D82 | D81 | D80 | - - - 00000B | R/W |

| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR9 Address : 000019H | | — | — | — | — | — | — | D91 | D90 | - - - - - - 00B | R/W |

- : Unused

When each terminal functions as a port, each correspondent pin are controlled by the port direction register to following;
0 : Input mode
1 : Output mode     This bit becomes "0" after a reset.

Note : When accessing this register by using the instruction of the read modify write system (instructions such as bit set) is mode, the bit targeted by an instruction becomes the defined value. However, the content of the output register set to input with the other changes to input value of the pin at that time. Therefore, be sure to write an expected value into PDR firstly, and then set DDR and finally change to the output when changing the input pin to the output pin is made.

**(3) Analog Input Enable register**

ADER0
Address : 00001E_H

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ADE7 | ADE6 | ADE5 | ADE4 | ADE3 | ADE2 | ADE1 | ADE0 |

Initial Value    Access
11111111_B    R/W

ADER1
Address : 00001F_H

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | ADE11 | ADE10 | ADE9 | ADE8 |

- - - -1111_B    R/W

-　: Unused

Each pin of port 6 is controlled by the analog input enable register as follow.

　　0 : Port input/output mode.

　　1 : Analog input mode.This bit becomes "1" after a reset.

## 2. UART

UART is a serial I/O port for asynchronous (start-stop synchronization) communication or CLK synchronous communications.

- With full-duplex double buffer
- Clock asynchronous (start-stop synchronization) , CLK synchronous communications (no start-bit/stop-bit) can be used.
- Supports multi-processor mode
- Built-in dedicated baud rate generator

  Asynchronous    : 120192/60096/30048/15024/781.25 K/390.625 Kbps
  CLK synchronous  : 25 M/12.5 M/6.25 M/3.125 M/1.5627 M/781.25 Kbps
- Variable baud rate can be set by an external clock.
- 7-bits data length (only asynchronous normal mode) /8-bits length
- Master/slave type communication function (at multiprocessor mode) : The communication between one (master) to n (slave) can be operating.
- Error detection functions(parity, framing, overrun)
- Transmission signal format is NRZ

## (1) Register list

| 15 | 8 | 7 | 0 |
|---|---|---|---|
| CDCR | | — | |
| SCR | | SMR | |
| SSR | | SIDR (R)/SODR (W) | |

← 8-bit → ← 8-bit →
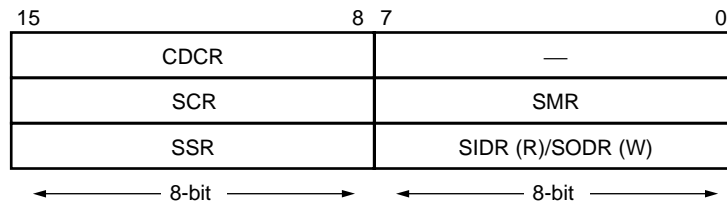
**Serial mode register (SMR0, SMR1)**

Address : 000020H / 000028H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MD1 | MD0 | CS2 | CS1 | CS0 | — | SCKE | SOE |
| R/W | R/W | R/W | R/W | R/W | — | R/W | R/W |

Initial Value
00000 - 00B
Read/Write

**Serial control register(SCR0, SCR1)**

Address : 000021H / 000029H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PEN | P | SBL | CL | A/D | REC | RXE | TXE |
| R/W | R/W | R/W | R/W | R/W | W | R/W | R/W |

Initial Value
00000100B
Read/Write

**Serial input/output register (SIDR0, SIDR1/SODR0, SODR1)**

Address : 000022H / 00002AH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial Value
XXXXXXXXB
Read/Write

**Serial Data Register (SSR0, SSR1)**

Address : 000023H / 00002BH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| PE | ORE | FRE | RDRF | TDRE | BDS | RIE | TIE |
| R | R | R | R | R | R/W | R/W | R/W |

Initial Value
00001000B
Read/Write

**Communication prescaler control register (CDCR0, CDCR1)**

Address : 000025H / 00002DH

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| MD | URST | — | — | Reserved | DIV2 | DIV1 | DIV0 |
| R/W | R/W | — | — | R/W | R/W | R/W | R/W |

Initial Value
00 - - 0000B
Read/Write

- : Unused

**(2) Block Diagram**

Control signal

Special-purpose
baud-rate generator

16-bit reload timer 0

Pin

Clock
selection
circuit

RX interrupt
(to CPU)

Transmission clock

TX interrupt
(to CPU)

Reception clock

Pin

Reception control
circuit

Start bit
detection circuit

Reception bit
counter

Reception
parity counter

Transmission
control circuit

Transmission
start circuit

Transmission bit
counter

Transmission
parity counter

Pin

Receive status
decision circuit

Reception error
occurrence signal
for EI$^2$OS (to CPU)

RX shifter

Reception
control
circuit

SIDR

TX shifter

Start
transmission

SODR

F$^2$MC-16LX bus

SMR
Register

MD1
MD0
CS2
CS1
CS0

SCKE
SOE

SCR
Register

PEN
P
SBL
CL
A/D
REC
REX
TXE

SSR
Register

PE
ORE
FRE
RDRF
TDRE
BDS
RIE
TIE

Control signal

## 3. I²C Interface

I²C interface is the serial input/output port that support Inter IC BUS and functions as the master/slave device on the I²C bus. MB90800 series have 1 channel of the built-in I²C interface.

**It has the features of I²C interface below.**

- Master/slave sending and receiving
- Arbitration function
- Clock synchronization function
- Slave address and general call address detection function
- Detecting transmitting direction function
- Repeat generating and detecting function of the start conditions
- Bus error detection function
- The forwarding rate can be supported to 100 Kbps.

### (1) Register list

I²C status register (IBSR)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| Address :00006A$_H$ | BB | RSC | AL | LRB | TRX | AAS | GCA | FBT | 00000000$_B$ |
| | R | R | R | R | R | R | R | R | Read/Write |

I²C control register (IBCR)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| Address :00006B$_H$ | BER | BEIE | SCC | MSS | ACK | GCAA | INTE | INT | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

I²C clock control register (ICCR)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| Address :00006C$_H$ | — | — | EN | CS4 | CS3 | CS2 | CS1 | CS0 | XX0XXXXX$_B$ |
| | — | — | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

I²C data register(IDAR)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| Address :00006E$_H$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXX$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

I²C address register (IADR)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| Address :00006D$_H$ | — | A6 | A5 | A4 | A3 | A2 | A1 | A0 | XXXXXXXX$_B$ |
| | — | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

- : Unused

31

**(2) Block Diagram**

## 4. Extended I/O serial interface

The extended I/O serial interface is a serial I/O interface that can transfer data through the adoption of 8-bit × 2 channels configured clock synchronization scheme. The extended I/O serial interface also has two alternatives in data transfer called LSB first and MSB first.

The serial I/O interface operates in two modes:
- Internal shift clock mode : Transfer data in sync with the internal clock.
- External shift clock mode : Transfers data in sync with the clock input through an external pin (SCK) . In this mode, transfer operation performed by the CPU instruction is also available by operating the general-use port sharing an external pin (SCK) .

### (1) Register list

Serial mode control status register(SMCS0, SMCS1)

| Address : | 000060H 000064H | | | | | | | | Initial Value |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|
| SMD2 | SMD1 | SMD0 | SIE | SIR | BUSY | STOP | STRT | 00000010B |
| R/W | R/W | R/W | R/W | R/W | R | R/W | R/W | Read/Write |

Address : 000061H / 000065H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| — | — | — | — | MODE | BDS | SOE | SCOE | ----0000B |
| — | — | — | — | R/W | R/W | R/W | R/W | Read/Write |

Serial Data Register (SDR0, SDR1)

Address : 000062H / 000066H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | XXXXXXXXB |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

Communication Prescaler control register (SDCR0, SDCR1)

Address : 000063H / 000067H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|
| MD | — | — | — | Reserved | DIV2 | DIV1 | DIV0 | 0---0000B |
| R/W | — | — | — | R/W | R/W | R/W | R/W | Read/Write |

- : Unused

**(2) Block Diagram**
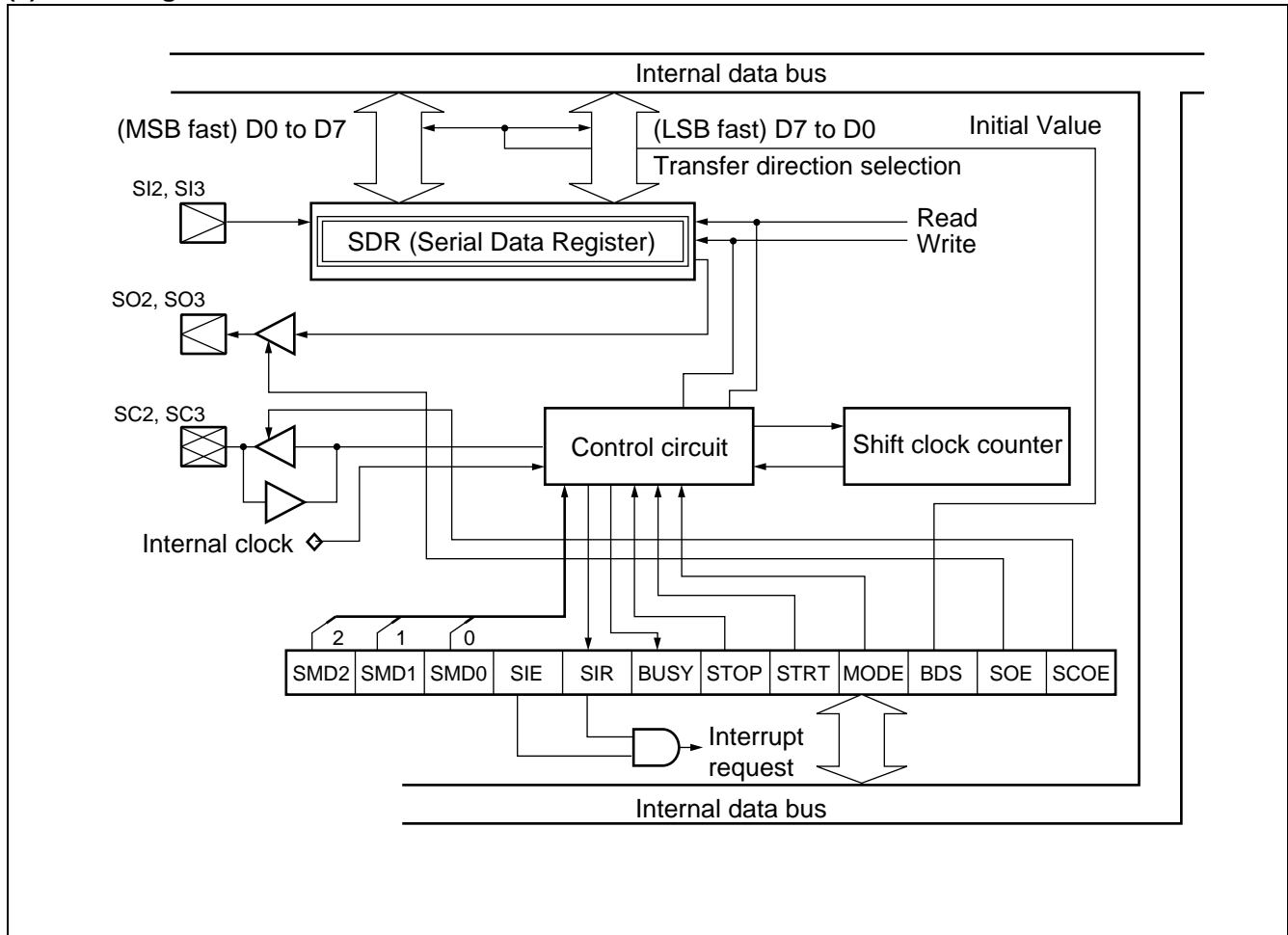
## 5.   8/10-bit A/D converter

The feature of 8/10-bit A/D converter is shown as follows.
 •  conversion time : 3.1 μs minimum per 1 channel

(78 machine cycle/at machine clock 25 MHz/including the sampling time)
 •  Sampling time : 2.0 μs minimum per 1channel

(50 machine cycle/at machine clock 25 MHz)
 •  Uses RC-type successive approximation conversion method with a sample & hold circuit
 •  8-bit resolution or 10-bit resolution can be select.
 •  12 channel program-selectable analog inputs.
   Single conversion mode         : Convert specified 1 channel
   Scan conversion mode           : Continuous plural channels (maximum 12 channels can be programmed) are
                                                converted.
   Continuous conversion mode  : Selected channel converted continuously.
   Stop conversion time             : Perform conversion for one channel, then pause it to wait for the next activation
                                                trigger (synchronizes the conversion start timing)
 •  EI²OS can be activated by outputting the interrupt request when the A/D conversion completes.
 •  If the A/D conversion is performed under the condition of the interrupt enable, the converting data will be
   protected.
 •  Selectable conversion activation trigger : Software, or reload timer (rising edge)

### (1) Register list

ADCS1, ADCS0 (Control status register)

ADCS0
Address  : 000034H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MD1 | MD0 | — | — | — | — | — | — |
| R/W | R/W | — | — | — | — | — | — |

Initial Value
00 - - - - - - B
Read/Write

ADCS1              bit
Address  : 000035H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|----|----|----|----|----|----|---|---|
| BUSY | INT | INTE | PAUS | STS1 | STS0 | STRT | Reserved |
| R/W | R/W | R/W | R/W | R/W | R/W | W | R/W |

Initial Value
00000000B
Read/Write

ADCR1, ADCR0 (data register)

ADCR0              bit
Address  : 000036H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| R | R | R | R | R | R | R | R |

Initial Value
XXXXXXXXB
Read/Write

ADCR1              bit
Address  : 000037H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|----|----|----|----|----|----|---|---|
| S10 | ST1 | ST0 | CT1 | CT0 | — | D9 | D8 |
| W | W | W | W | W | — | R | R |

Initial Value
00101 - XXB
Read/Write

-   : Unused

**(2) Block Diagram**

## 6.   16 bits PPG

The PPG timer consists of the following:
• Prescaler
• 16-bit down-counter: 1
• 16-bit data register with a cycle setting buffer
• 16-bit compare register with a duty setting buffer
• Pin control unit

The PPG timer can output pulses synchronized to the software trigger.

The output pulse can be changed to any cycle and duty freely by updating the PCSRL, PCSRH/PDUTL, PDUTH registers.

• PWM function

The PPG timer can output pulses programmably by updating the PCSR and PDVT registers described above in synchronization to the trigger.

Can also be used as a D/A converter by an external circuit.

• Single shot function

By detecting an edge of the trigger input, a single pulse can be output.

• 16-bit down counter

The counter operation clock comes from eight kinds optional. There are eight kinds of internal clocks.

($\phi$, $\phi2$, $\phi4$, $\phi8$, $\phi16$, $\phi32$, $\phi64$, $\phi128$)  $\phi$ : machine clock

The counter can be initialized to " $FFFF_H$ " at a reset or counter borrow.

• Interrupt request

The PPG timer generates an interrupt request when :
  • Timer start-up
  • Counter borrow occurrence (cycle match)
  • Duty match occurrence

## (1) Register list

PCNTH (PCNTH0/PCNTH1 Control Status register)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000077$_H$ 00007F$_H$ | CNTE | STGR | MDSE | RTRG | CSK2 | CSK1 | CSK0 | PGMS | 0000000X$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

PCNTL (PCNTL0/PCNTL1 Control Status register)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000076$_H$ 00007E$_H$ | — | — | IREN | IRQF | IRS1 | IRS0 | POEN | OSEL | - - 000000$_B$ |
| | — | — | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

PDCRH (PDCRH0/PDCRH1 PPG Down Counter Register)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000071$_H$ 000079$_H$ | DC15 | DC14 | DC13 | DC12 | DC11 | DC10 | DC09 | DC08 | 11111111$_B$ |
| | R | R | R | R | R | R | R | R | Read/Write |

PDCRL (PDCRL0/PDCRL1 PPG Down Counter Register)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000070$_H$ 000078$_H$ | DC07 | DC06 | DC05 | DC04 | DC03 | DC02 | DC01 | DC00 | 11111111$_B$ |
| | R | R | R | R | R | R | R | R | Read/Write |

PCSRH (PCSRH0/PCSRH1 PPG cycle set register)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000073$_H$ 00007B$_H$ | CS15 | CS14 | CS13 | CS12 | CS11 | CS10 | CS09 | CS08 | XXXXXXXX$_B$ |
| | W | W | W | W | W | W | W | W | Read/Write |

PCSRL (PCSRL0/PCSRL1 PPG cycle set register)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000072$_H$ 00007A$_H$ | CS07 | CS06 | CS05 | CS04 | CS03 | CS02 | CS01 | CS00 | XXXXXXXX$_B$ |
| | W | W | W | W | W | W | W | W | Read/Write |

PDUTH (PDUTH0/PDUTH1 PPG duty set register)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000075$_H$ 00007D$_H$ | DU15 | DU14 | DU13 | DU12 | DU11 | DU10 | DU09 | DU08 | XXXXXXXX$_B$ |
| | W | W | W | W | W | W | W | W | Read/Write |

PDUTL (PDUTL0/PDUTL1 PPG duty set register)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000074$_H$ 00007C$_H$ | DU07 | DU06 | DU05 | DU04 | DU03 | DU02 | DU01 | DU00 | XXXXXXXX$_B$ |
| | W | W | W | W | W | W | W | W | Read/Write |

- : Unused

**(2) Block Diagram**
• 16-bit PPG ch.0/ch.1 block diagram
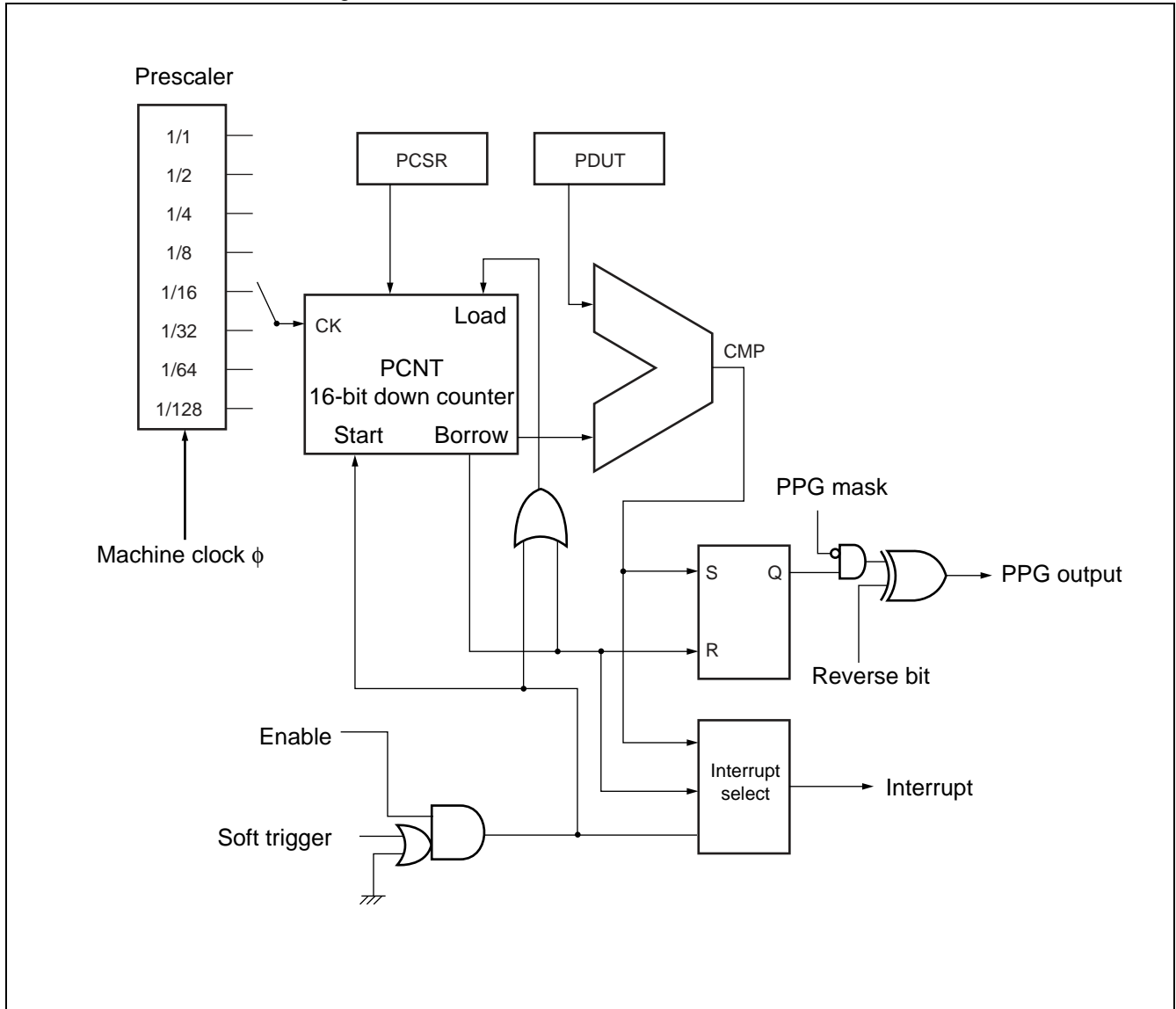
# MB90800 Series

## 7. Delay interrupt generator module

The delayed interrupt generation module outputs an interrupt request for task switching. The hardware interrupt request can be generated by software.

**(1) Register list**

Delayed Interrupt/release register(DIRR)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| DIRR | — | — | — | — | — | — | — | R0 | - - - - - - - $0_B$ |
| Address : 00009F$_H$ | — | — | — | — | — | — | — | R/W | Read/Write |

- : Unused

**(2) Block diagram**

F$^2$MC-16LX bus

Delay interruption factor generation/
release decoder

Factor latch
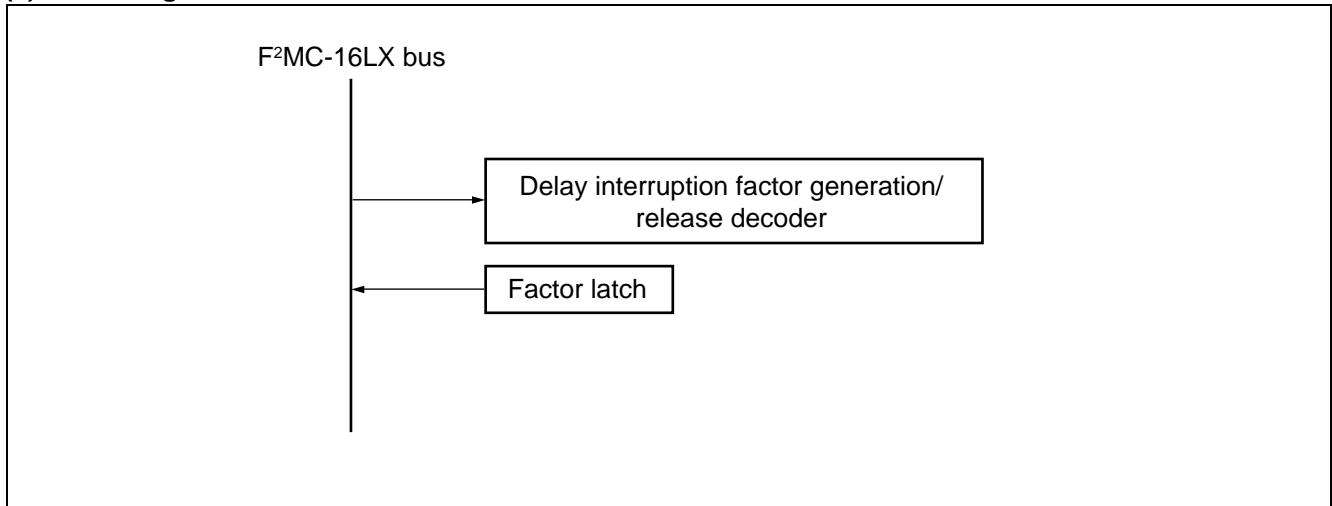
## 8. DTP/External interrupt

DTP (Data Transfer Peripheral)/External interrupt circuit detects the interrupt request input from the external interrupt input terminal, and outputs the interrupt request.

### (1) Register list

Interrupt/DTP enable register (ENIR)

ENIR
Address : 000030H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | EN3 | EN2 | EN1 | EN0 |
| — | — | — | — | R/W | R/W | R/W | R/W |

Initial Value
- - - - 0000B
Read/Write

Interrupt/DTP source register (EIRR)

EIRR
Address : 000031H

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|----|----|----|----|----|----|---|---|
| — | — | — | — | ER3 | ER2 | ER1 | ER0 |
| — | — | — | — | R/W | R/W | R/W | R/W |

Initial Value
- - - - XXXXB
Read/Write

Request level setting register (ELVR)

Address : 000032H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LB3 | LA3 | LB2 | LA2 | LB1 | LA1 | LB0 | LA0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial Value
00000000B
Read/Write

- : Unused

### (2) Block diagram

F$^2$MC-16LX bus

4 — Interrupt/DTP enable register

4 — Gate ← Source F/F ← Edge detection circuit — 4 — Request input

4 — Interrupt/DTP source register

8 — Request level setting register
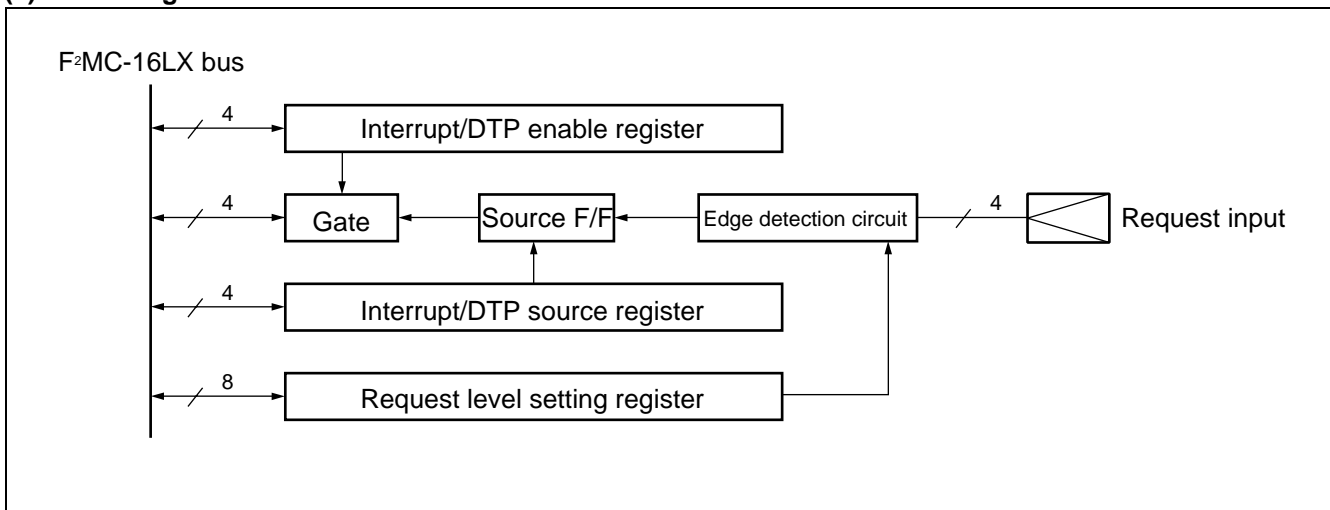
## 9. 16-bit input/output timer

The 16-bit I/O timer consists of one 16-bit free-run timer, two output compare and two input capture. This function enables six independent waveforms to be output based on the 16-bit free-run timer, and input pulse widths and external clock frequencies to be measured.

• Register list

• 16-bit free-run timer

| 15 | 0 | |
|---|---|---|
| 00003B$_H$/00003A$_H$ | CPCLR | Compare clear register |
| 00003D$_H$/00003C$_H$ | TCDT | Timer counter data register |
| 00003F$_H$/00003E$_H$ | TCCSH : TCCSL | Timer counter control/status register |

• 16-bit Output Compare

| 15 | 0 | |
|---|---|---|
| 00004A$_H$/00004B$_H$/ 00004C$_H$/00004D$_H$ | OCCP0, OCCP1 | Compare register |
| 00004F$_H$/00004E$_H$ | OCSH : OCSL | Control status register |

• 16-bit Input Capture

| 15 | 0 | |
|---|---|---|
| 000044$_H$/000045$_H$/ 000046$_H$/000047$_H$ | IPCP0, IPCP1 | Input capture data register |
| 000048$_H$ | ICS01 | Control status register |

• Block diagram

## (1) 16-bit free-run timer

The 16-bit free-run timer consists of a 16-bit up-down counter and control status register.

Counter value of 16-bit free-run timer is available as base timer for input capture and output compare.
- Clock for the counter operation can be selected from eight types.
- The counter overflow interruption can be generated.
- Setting the mode enables initialization of the counter through compare-match operation with the value of the compare clear register in the output compare and that of the free-run timer counter.

• Register list

Compare clear register (CPCLR)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00003B$_H$ | CL15 | CL14 | CL13 | CL12 | CL11 | CL10 | CL09 | CL08 | XXXXXXXX$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00003A$_H$ | CL07 | CL06 | CL05 | CL04 | CL03 | CL02 | CL01 | CL00 | XXXXXXXX$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

Timer counter data register (TCDT)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00003D$_H$ | T15 | T14 | T13 | T12 | T11 | T10 | T09 | T08 | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00003C$_H$ | T07 | T06 | T05 | T04 | T03 | T02 | T01 | T00 | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

Timer counter control/status register (TCCS)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00003F$_H$ | ECKE | — | — | MSI2 | MSI1 | MSI0 | ICLR | ICRE | 0--00000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00003E$_H$ | IVF | IVFE | STOP | MODE | SCLR | CLK2 | CLK1 | CLK0 | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

- : Unused

• Block diagram
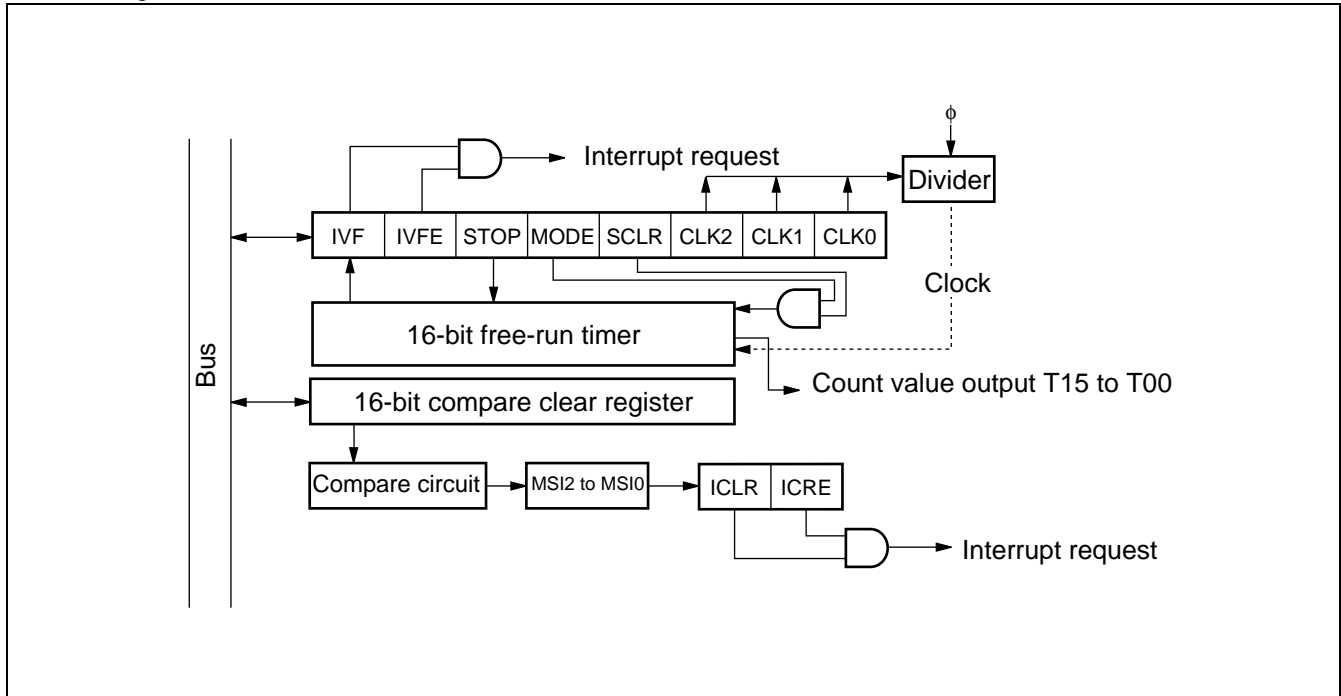
## (2) Output compare

The output compare consists of 16-bit compare registers, compare output pin part and a control register. It can reverse the output level for the pin and at the same time, generate an interrupt when the 16-bit free-run timer value matches a value set in one of the 16-bit compare registers of this module.
- It has a total of six compare registers that can operate independently. In addition, the output can be set to be controlled by using two compare registers.
- An interrupt can be set by a comparing match.

• Register list

Compare register (OCCP0, OCCP1)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00004B$_H$ 00004D$_H$ | OP15 | OP14 | OP13 | OP12 | OP11 | OP10 | OP09 | OP08 | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00004A$_H$ 00004C$_H$ | OP07 | OP06 | OP05 | OP04 | OP03 | OP02 | OP01 | C00 | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

Control register (OCSH)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00004F$_H$ | — | — | — | CMOD | OTE1 | OTE0 | OTD1 | OTD0 | ---00000$_B$ |
| | — | — | — | R/W | R/W | R/W | R/W | R/W | Read/Write |

Control register (OCSL)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00004E$_H$ | IOP1 | IOP0 | IOE1 | IOE0 | — | — | CST1 | CST0 | 0000--00$_B$ |
| | R/W | R/W | R/W | R/W | — | — | R/W | R/W | Read/Write |

-  : Unused

• Block diagram



16-bit timer counter value (T15 to T00)

Compare control

Compare register 0

16-bit timer counter value (T15 to T00)

Compare control

Compare register 1

Control logic

Each control blocks

Bus

TQ    OTE0

CMOD

TQ    OTE1

ICP1  ICP0  ICE0  ICE0

Interrupt

#29

#29
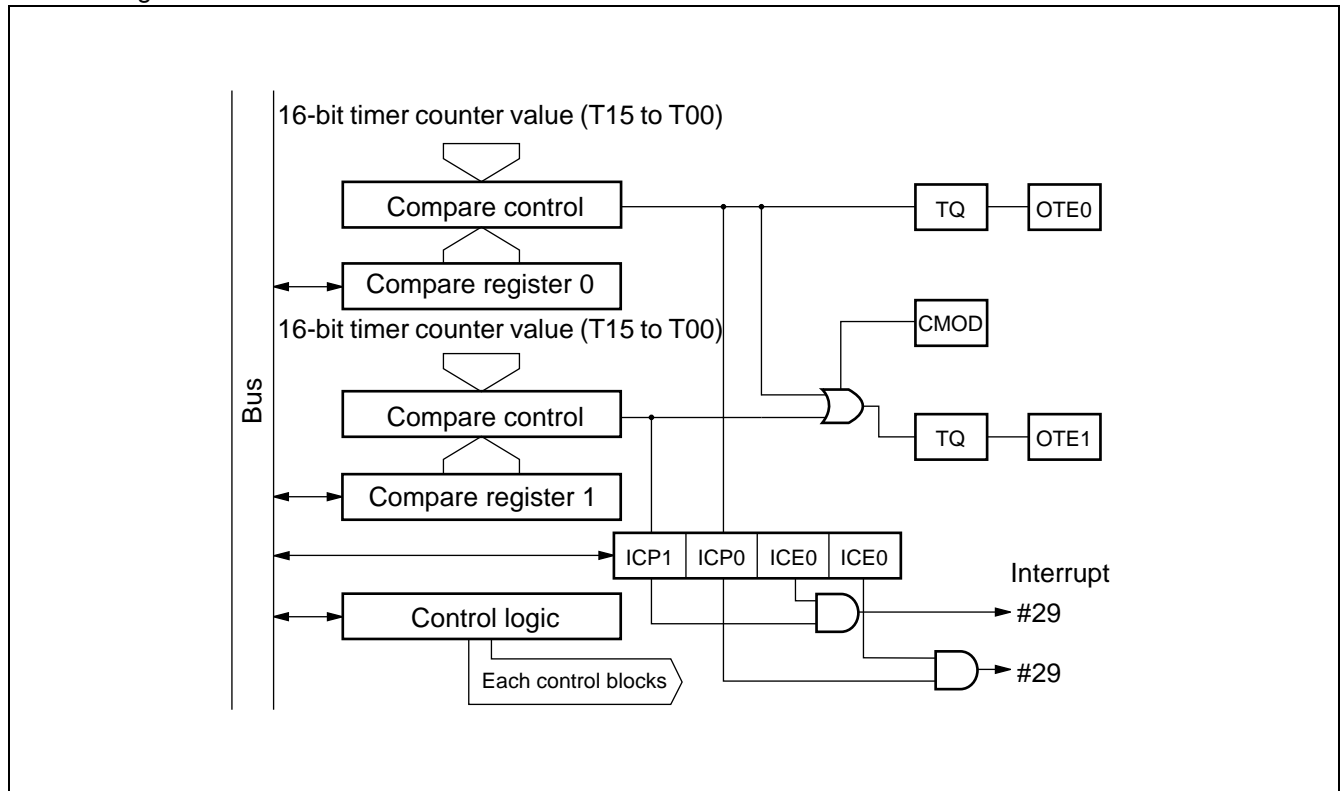
**(3) Input capture**

The input capture consists of input capture and control registers. Each input capture has its corresponding external input pin.

This module has a function that detects a rising edge, falling edge or both edges and holds a value of the 16-bit free-run timer in a register at the time of detection. It can also generate an interrupt when detecting an edge.
• The detection edge of an external input can be selected from among three types. Rising edge/falling edge/both edges.
• It can generate an interrupt when it detects the valid edge of the external input.

• Register list

Input capture data register (IPCP0, IPCP1)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000045H 000047H | CP15 | CP14 | CP13 | CP12 | CP11 | CP10 | CP09 | CP08 | XXXXXXXX$_B$ |
| | R | R | R | R | R | R | R | R | Read/Write |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000044H 000046H | CP07 | CP06 | CP05 | CP04 | CP03 | CP02 | CP01 | CP00 | XXXXXXXX$_B$ |
| | R | R | R | R | R | R | R | R | Read/Write |

Control status register (ICS01)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 000048H | ICP1 | ICP0 | ICE1 | ICE0 | EG11 | EG10 | EG01 | EG00 | 00000000$_B$ |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

• Block diagram
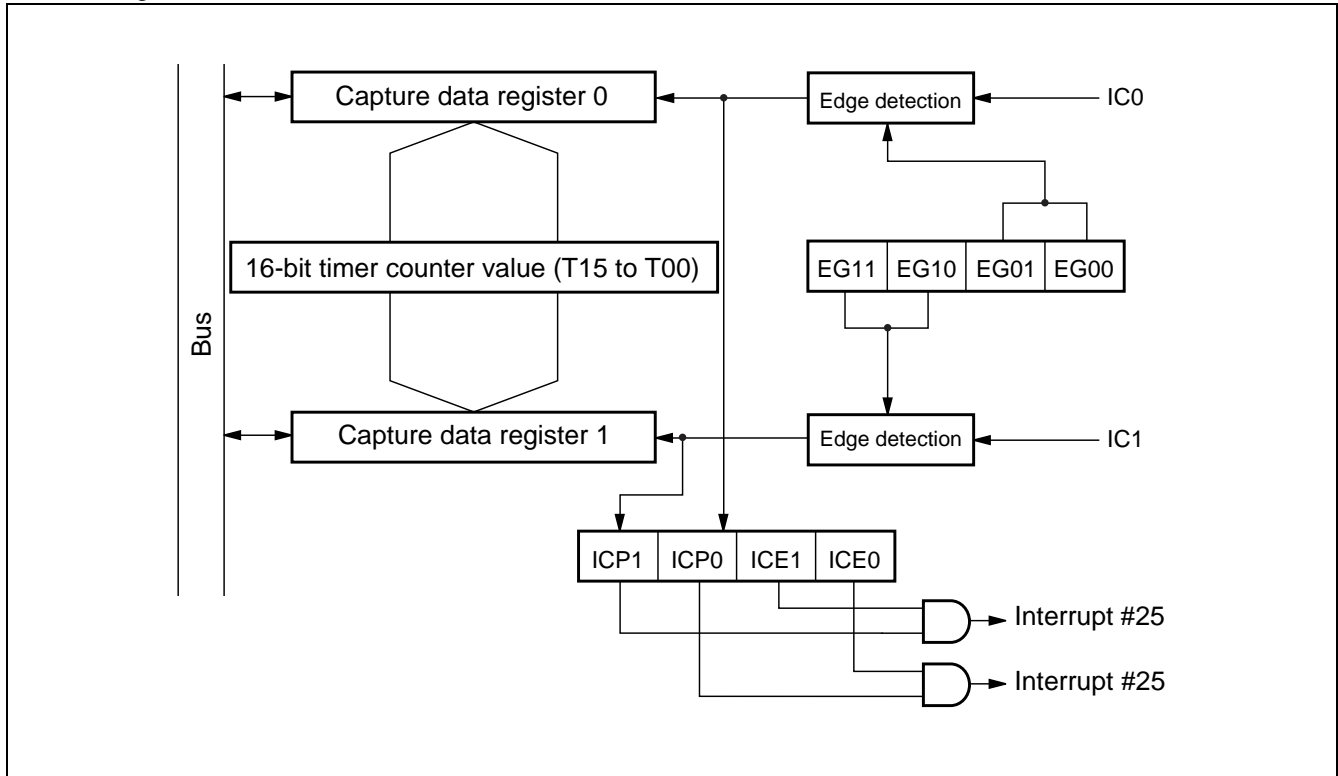
## 10. 16-bit reload timer

The 16-bit reload timer provides two functions either one which can be selected, the internal clock mode that performs the count down by synchronizing with 3-type internal clocks and the event count mode that performs the count down by detecting the arbitration.  This timer defines an underflow as a transition of the count value from $0000_H$ to $FFFF_H$. Therefore, when the equation  (counted value = reload register setting value+1) holds, an underflow occurs. Either mode can be selected for the count operation from the reload mode which repeats the count by reloading the count setting value at the underflow occurrence or the one-shot mode which stops the count at the underflow occurrence. The interrupt can be generated at the counter underflow occurrence so as to correspond to the DTC.

### (1) Register list

• TMCSR Timer control status register
Timer control status register (upper) (TMCSR0H to TMCSR2H)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| $000051_H$ $000055_H$ | — | — | — | — | CSL1 | CSL0 | MOD2 | MOD1 | - - - - $0000_B$ |
| $000059_H$ | — | — | — | — | R/W | R/W | R/W | R/W | Read/Write |

Timer control status register (lower) (TMCSR0L to TMCSR2L)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| $000050_H$ $000054_H$ | MOD0 | OUTE | OUTL | RELD | INTE | UF | CNTE | TRG | $00000000_B$ |
| $000058_H$ | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

• 16-bit timer register/16-bit reload register TMR0 to TMR2/TMRLR0 to TMRLR2 (upper)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| $000053_H$ $000057_H$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | $XXXXXXXX_B$ |
| $00005B_H$ | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

TMR0 to TMR2/TMRLR0 to TMRLR2 (low)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| $000052_H$ $000056_H$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | $XXXXXXXX_B$ |
| $00005A_H$ | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

-   : Unused

**(2) Block diagram**

Internal data bus

TMRLR
16-bit reload register

Reload signal

TMR
16-bit timer register
(down counter)    UF

Reload control
circuit

CLK

Count clock generation circuit

Gate
input

Machine
clock φ

Prescaler    3

Valid clock
identification circuit

Wait signal

Clear

CLK

Output signal
generation circuit

Pin

Input control
circuit

Clock
selector

Re-
verse

Output signal
generation circuit

Pin

EN

External clock

OUTL    RELD    Operation
control circuit

Select
function    3

Select signal    2

OUTE

Timer control status register (TMCSR)

## 11. Watch timer

The watch timer is a 15-bit timer using the subclock. It can generate the interrupt request for each interval time. The watch timer can also be used as the clock source of the watchdog timer by setting so.

### (1) Register list

Watch timer control register (WTC)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| $0000AA_H$ | WDCS | SCE | WTIE | WTOF | WTR | WTC2 | WTC1 | WTC0 | $1X011000_B$ |
| | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

### (2) Block diagram

Watch timer control register (WTC)

| WDCS | SCE | WTIE | WTOF | WTR | WTC2 | WTC1 | WTC0 |
|---|---|---|---|---|---|---|---|

Clear

Sub clock

Watch counter

$2^8$
$2^9$
$2^{10}$
$2^{11}$
$2^{12}$
$2^{13}$
$2^{14}$

$2^{10}$ $2^{13}$ $2^{14}$ $2^{15}$

Interval selector

Interrupt generation circuit

Watch timer interrupt
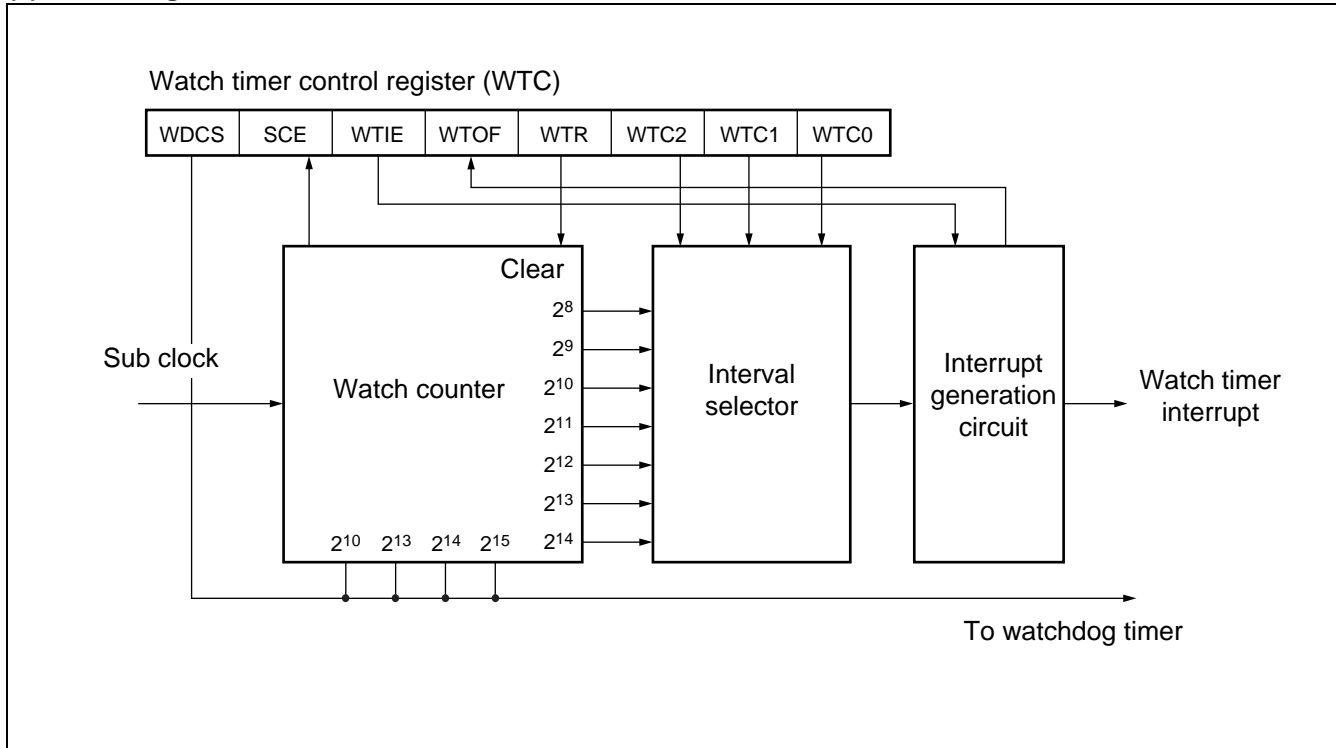
To watchdog timer

## 12. Watchdog timer

The watchdog timer is a timer counter provided for preventing program malfunction. The watchdog timer is a 2-bit counter operating with an output of the timebase timer or watch timer as count clock and resets the CPU when the counter is not cleared within the interval time.

### (1) Register list

Watchdog timer control register (WDTC)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0000A8$_H$ | PONR | — | WRST | ERST | SRST | WTE | WT1 | WT0 |
| | R | — | R | R | R | W | W | W |

Initial Value
XXXXX111$_B$

Read/Write

− : Unused

### (2) Block diagram

Watchdog timer control register (WDTC)

| PONR | — | WRST | ERST | SRST | WTE | WT1 | WT0 |

WDCS bit of watch timer control register (WTO)

SCM bit of clock selection register (CKSCR)

Watch mode start
Time-base timer mode start
Sleep mode start
Hold status start

Watchdog timer

CLR and start-up

CLR

Counter clear control circuit

Count clock selector

2-bit counter

Watchdog reset generation circuit

Internal reset generation circuit

Stop mode start

2

CLR

Clear

4

4

Time base counter

Dividing HCLK by 2

$\times 2^1$ | $\times 2^2$ | $\cdot\cdot$ | $\times 2^8$ | $\times 2^9$ | $\times 2^{10}$ | $\times 2^{11}$ | $\times 2^{12}$ | $\times 2^{13}$ | $\times 2^{14}$ | $\times 2^{15}$ | $\times 2^{16}$ | $\times 2^{17}$ | $\times 2^{18}$

SCLK

$\times 2^1$ | $\times 2^2$ | $\cdot\cdot$ | $\times 2^8$ | $\times 2^9$ | $\times 2^{10}$ | $\times 2^{11}$ | $\times 2^{12}$ | $\times 2^{13}$ | $\times 2^{14}$ | $\times 2^{15}$ | $\times 2^{16}$ | $\times 2^{17}$ | $\times 2^{18}$

HCLK: Oscillation clock
SCLK: Sub clock

## 13. Time-base timer

The time-base timer has a function that enables a selection of four interval times using 18-bit free-run counter (time-base counter) with synchronizing to the internal count clock (two division of original oscillation). Furthermore, the function of timer output of oscillation stabilization wait or function supplying operation clocks for watchdog timer are provided.

### (1) Register list

Timer base timer control register (TBTC)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 0000A9$_H$ | Reserved | — | — | TBIE | TBOF | TBR | TBC1 | TBC0 | 1 - - 00100$_B$ |
| | R/W | — | — | R/W | R/W | W | R/W | R/W | Read/Write |

- : Unused

### (2) Block diagram



To PPG timer

To watchdog timer

Time-base timer counter

Dividing HCLK by 2

$\times 2^1$ | $\times 2^2$ | · · | $\times 2^8$ | $\times 2^9$ | $\times 2^{10}$ | $\times 2^{11}$ | $\times 2^{12}$ | $\times 2^{13}$ | $\times 2^{14}$ | $\times 2^{15}$ | $\times 2^{16}$ | $\times 2^{17}$ | $\times 2^{18}$

OF    OF    OF    OF

Power-on reset
Stop mode start

Counter clear control circuit

To clock controller
Oscillation stabilizing
Wait time selector

Hold status start
CKSCR : MCS = 0*1
CKSCR : SCS = 0→1*2

Interval timer selector

TBOF set

TBOF clear

Time-base timer control register (TBTC)   Reserved | — | — | TBIE | TBOF | TBR | TBC1 | TBC0

Time-base timer interrupt signal

```
—      : Unused
OF     : Overflow
HCLK   : Oscillation clock
*1     : The machine clock is switched from main/sub clock to PLL clock.
*2     : The machine clock is switched from sub clock to main clock.
```

## 14. Clock generator

The clock generator controls operation of the internal clock which is the operation clock for the CPU and peripheral devices. This internal clock is used as machine clock and its one cycle as machine cycle. In addition, the clock generated by original oscillation is used as oscillation clock and that by internal PLL oscillation as PLL clock.

**(1) Register list**

Clock selection register (CKSCR)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 0000A1$_H$ | SCM | MCM | WS1 | WS0 | SCS | MCS | CS1 | CS0 | 11111100$_B$ |
| | R | R | R/W | R/W | R/W | R/W | R/W | R/W | Read/Write |

# MB90800 Series

**(2) Block diagram**

Standby control circuit

Low power consumption mode control register (LPMCR)

| STP | SLP | SPL | RST | TMD | CG1 | CG0 | Reserved |

Pin High-Z control circuit → Pin High-Z control

RST Pin

Internal reset generation circuit → Internal reset

CPU intermittent operation selector → Intermittent cycle selection

CPU clock control circuit → CPU clock

Standby control circuit

Release interrupting

Stop, sleep signal

Stop signal

Peripheral clock control circuit → Peripheral clock

Machine clock

Oscillation stabilization wait

Clock generation block

Clock selector

Oscillation stabilization wait time selector

Dividing by 4 → SCLK

PLL multiplying circuit

| SCM | MCM | WS1 | WS0 | SCS | MCS | CS1 | CS0 |

Clock selection register (CKSCR)

Sub clock generation circuit

X0A Pin

X1A Pin

System clock generation circuit

X0 Pin

X1 Pin

HCLK

MCLK

Dividing by 2

Dividing by 1024

Dividing by 2

Dividing by 4

Dividing by 4

Dividing by 4

Dividing by 2

Time-base timer

To watchdog timer

HCLK : Oscillation clock
MCLK : Main clock
SCLK : Sub clock

**(3) Clock supply map**

```
Clock generation circuit

X0 → Oscillation circuit       Watch timer          Timer clock divider
X1 ←                                                Watchdog timer
                               Selector
X0A → Oscillation circuit                           ┌ Internal resources ┐
X1A ←                          Time-base timer        LCD controller
                                                      16-bit Reload Timer
                                                      8/10-bit A/D converter
                                                      Serial I/O
                                                      Free-run timer
                                                      Input capture

                    1   2   3   4
                    PLL multiplying circuit
                              PCLK
   2 division circuit         Selector              CPU (F²MC-16LX)
   HCLK        MCLK
   2 division circuit    SCLK                       ROM/RAM (memory)
```

HCLK : Oscillation clock
MCLK : Main clock
PCLK : PLL clock
SCLK : Sub clock

## 15. Low power consumption mode

The low-power consumption mode has the following CPU operation modes by selecting the operation clock and operating the control of the clock.
- Clock mode
  (PLL clock mode, main clock mode and sub clock mode)
- CPU intermittent operation mode
  (PLL clock intermittent operation mode, main clock intermittent operation mode and subclock intermittent
   operation mode)
- Standby mode
  (Sleep mode, time base timer mode, stop mode and watch mode)

### (1) Register list

Low power consumption mode control register (LPMCR)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 0000A0$_H$ | STP | SLP | SPL | RST | TMD | CG1 | CG0 | Reserved | 00011000$_B$ |
| | W | W | R/W | W | R/W | R/W | R/W | R/W | Read/Write |

## (2) Block diagram

Standby control circuit

Low power consumption mode control register (LPMCR)

| STP | SLP | SPL | RST | TMD | CG1 | CG0 | Reserved |

Pin High-Z control circuit → Pin High-Z control

RST Pin

Internal reset generation circuit → Internal reset

CPU intermittent operation selector

Intermittent cycle selection

CPU clock control circuit → CPU clock

Standby control circuit

Release of interrupt

Stop, sleep signal

Stop signal

Peripheral clock control → Peripheral clock

Machine clock

Release of oscillation stabilization wait

Clock generation block

Clock selector

Oscillation stabilization wait time selector

Dividing by 4

SCLK

2

2

PLL multiplying circuit

| SCM | MCM | WS1 | WS0 | SCS | MCS | CS1 | CS0 |

Clock selection register (CKSCR)

Sub clock generation circuit

X0A Pin

X1A Pin

System clock generation circuit

Dividing by 2

X0 Pin

X1 Pin

HCLK    MCLK

| Dividing by 1024 | Dividing by 2 | Dividing by 4 | Dividing by 4 | Dividing by 4 | Dividing by 2 |

Time-base timer

To watchdog timer

HCLK    : Oscillation clock
MCLK    : Main clock
SCLK    : Sub clock

**(3) Figure of status transition**

External reset, watchdog timer reset, software reset,

Power supply

Reset

Power-on reset

SCS = 0

SCS = 1

End of oscillation
stabilization wait

Main clock mode

MCS = 0

PLL clock mode

SCS = 0

Sub clock mode

MCS = 1

SCS = 1

SLP = 1    Interrupt

SLP = 1    Interrupt

SLP = 1    Interrupt

Main sleep mode

PLL sleep mode

Sub sleep mode

TMD = 0    Interrupt

TMD = 0    Interrupt

TMD = 0    Interrupt

Time-base
timer mode

Time-base
timer mode

Watch mode

STP = 1

STP = 1

STP = 1

Main stop mode

PLL stop mode

Sub stop mode

Interrupt    End of oscillation
stabilization wait

Interrupt    End of oscillation
stabilization wait

Interrupt    End of oscillation
stabilization wait

Main clock Oscillation
stabilization wait

Main clock Oscillation
stabilization wait

Sub clock Oscillation
stabilization wait

## 16. Timer clock output

The timer clock output circuit divides the oscillation clock by the time-base timer and generates and outputs the set division clock. Selectable from 32/64/128/256 division of the oscillation clock.

The timer clock output circuit is inactive in reset or stop mode. It is active in normal run, sleep, or pseudo-timer mode.

|  | PLL_Run | Main_Run | Sleep | Pseudo clock | STOP | Reset |
|---|---|---|---|---|---|---|
| Operation status | ○ | ○ | ○ | ○ | × | × |

Note : When the time-base timer is cleared while using the timer clock output circuit, the clock is not correctly output. For detail of the time-base timer's clear condition, see the section of time-base timer in the MB90800 Hardware Manual.

**(1) Register list**

Watch clock output control register (TMCS)

| $0000AF_H$ | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
|  | — | — | — | — | — | TEN | TS1 | TS0 |
|  | — | — | — | — | — | R/W | R/W | R/W |

Initial Value
$XXXXX000_B$

Read/Write

- : Unused

**(2) Block diagram**



Timer clock selection circuit
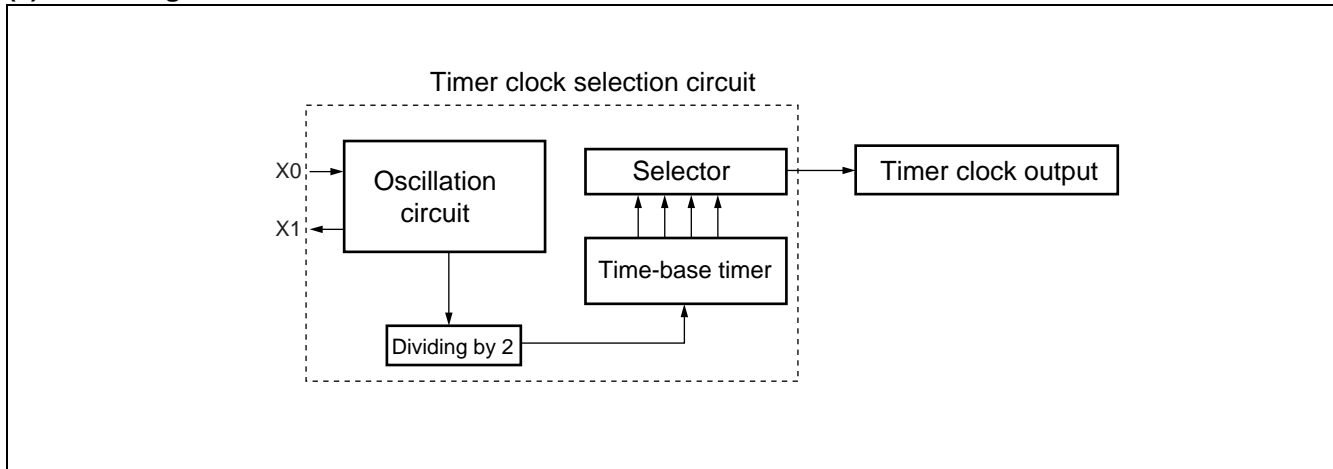
## 17. ROM mirroring function selection module

ROM mirrorring function selection module provides the setting so that ROM data located in FF bank can be read by access to 00 bank.

### (1) Register list

ROM mirror function select register (ROMM)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial Value |
|---|---|---|---|---|---|---|---|---|---|
| 00006F$_H$ | — | — | — | — | — | — | — | MI | XXXXXXX1$_B$ |
| | — | — | — | — | — | — | — | R/W | Read/Write |

- : Unused

### (2) Block diagram
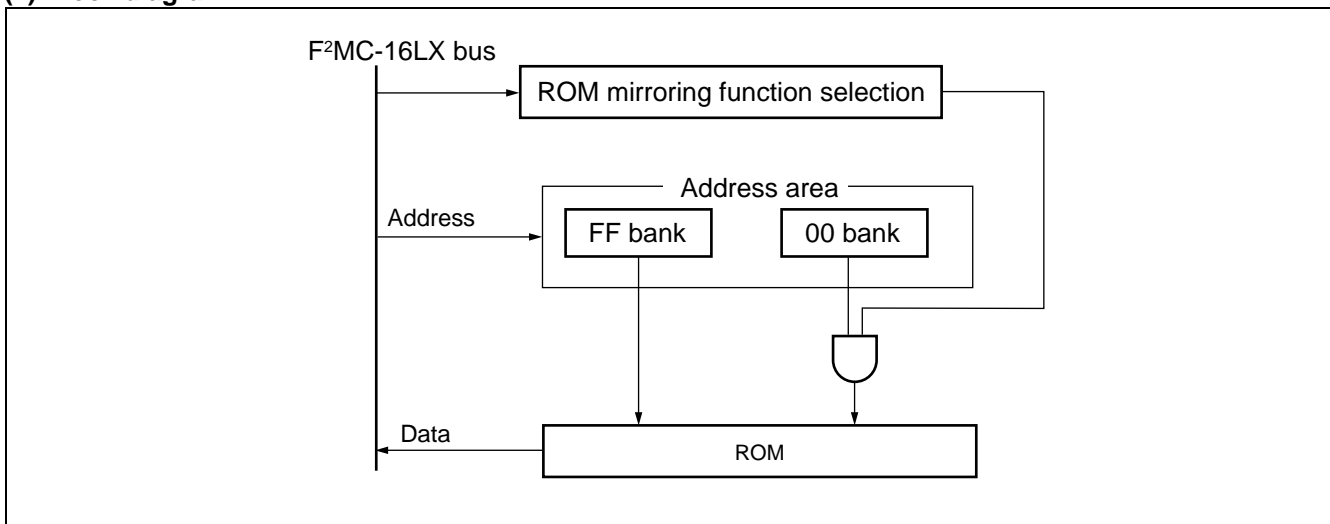


Note : Do not access to ROM mirroring function selection register in the middle of the operation of the address 008000$_H$ to 00FFFF$_H$.

## 18. Interrupt controller

Interrupt control register is in the interrupt controller. The register corresponds to all I/O of interrupt function. The register has following functions;
• Setting of Interrupt level at correspondent peripheral circuit.

### (1) Register list (at writing)

Interrupt control register                                                                     Initial Value

Address :
   ICR01  0000B1$_H$
   ICR03  0000B3$_H$
   ICR05  0000B5$_H$
   ICR07  0000B7$_H$
   ICR09  0000B9$_H$
   ICR11  0000BB$_H$
   ICR13  0000BD$_H$
   ICR15  0000BF$_H$

| bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----|------|------|------|------|-----|-----|-----|-----|
|     | ICS3 | ICS2 | ICS1 | ICS0 | ISE | IL2 | IL1 | IL0 |
|     | W | W | W | W | R/W | R/W | R/W | R/W |

00000111$_B$

Read/Write

Interrupt control register                                                                     Initial Value

Address :
   ICR00  0000B0$_H$
   ICR02  0000B2$_H$
   ICR04  0000B4$_H$
   ICR06  0000B6$_H$
   ICR08  0000B8$_H$
   ICR10  0000BA$_H$
   ICR12  0000BC$_H$
   ICR14  0000BE$_H$

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|------|------|------|------|-----|-----|-----|-----|
|     | ICS3 | ICS2 | ICS1 | ICS0 | ISE | IL2 | IL1 | IL0 |
|     | W | W | W | W | R/W | R/W | R/W | R/W |

00000111$_B$

Read/Write

Note : Do not access using read modify write instruction because it causes the malfunction.

**(2)Register list (at reading)**

Interrupt control register                                                    Initial Value

Address :
ICR01    0000B1H
ICR03    0000B3H
ICR05    0000B5H
ICR07    0000B7H
ICR09    0000B9H
ICR11    0000BBH
ICR13    0000BDH
ICR15    0000BFH

| bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|-----|----|----|----|----|----|----|----|----|
|  | — | — | S1 | S0 | ISE | IL2 | IL1 | IL0 |

- - 000111B

Read/Write              —     —     R     R     R/W   R/W   R/W   R/W        Read/Write
Initial Value


Interrupt control register                                                    Initial Value

Address :
ICR00    0000B0H
ICR02    0000B2H
ICR04    0000B4H
ICR06    0000B6H
ICR08    0000B8H
ICR10    0000BAH
ICR12    0000BCH
ICR14    0000BEH

| bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|
|  | — | — | S1 | S0 | ISE | IL2 | IL1 | IL0 |
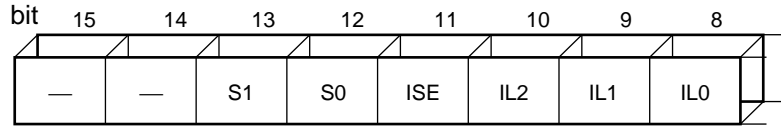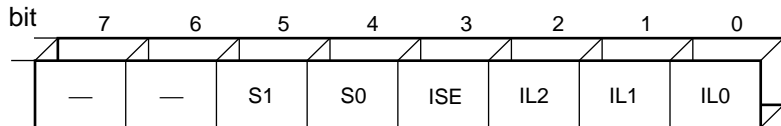
- - 000111B

Read/Write              —     —     R     R     R/W   R/W   R/W   R/W        Read/Write
Initial Value

- : Unused

Note : Do not access using read modify write instruction because it causes the malfunction.

**(3) Block diagram**
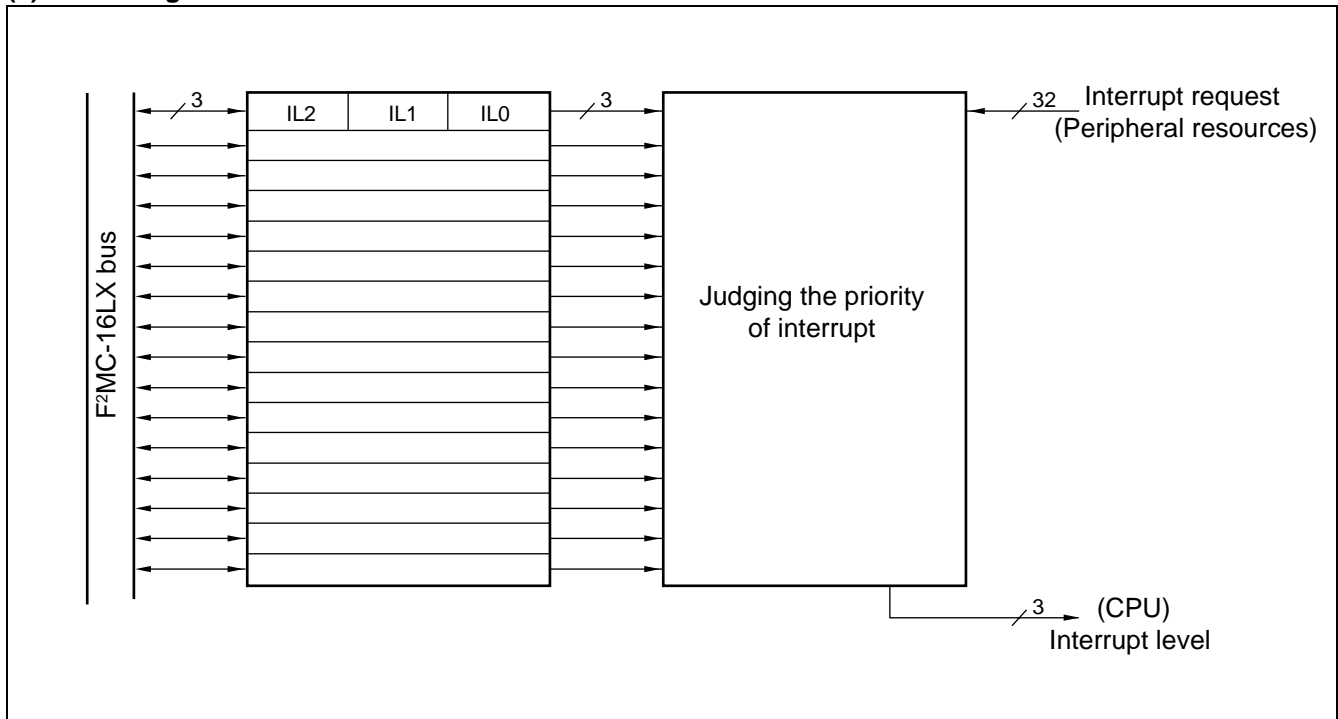
## 19. LCD controller/driver

The LCD controller/driver contains 24 × 8-bit display data memory and controls the LCD display with four common output lines and 48 segment output lines. Three duty outputs can be selected to directly drive the LCD panel (liquid crystal display).
- Contains an LCD driving voltage split resistor. Moreover, the external division resistance can be connected.
- A maximum of four common output lines (COM0 to COM3) and 48 segment output lines (SEG0 to SEG47) are available.
- Contains 24-byte display data memory (display RAM).
- For the duty, 1/2, 1/3, or 1/4 can be selected (restricted by bias setting).
- The LCD can directly be driven.

| Bias | 1/2 duty | 1/3 duty | 1/4 duty |
|---|---|---|---|
| 1/2 bias | ○ | × | × |
| 1/3 bias | × | ○ | ○ |

○ : Recommended mode

× : Disable

### (1) Register list

• LCR (LCD control register)
LCD control register (higher) (LCRH)

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| 00005D$_H$ | SS4 | VS0 | CS1 | CS0 | SS3 | SS2 | SS1 | SS0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial Value
00000000$_B$
Read/Write

LCD control register (lower) (LCRL)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 00005C$_H$ | CSS | LCEN | VSEL | BK | MS1 | MS0 | FP1 | FP0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial Value
00010000$_B$
Read/Write

• LCDC range register (LCRR)

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 00005E$_H$ | Reserved | Reserved | SE4 | SE3 | SE2 | SE1 | SE0 | LCR |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial Value
00000000$_B$
Read/Write

**(2) Block diagram**
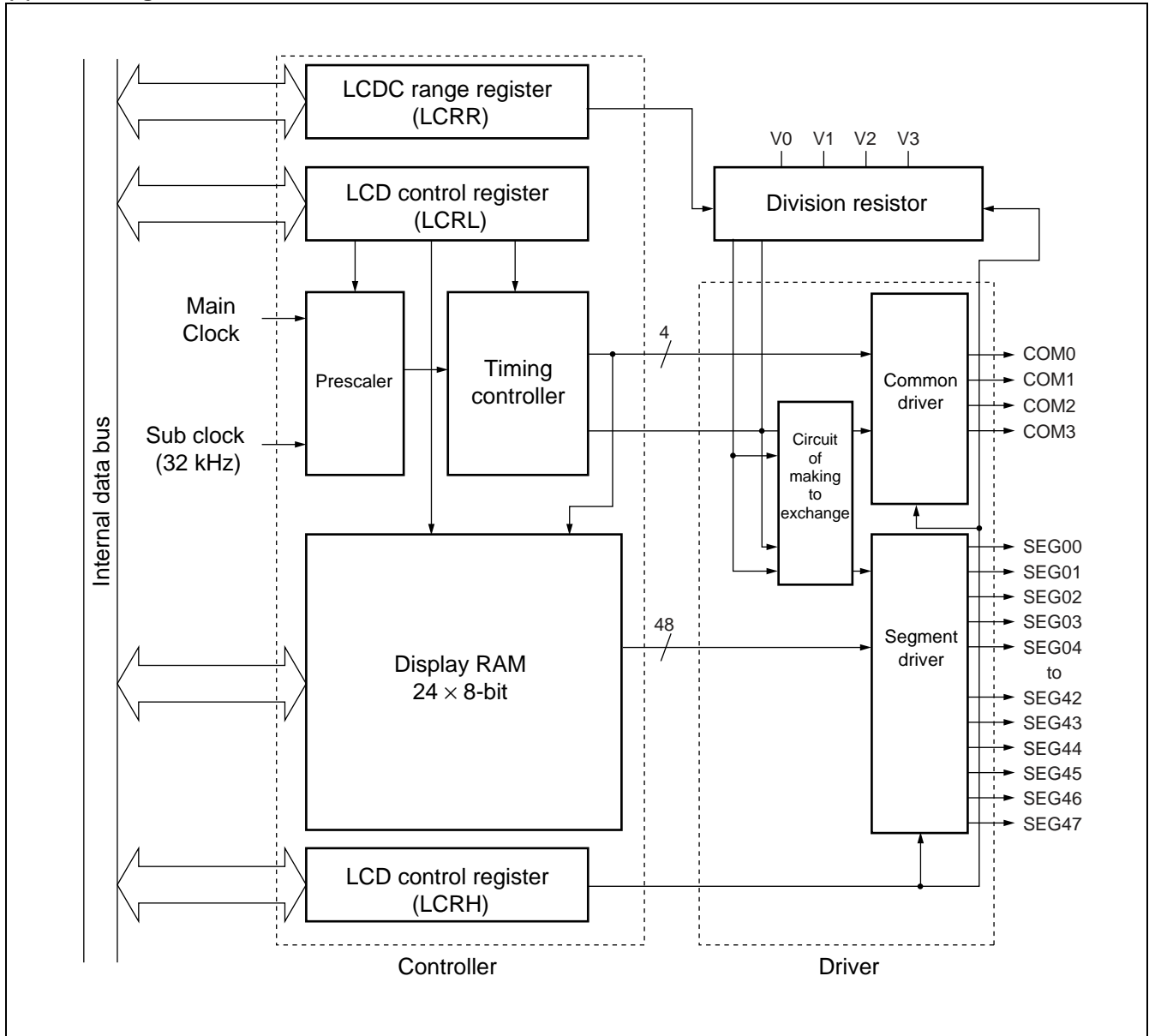
## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
| --- | --- | --- | --- | --- | --- |
| | | Min | Max | | |
| Power supply voltage[1] | $V_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | |
| | $AV_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | $V_{CC} \geq AV_{CC}$[2] |
| Input voltage[1] | $V_I$ | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | [3] |
| | | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | N-ch open-drain (5 V withstand voltageI/O) [4] |
| Output voltage[1] | $V_O$ | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | [3] |
| "L" level maximum output current | $I_{OL11}$ | — | 10 | mA | Other than P74, P75, P40 to P47[5] |
| | $I_{OL12}$ | — | 30 | mA | P74, P75, P40 to P47 (Heavy-current output port) [5] |
| "L" level average output current | $I_{OLAV1}$ | — | 3 | mA | Other than P74, P75, P40 to P47[6] |
| | $I_{OLAV2}$ | — | 15 | mA | P74, P75, P40 to P47 (Heavy-current output port) [6] |
| "L" level maximum total output current | $\Sigma I_{OL}$ | — | 120 | mA | |
| "L" level average total output current | $\Sigma I_{OLAV}$ | — | 60 | mA | [7] |
| "H" level maximum output current | $I_{OH11}$ | — | $-10$ | mA | Other than P74, P75, P40 to P47[5] |
| | $I_{OH12}$ | — | $-12$ | mA | P40 to P47 (Heavy-current output port) [5] |
| "H" level average output current | $I_{OHAV}$ | — | $-3$ | mA | [6] |
| "H" level maximum total output current | $\Sigma I_{OH}$ | — | $-120$ | mA | |
| "H" level average total output current | $\Sigma I_{OHAV}$ | — | $-60$ | mA | [7] |
| Power consumption | Pd | — | 351 | mW | |
| Operating temperature | $T_A$ | $-40$ | $+85$ | °C | |
| Storage temperature | $T_{STG}$ | $-55$ | $+150$ | °C | |

[1] : The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

[2] : $AV_{CC}$ should not be exceeding $V_{CC}$ at power-on etc.

[3] : $V_I$, $V_O$, should not exceed $V_{CC} + 0.3$ V.

[4] : Applicable to pins : P74, P75

[5] : A peak value of an applicable one pin is specified as a maximum output current.

[6] : An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

[7] : An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

WARNING:    Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

$( V_{SS} = AV_{SS} = 0.0$ V$)$

| Parameter | Symbol | Value | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage | $V_{CC}$ | 2.7 | 3.6 | V | At normal operating |
| | | 1.8 | 3.6 | V | Stop operation state maintenance |
| "H" level input voltage | $V_{IH}$ | 0.7 $V_{CC}$ | $V_{CC}$ + 0.3 | V | CMOS input pin |
| | $V_{IHS}$ | 0.8 $V_{CC}$ | $V_{CC}$ + 0.3 | V | CMOS hysteresis input pin (Resisting pressure of 5 V is $V_{CC}$ = 5.0 V) |
| | $V_{IHM}$ | $V_{CC}$ – 0.3 | $V_{CC}$ + 0.3 | V | MD pin input |
| "L" level input voltage | $V_{IL}$ | $V_{SS}$ – 0.3 | 0.3 $V_{CC}$ | V | CMOS input pin |
| | $V_{ILS}$ | $V_{SS}$ – 0.3 | 0.2 $V_{CC}$ | V | CMOS hysteresis input pin |
| | $V_{ILM}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 0.3 | V | MD pin input |
| Operating temperature | $T_A$ | – 40 | + 85 | °C | |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## 3. DC Characteristics
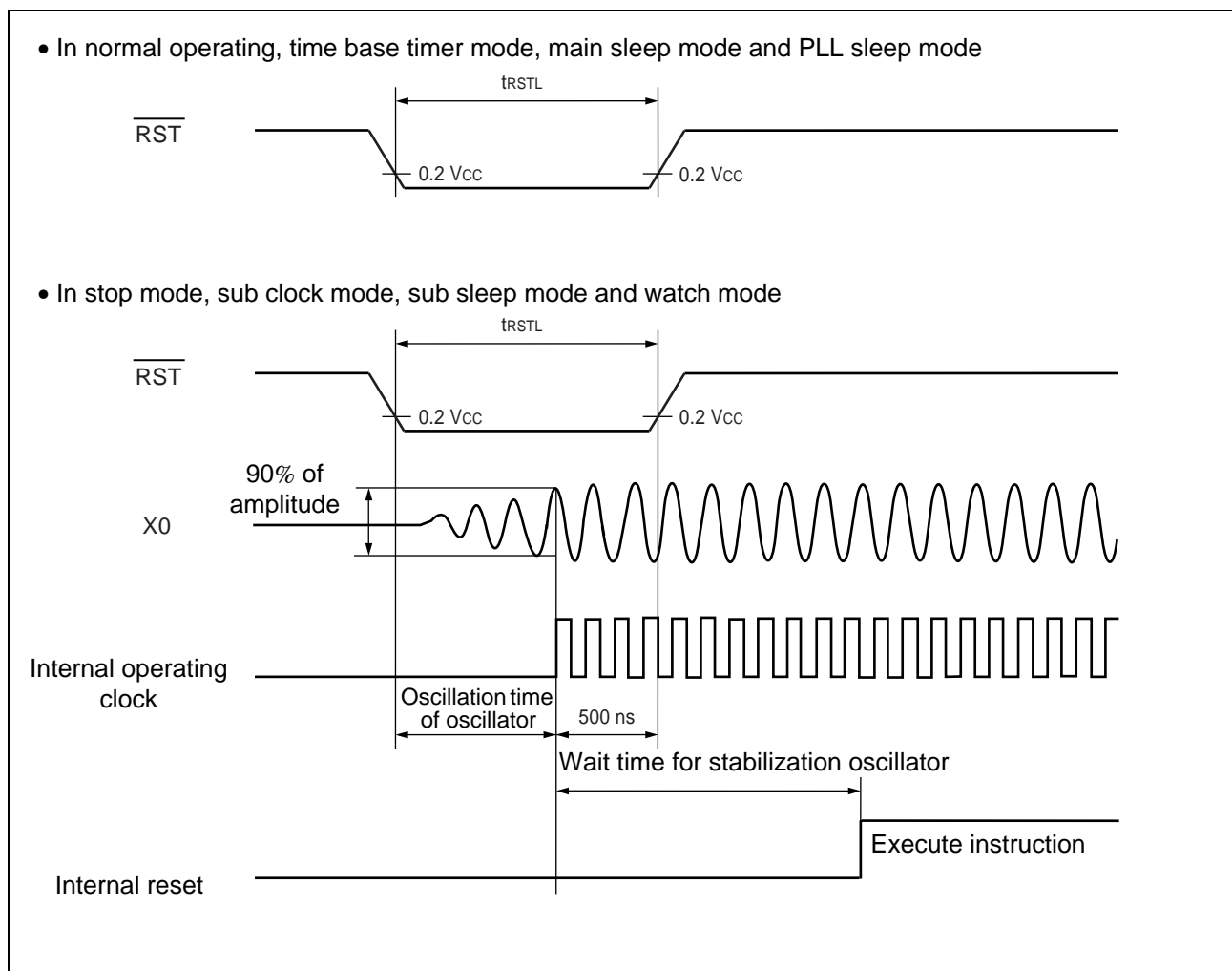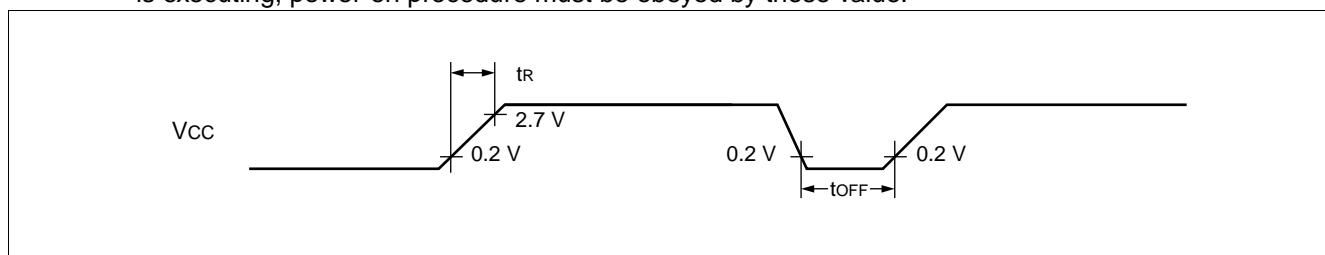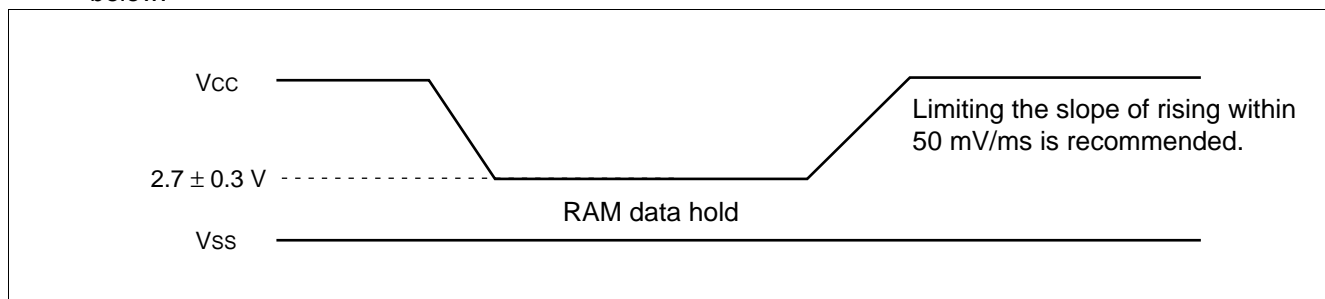
$(V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ }^{\circ}\text{C to} + 85 \text{ }^{\circ}\text{C})$

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level output voltage | $V_{OH}$ | Output pins other than P40 to P47, P74, P75 | $I_{OH} = -4.0$ mA | $V_{CC} - 0.5$ | — | Vcc | V | |
| | $V_{OH1}$ | P40 to P47 | $I_{OH} = -8.0$ mA | $V_{CC} - 0.5$ | — | Vcc | V | Heavy-current output port |
| "L" level output voltage | $V_{OL}$ | Output pins other than P40 to P47, P74, P75 | $I_{OL} = 4.0$ mA | Vss | — | Vss + 0.4 | V | |
| | $V_{OL1}$ | P40 to P47 | $I_{OL} = 15.0$ mA | Vss | — | Vss + 0.6 | V | Heavy-current output port |
| | $V_{OL2}$ | P74, P75 | $I_{OL} = 15.0$ mA | — | 0.5 | Vss + 0.8 | V | Open-drain pin |
| Open-drain output application voltage | $V_{D1}$ | P74, P75 | — | Vss − 0.3 | — | Vss + 5.5 | V | |
| Input leak current | $I_{IL}$ | All output pin | $V_{CC} = 3.3$ V, $V_{SS} < V_I < V_{CC}$ | − 10 | — | + 10 | μA | |
| Pull-up resistor | $R_{UP}$ | $\overline{RST}$ | $V_{CC} = 3.3$ V, $T_A = +25$ °C | 25 | 50 | 100 | kΩ | |
| Pull-down resistor | $R_{DOWN}$ | MD2 | $V_{CC} = 3.3$ V, $T_A = +25$ °C | 25 | 50 | 100 | kΩ | Except FLASH memory products |
| Open drain output current | $I_{leak}$ | P74, P75 | — | — | 0.1 | 10 | μA | |
| Power supply current | $I_{CC}$ | Vcc | $V_{CC} = 3.3$ V, Internal frequency 25 MHz At normal operating | — | 48 | 60 | mA | |
| | | | $V_{CC} = 3.3$ V, Internal frequency 25 MHz At Flash writing | — | 60 | 75 | mA | FLASH memory products |
| | | | $V_{CC} = 3.3$ V, Internal frequency 25 MHz At Flash erasing | — | 60 | 75 | mA | FLASH memory products |
| | $I_{CCS}$ | | $V_{CC} = 3.3$ V, Internal frequency 25 MHz at sleep mode | — | 22.5 | 30 | mA | |

*(Continued)*

*(Continued)*

$(V_{CC} = AV_{CC} = 3.3\ V \pm 0.3\ V,\ V_{SS} = AV_{SS} = 0.0\ V,\ T_A = -40\ °C\ to +85\ °C)$

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CCTS}$ | $V_{CC}$ | $V_{CC} = 3.3\ V$, Internal frequency 3 MHz at timer mode | — | 0.75 | 7 | mA | |
| | $I_{CCL}$ | | $V_{CC} = 3.3\ V$, Internal frequency 8 kHz at subclock operation, $(T_A = +25\ °C)$ | — | 15 | 140 | µA | MASK ROM products |
| | | | | — | 0.5 | 0.9 | mA | FLASH memory products |
| | $I_{CCLS}$ | | $V_{CC} = 3.3\ V$, Internal frequency 8 kHz at subclock sleep operation, $(T_A = +25\ °C)$ | — | 23 | 40 | µA | |
| | $I_{CCT}$ | | $V_{CC} = 3.3\ V$, Internal frequency 8 kHz at watch mode $(T_A = +25\ °C)$ | — | 1.8 | 40 | µA | |
| | $I_{CCH}$ | | At Stop mode, $(T_A = +25\ °C)$ | — | 0.8 | 40 | µA | |
| LCD division resistance | $R_{LCD}$ | $V_{CC} - V3$ | At LCR = 0 setting | 100 | 200 | 400 | kΩ | * |
| | | $V_{CC} - V3$ | At LCR = 1 setting | 12.5 | 25 | 50 | | |
| | | V0 – V1, V1 – V2, V2 – V3 | At LCR = 0 setting | 50 | 100 | 200 | | |
| | | V0 – V1, V1 – V2, V2 – V3 | At LCR = 1 setting | 6.25 | 12.5 | 25 | | |
| COM0 to COM3 output impedance | $R_{VCOM}$ | COM0 to COM3 | V1 to V3 = 3.3 V | — | — | 2.5 | kΩ | |
| SEG00 to SEG47 output impedance | $R_{VSEG}$ | SEG00 to SEG47 | | — | — | 15 | kΩ | |
| LCD leak current | $I_{LCDC}$ | V0 to V3, COM0 to COM3, SEG00 to SEG47 | — | – 5 | — | + 5 | µA | |

* : LCD internal divided resistor can be select two type resistor by internal divided resistor selecting bit (LCR) of LCDC range register (LCRR) .

## 4. AC Characteristics

### (1) Clock timing

$(V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

| Parameter | Symbol | Pin name | Conditions | Value Min | Value Typ | Value Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Clock frequency | $f_{CH}$ | X0, X1 | — | 3 | | 16 | MHz | External crystal oscillation |
| | $f_{CH}$ | | | 3 | | 16 | | $\times 1/2$ (at PLL stop) At oscillation circuit |
| | | | | 4 | | 16 | | Multiply by 1 At oscillation circuit |
| | | | | 4 | | 12.5 | | Multiply by 2 At oscillation circuit |
| | | | | 4 | | 8.33 | | Multiply by 3 At oscillation circuit |
| | | | | 4 | — | 6.25 | | Multiply by 4 At oscillation circuit |
| | | X0 | | 3 | | 25 | | $\times 1/2$ (at PLL stop) At external clock |
| | | | | 4 | | 25 | | Multiply by 1 At external clock |
| | | | | 4 | | 12.5 | | Multiply by 2 At external clock |
| | | | | 4 | | 8.33 | | Multiply by 3 At external clock |
| | | | | 4 | | 6.25 | | Multiply by 4 At external clock |
| | $f_{CL}$ | X0A, X1A | | — | 32.768 | — | kHz | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | | 40 | — | 333 | ns | |
| | $t_{LCYL}$ | X0A, X1A | | — | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$ $P_{WL}$ | X0 | | 5 | — | — | ns | Set duty ratio 50% ± 3% |
| | $P_{WLH}$ $P_{WLL}$ | X0A | | — | 15.2 | — | µs | Set duty ratio at 30% to 70% as a guideline. |
| Input clock rise time and fall time | tcr tcf | X0 | | — | — | 5 | ns | At external clock |
| Internal operating clock frequency | $f_{CP}$ | — | | 1.5 | — | 25 | MHz | When main clock is used |
| | $f_{CP1}$ | — | | — | 8.192 | — | kHz | When sub clock is used |
| Internal operating clock cycle time | $t_{CP}$ | — | | 40 | — | 666 | ns | When main clock is used |
| | $t_{CP1}$ | — | | — | 122.1 | — | µs | When sub clock is used |

• X0, X1 clock timing

$t_C$

$P_{WH}$  $P_{WL}$

$t_{cf}$  $t_{cr}$

0.8 $V_{CC}$
0.2 $V_{CC}$
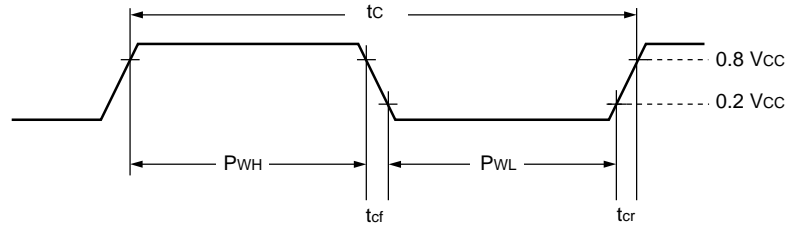
• X0A, X1A clock timing

$t_{CL}$

$P_{WLH}$  $P_{WLL}$

$t_{cf}$  $t_{cr}$

0.8 $V_{CC}$
0.2 $V_{CC}$
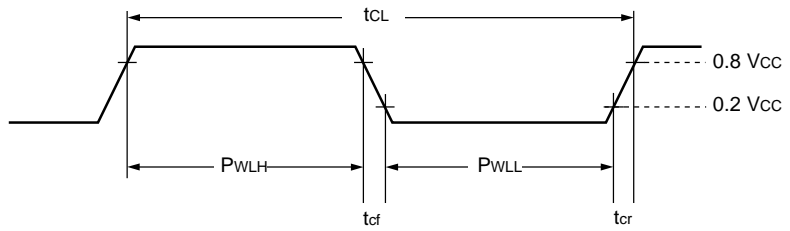
• PLL operation guarantee range

   Relation between internal operation clock frequency and power supply voltage
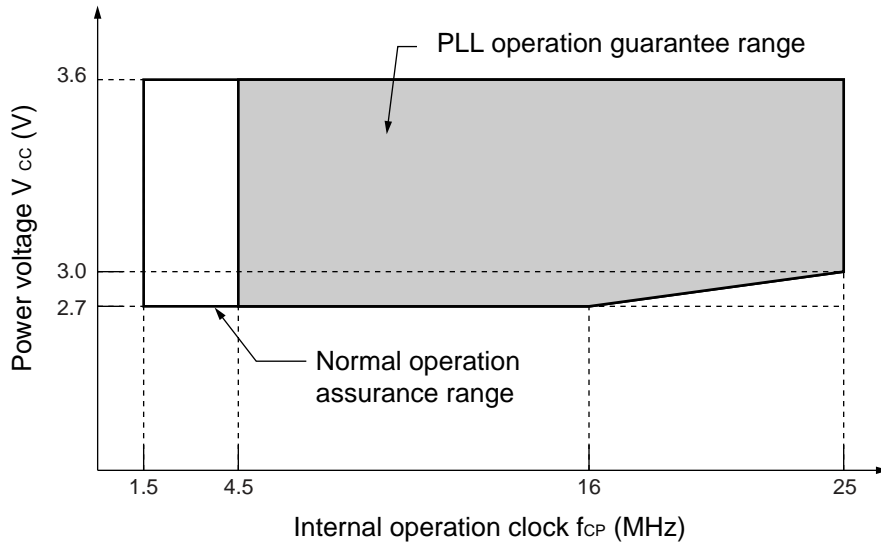


Relation between oscillation clock frequency and internal operating clock frequency
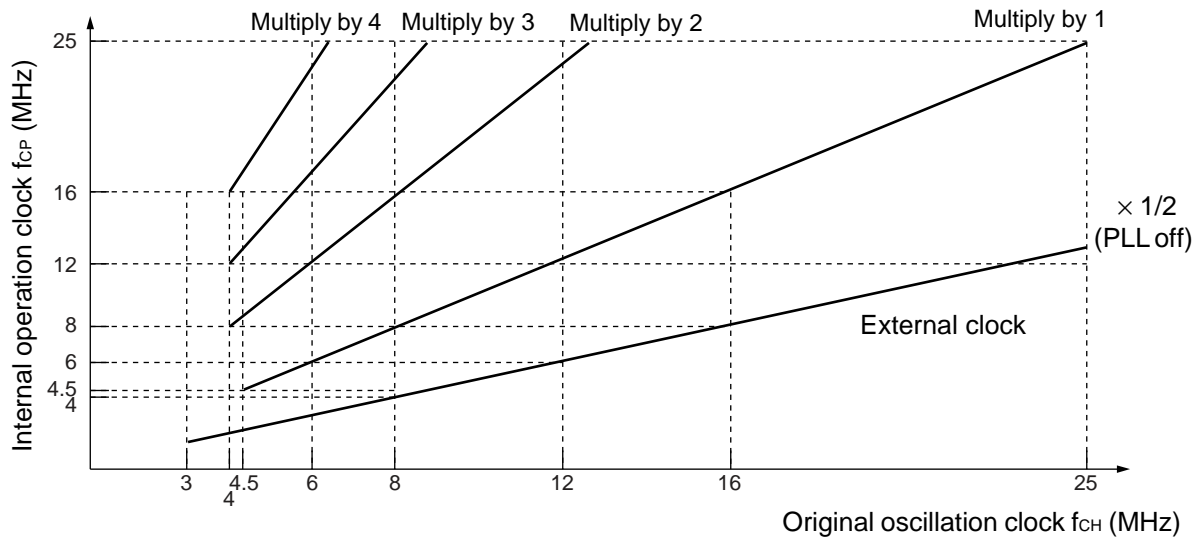


Rating values of alternating current is defined by the measurement reference voltage values shown below :

• Input signal waveform

Hysteresis input pin
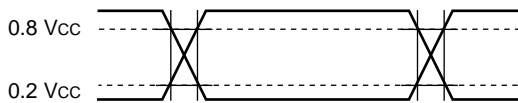


• Output signal waveform

Output pin
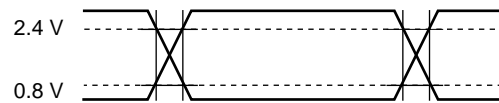
## (2) Reset input timing

$(V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to} + 85 \text{ °C})$

| Parameter | Sym-bol | Pin name | Condi-tions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | — | 500 | — | ns | At normal operating, at time base timer mode, at main sleep mode, at PLL sleep mode |
| | | | | Oscillation time of oscillator*+ 500 ns | — | µs | At stop mode, at sub clock mode, at sub sleep mode, at watch mode |

* : Oscillation time of oscillator is time until oscillation reaches 90% of amplitude. It takes several milliseconds to several dozens of milliseconds on a crystal oscillator, several hundreds of microseconds to several milliseconds on a FAR/ceramic oscillator, and 0 milliseconds on an external clock.



• In normal operating, time base timer mode, main sleep mode and PLL sleep mode

$\overline{RST}$    $t_{RSTL}$    0.2 $V_{CC}$    0.2 $V_{CC}$

• In stop mode, sub clock mode, sub sleep mode and watch mode

$\overline{RST}$    $t_{RSTL}$    0.2 $V_{CC}$    0.2 $V_{CC}$

X0    90% of amplitude

Internal operating clock    Oscillation time of oscillator    500 ns

Wait time for stabilization oscillator

Execute instruction

Internal reset

**(3) Power-on reset**

$(V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 °C \text{ to} + 85 °C)$

| Parameter | Symbol | Pin name | Condi-tions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power supply rising time | $t_R$ | $V_{CC}$ | — | — | 30 | ms | At normal operating |
| Power supply shutdown time | $t_{OFF}$ | $V_{CC}$ | | 1 | — | ms | Wait time until power on |

Notes :  • $V_{CC}$ should be set under  0.2 V before power-on rising up.
  • These value are for power-on reset.
  • In the device, there are internal registers which is initialized only by a power-on reset. If these initialization is executing, power-on procedure must be obeyed by these value.



Note :  Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below.

**(4) Serial I/O**

$(V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40 \text{ °C to } +85 \text{ °C})$

| Parameter | Symbol | Pin name | Conditions | Value Min | Value Max | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Serial clock cycle time | $t_{SCYC}$ | SC0 to SC3 | Internal shift clock mode output pin : $C_L$ = 80 pF + 1TTL | 8 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SC0 to SC3, SO0 to SO3 | | −80 | 80 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SC0 to SC3, SI0 to SI3 | | 100 | — | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIX}$ | | | 60 | — | ns | |
| Serial clock H pulse width | $t_{SHSL}$ | SC0 to SC3 | External shift clock mode output pin : $C_L$ = 80 pF + 1TTL | 4 $t_{CP}$ | — | ns | |
| Serial clock L pulse width | $t_{SLSH}$ | | | 4 $t_{CP}$ | — | ns | |
| SCK ↓ → SOT delay time | $t_{SLOV}$ | SC0 to SC3, SO0 to SO3 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | $t_{IVSH}$ | SC0 to SC3, SI0 to SI3 | | 60 | — | ns | |
| SCK ↑ → valid SIN hold time | $t_{SHIX}$ | | | 60 | — | ns | |

Notes :  • The above rating is in CLK synchronous mode.
 • $C_L$ is a load capacitance value on pins for testing.
 • $t_{CP}$ is machine cycle frequency (ns) . Refer to " (1) Clock timing".
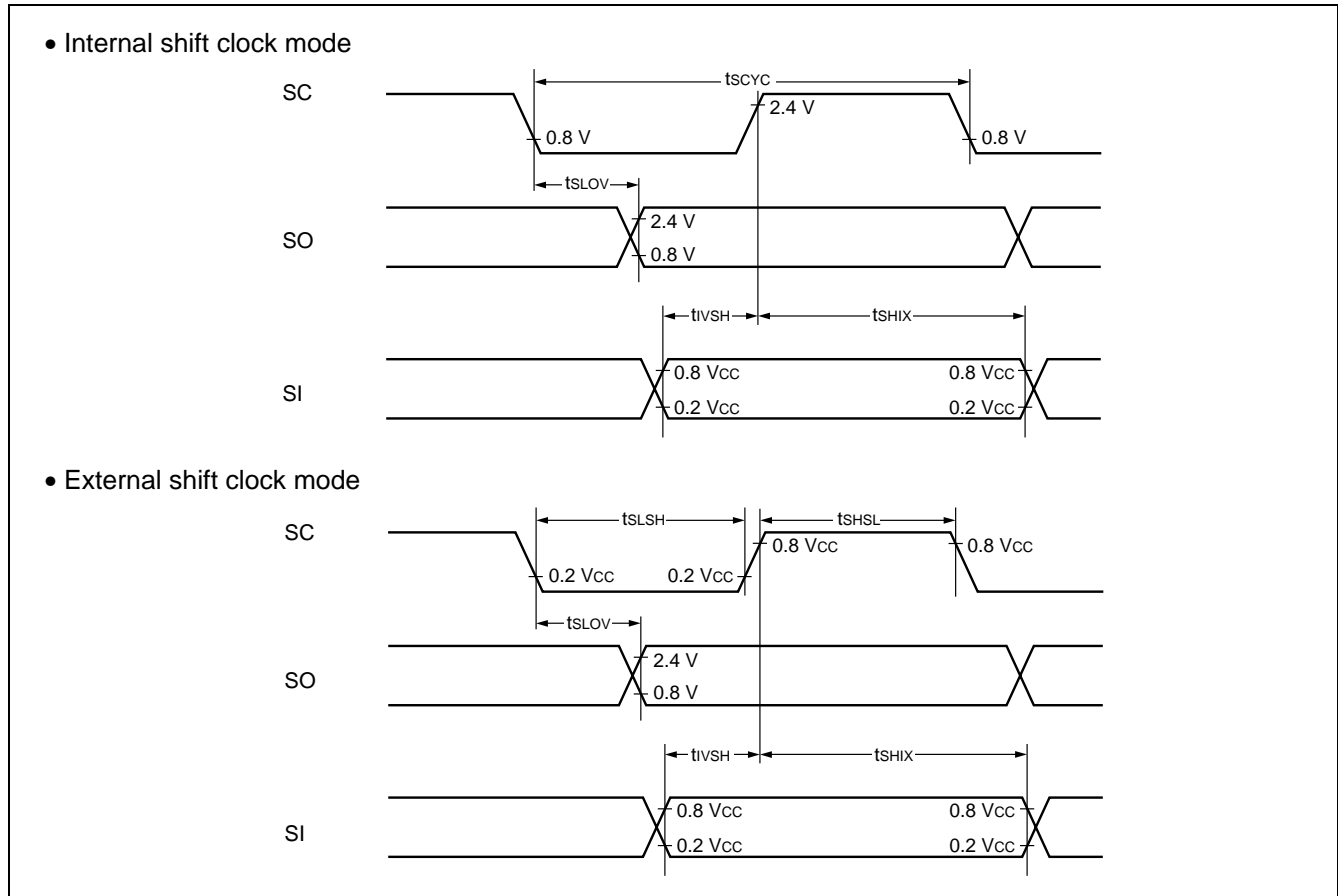
**(5) Timer input timing**

$(V_{CC} = AV_{CC} = 3.3\ V \pm 0.3\ V, V_{SS} = AV_{SS} = 0.0\ V, T_A = -40\ °C\ to + 85\ °C)$

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$ $t_{TIWL}$ | TIN0 to TIN2, IC0, IC1 | — | $4\ t_{CP}$ | — | ns | |

Note : $t_{CP}$ is machine cycle frequency (ns) . Refer to " (1) Clock timing".
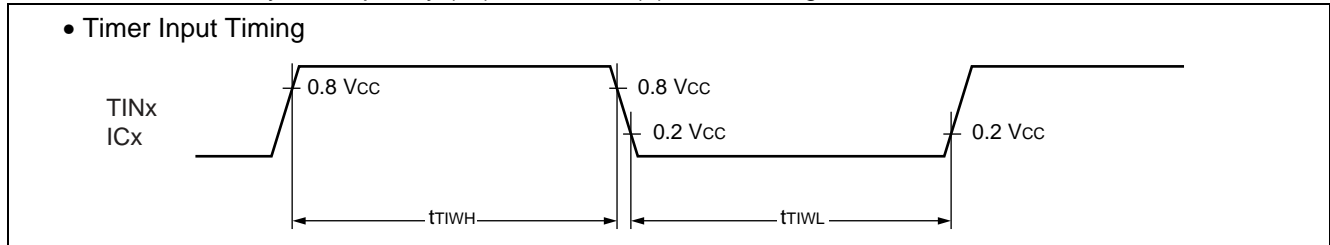
- Timer Input Timing



**(6) Timer output timing**

$(V_{CC} = AV_{CC} = 3.3\ V \pm 0.3\ V, V_{SS} = AV_{SS} = 0.0\ V, T_A = -40\ °C\ to + 85\ °C)$

| Parameter | Sym-bol | Pin name | Condi-tions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| CLK $\uparrow \rightarrow T_{OUT}$ change time | $t_{TO}$ | TOT0 to TOT2, PPG0, PPG1, OCU0, OCU1 | — | 30 | — | ns | |

- Timer Output Timing
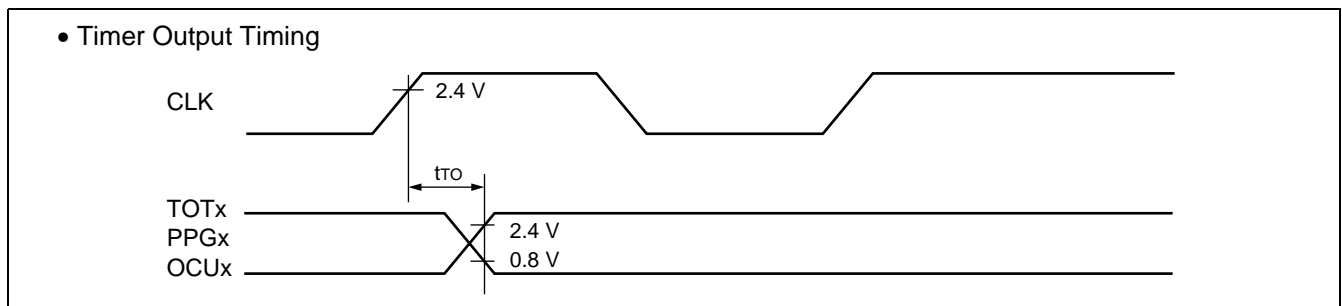


**(7) Trigger input timing**

$(V_{CC} = AV_{CC} = 3.3\ V \pm 0.3\ V, V_{SS} = AV_{SS} = 0.0\ V, T_A = -40\ °C\ to + 85\ °C)$

| Parameter | Symbol | Pin name | Condi-tions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$ $t_{TRGL}$ | INT0 to INT3 | — | $5\ t_{CP}$ | — | ns | At normal operating |
| | | | | 1 | — | µs | In Stop mode |

Note : $t_{CP}$ is machine cycle frequency (ns) . Refer to " (1) Clock timing".

- Trigger Input Timing
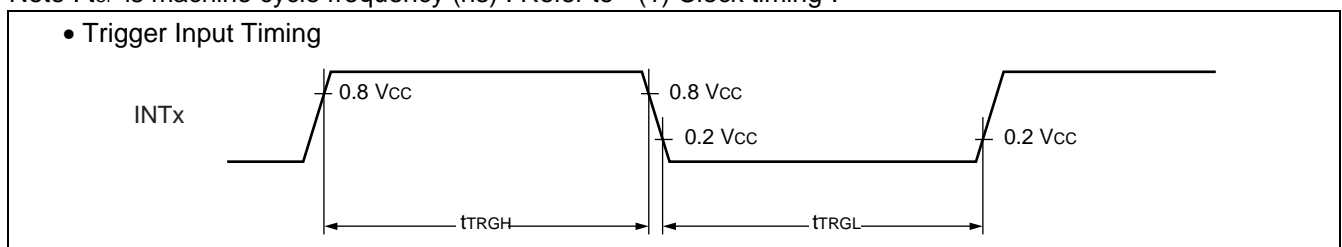
## (8) I²C timing

$(AV_{CC} = V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = - 40 \text{ °C to} + 85 \text{ °C})$

| Parameter | Symbol | Conditions | Standard-mode Min | Standard-mode Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | When power supply voltage of external pull-up resistor is 5.0 V R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V R = 1.0 kΩ, C = 50 pF*2 | 0 | 100 | kHz |
| Hold time (repeated) START condition SDA ↓ → SCL ↓ | $t_{HDSTA}$ | | 4.0 | — | µs |
| "L" width of the SCL clock | $t_{LOW}$ | | 4.7 | — | µs |
| "H" width of the SCL clock | $t_{HIGH}$ | | 4.0 | — | µs |
| Set-up time for a repeated START condition SCL ↑ → SDA ↓ | $t_{SUSTA}$ | | 4.7 | — | µs |
| Data hold time SCL ↓ → SDA ↓ ↑ | $t_{HDDAT}$ | | 0 | 3.45 *3 | µs |
| Data set-up time SDA ↓ ↑ → SCL ↑ | $t_{SUDAT}$ | When power supply voltage of external pull-up resistor is 5.0 V $f_{CP}$*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V $f_{CP}$*1 ≤ 20 MHz, R = 1.0 kΩ, C = 50 pF*2 | 250 *4 | — | ns |
| | | When power supply voltage of external pull-up resistor is 5.0 V $f_{CP}$*1 > 20 MHz, R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V $f_{CP}$*1 > 20 MHz, R = 1.0 kΩ, C = 50 pF*2 | 200 *4 | — | ns |
| Set-up time for STOP condition SCL ↑ → SDA ↑ | $t_{SUSTO}$ | When power supply voltage of external pull-up resistor is 5.0 V R = 1.0 kΩ, C = 50 pF*2 When power supply voltage of external pull-up resistor is 3.6 V R = 1.0 kΩ, C = 50 pF*2 | 4.0 | — | µs |
| Bus free time between a STOP and START condition | $t_{BUS}$ | | 4.7 | — | µs |

*1 : $f_{CP}$ is internal operation clock frequency. Refer to " (1) Clock timing".

*2 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*3 : The maximum $t_{HDDAT}$ only has to be met if the device does not stretch the "L" width ($t_{LOW}$) of the SCL signal.

*4 : Refer to "• Note of SDA and SCL set-up time".

• Note of SDA and SCL set-up time



SDA

Input data set-up time

SCL

6 tcp
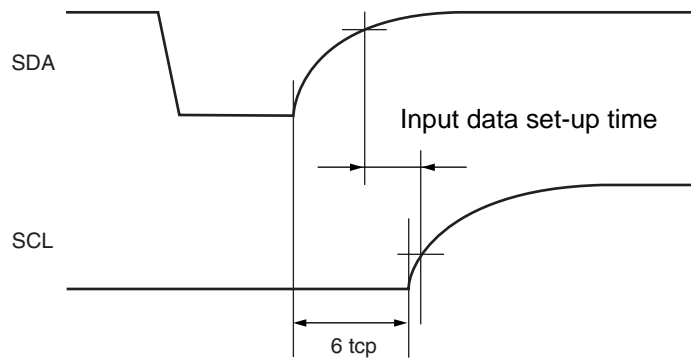
Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.

• Timing definition



SDA

$t_{BUS}$

$t_{SUDAT}$

$t_{HDSTA}$

SCL

$t_{HDSTA}$

$t_{HDDAT}$   $t_{HIGH}$

$t_{SUSTA}$

$t_{SUSTO}$

$t_{LOW}$

$f_{SCL}$
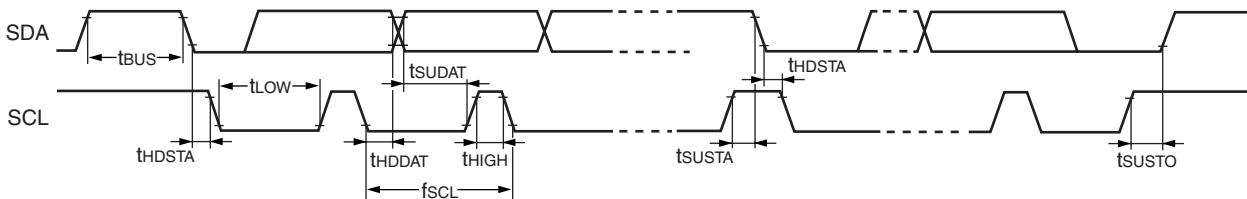
### 5. Electrical Characteristics for the A/D Converter

$(V_{CC} = AV_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40^\circ C \text{ to } +85\,^\circ C)$

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | — | — | ± 3.0 | LSB | |
| Nonlinear error | — | — | — | — | ± 2.5 | LSB | |
| Differential linear error | — | — | — | — | ± 1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN11 | $AV_{SS} - 1.5$ LSB | $AV_{SS} + 0.5$ LSB | $AV_{SS} + 2.5$ LSB | mV | 1 LSB = AVcc/1024 |
| Full-scale transition voltage | $V_{FST}$ | AN0 to AN11 | $AVcc - 3.5$ LSB | $AVcc - 1.5$ LSB | $AVcc + 0.5$ LSB | mV | |
| Conversion time | — | — | 8.64*1 | — | — | µs | |
| Sampling time | — | — | 2 | — | — | µs | |
| Analog port input current | $I_{AIN}$ | AN0 to AN11 | — | — | 10 | µA | |
| Analog input voltage | $V_{AIN}$ | AN0 to AN11 | 0 | — | AVcc | V | |
| Reference voltage | — | AVcc | 3.0 | — | AVcc | V | |
| Power supply current | $I_A$ | AVcc | — | 1.4 | 3.5 | mA | |
| | $I_{AH}$ | AVcc | — | — | 5*2 | µA | |
| Reference voltage supplying current | $I_R$ | AVcc | — | 94 | 150 | µA | |
| | $I_{RH}$ | AVcc | — | — | 5*2 | µA | |
| Interchannel disparity | — | AN0 to AN11 | — | — | 4 | LSB | |

*1 : At operating, main clock 25 MHz.

*2 : If A/D converter is not operating, a current when CPU is stopped is applicable (at Vcc – CPU = AVcc = 3.3 V)

**About the external impedance of analog input and its sampling time>**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relation-ship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. And, if the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input circuit model
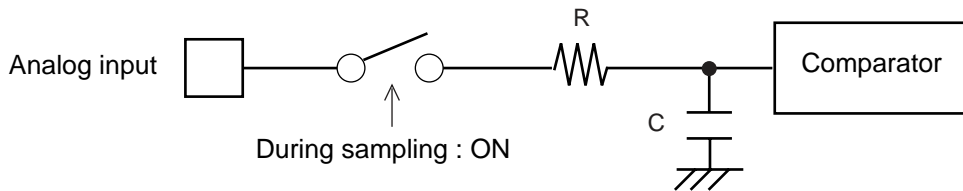


| | R | C |
|---|---|---|
| MB90802 (S)/803 (S) | 1.9 kΩ (Max) | 32.3 pF (Max) |
| MB90F804 | 1.9 kΩ (Max) | 25.0 pF (Max) |
| MB90V800 | 1.9 kΩ (Max) | 32.3 pF (Max) |

Note : The values are reference values.

- The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)

(External impedance = 0 kΩ to 20 kΩ)
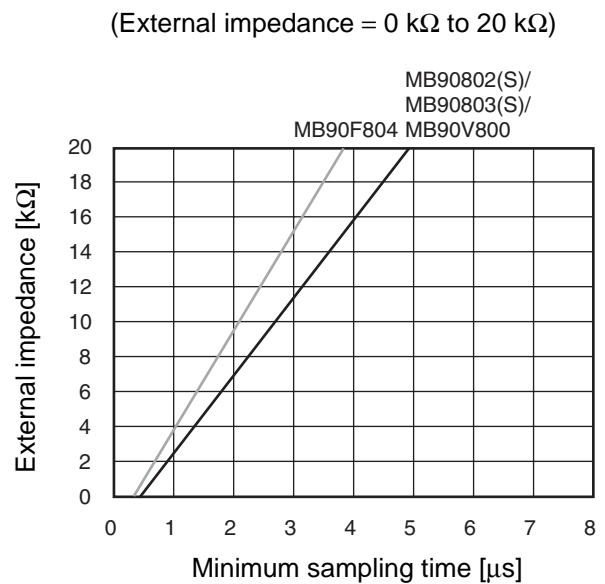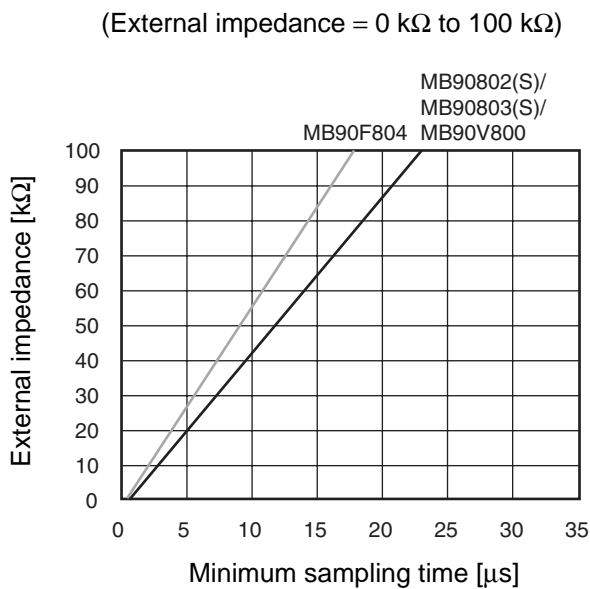


- About errors
  As | AVRH − AV$_{SS}$ | becomes smaller, values of relative errors grow larger.

## 6. Definition of A/D Converter Terms

**Resolution**

Analog variation that is recognized by an A/D converter.

The 10-bit can resolve analog voltage into $2^{10} = 1024$.

**Total error**

This shows the difference between the actual voltage and the ideal value and means a total of error because of offset error, gain error, non-linearity error and noise.

**Linearity error**

Deviation between a line across zero-transition line (00 0000 0000↔00 0000 0001) and full-scale transition line (11 1111 1110↔11 1111 1111) and actual conversion characteristics.

**Differential linear error**

Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.



Total error

Digital output

3FFH
3FEH
3FDH

004H
003H
002H
001H

Actual conversion characteristic

{1 LSB × (N − 1) + 0.5 LSB}

$V_{NT}$
(measurement value)

Actual conversion characteristics

Ideal characteristics

0.5 LSB

0.5 LSB

AVss (AVRL)        Analog input        AVcc (AVRH)
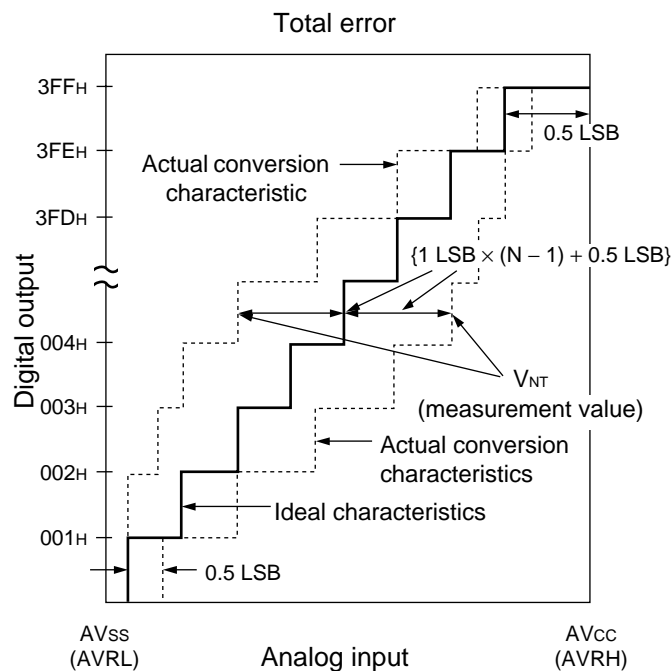
$$\text{Total error of digital output } N = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\text{LSB(Ideal value)} = \frac{AV_{CC} - AV_{SS}}{1024}\ [\text{V}]$$

N : A/D converter digital output value

$V_{OT}$(Ideal value) = $AV_{SS}$ + 0.5 LSB [V]

$V_{FST}$(Ideal value) = $AV_{CC}$ − 1.5 LSB [V]

$V_{NT}$: A voltage at which digital output transitions from (N − 1) to N.

*(Continued)*

*(Continued)*

### Linearity error



### Differential linear error
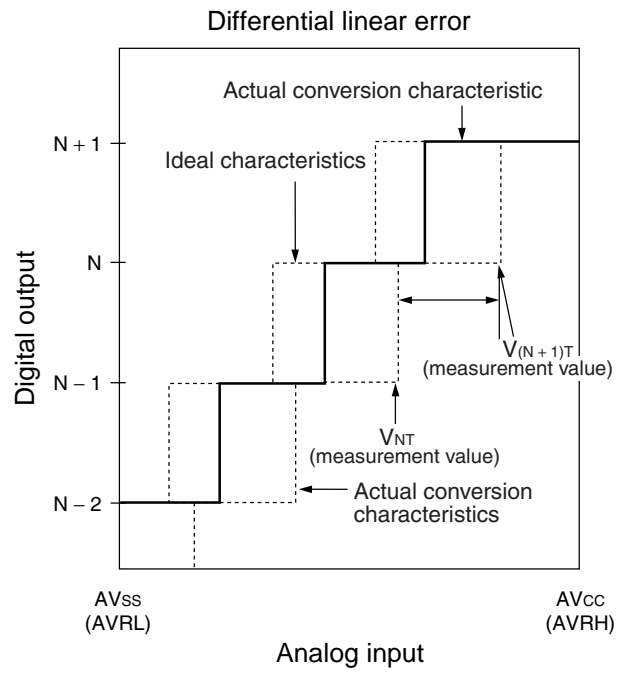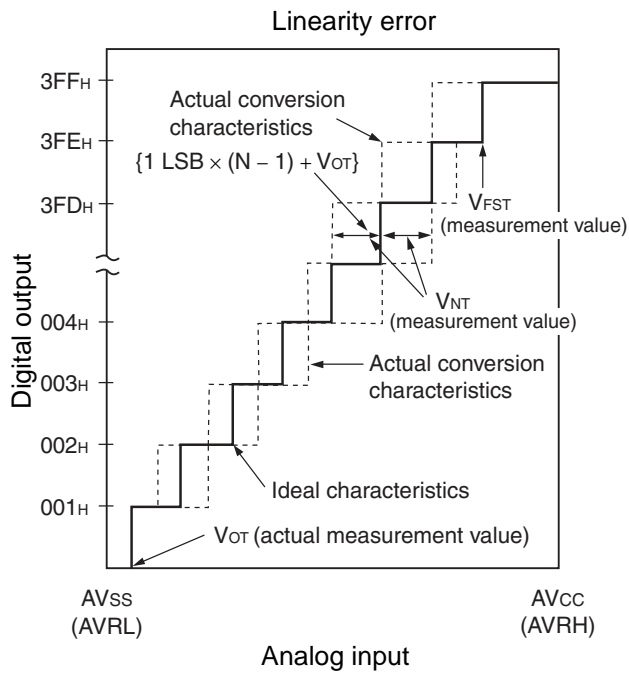


$$\text{Linear error in digital output N} = \frac{V_{NT} - \{1\ LSB \times (N - 1) + V_{OT}\}}{1\ LSB}\ \ [LSB]$$

$$\text{Differential linear error in digital output N} = \frac{V_{(N+1)\,T} - V_{NT}}{1\ LSB}\ - 1LSB\ \ \ \ [LSB]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ \ [V]$$

N : A/D converter digital output value

$V_{OT}$ : Voltage at which digital output transits from $000_H$ to $001_H$.

$V_{FST}$ : Voltage at which digital output transits from $3FE_H$ to $3FF_H$.

## 7. FLASH MEMORY

| Parameter | Conditions | Value | | | Unit | Remarks |
| --- | --- | --- | --- | --- | --- | --- |
| | | **Min** | **Typ** | **Max** | | |
| Sector erase time | $T_A = +25\ °C$ $Vcc = 3.0\ V$ | — | 1 | 15 | s | Excludes 00$_H$ programming prior to erasure. |
| Chip erase time | | — | 9 | — | s | Excludes 00$_H$ programming prior to erasure. |
| Word (16-bit width) programming time | | — | 16 | 3600 | μs | Except for the over head time of the system. |
| Program/erase cycle | — | 10000 | — | — | cycle | |
| Flash memory data retention time | Average $T_A = +85\ °C$ | 20 | — | — | year | * |

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85\ °C$).

# MB90800 Series

■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB90F804-101PF-G<br>MB90F804-201PF-G | 100-pin plastic QFP<br>(FPT-100P-M06) | |
| MB90803PF-G<br>MB90803SPF-G<br>MB90802PF-G<br>MB90802SPF-G | | |

## ■ PACKAGE DIMENSION

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

23.90±0.40(.941±.016)
*20.00±0.20(.787±.008)

80     51
81     50
100    31
1      30

17.90±0.40
(.705±.016)
*14.00±0.20
(.551±.008)

INDEX

0.65(.026)

0.32±0.05
(.013±.002)     ⊕ 0.13(.005) Ⓜ

"A"

⌒ 0.10(.004)

0.17±0.06
(.007±.002)

Details of "A" part

$3.00 ^{+0.35}_{-0.20}$
$(.118 ^{+.014}_{-.008})$
(Mounting height)

0.25(.010)

0~8°

0.80±0.20
(.031±.008)

0.25±0.20
(.010±.008)
(Stand off)

0.88±0.15
(.035±.006)
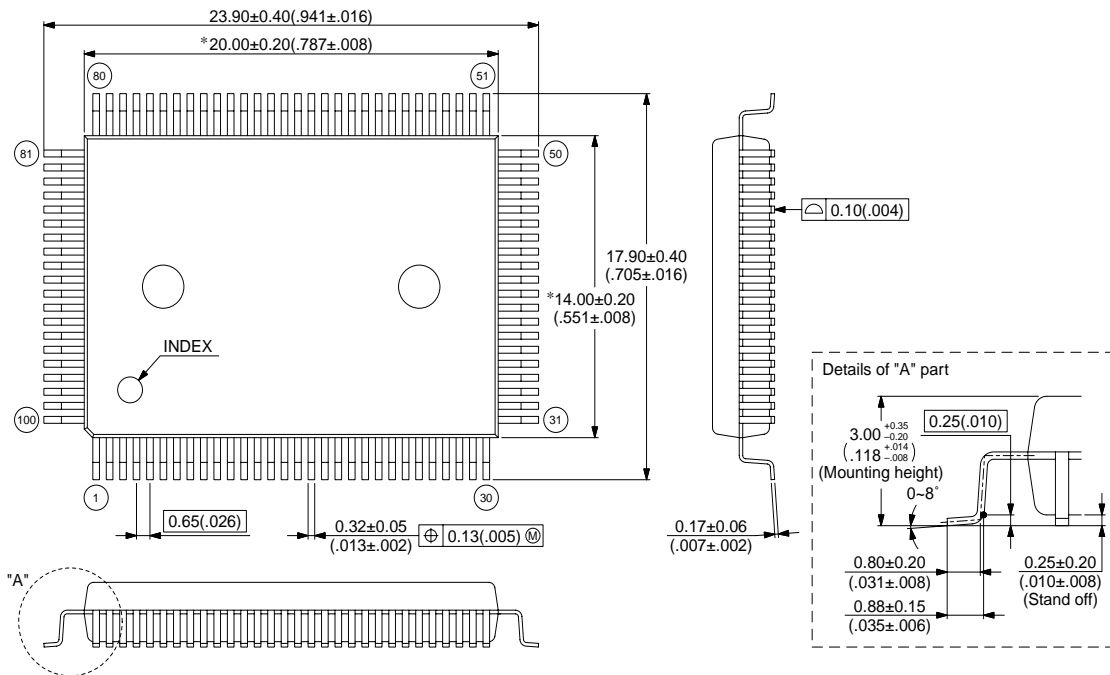
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Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

The information for microcontroller supports is shown in the following homepage.
http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

# FUJITSU LIMITED

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