MOTOROLA

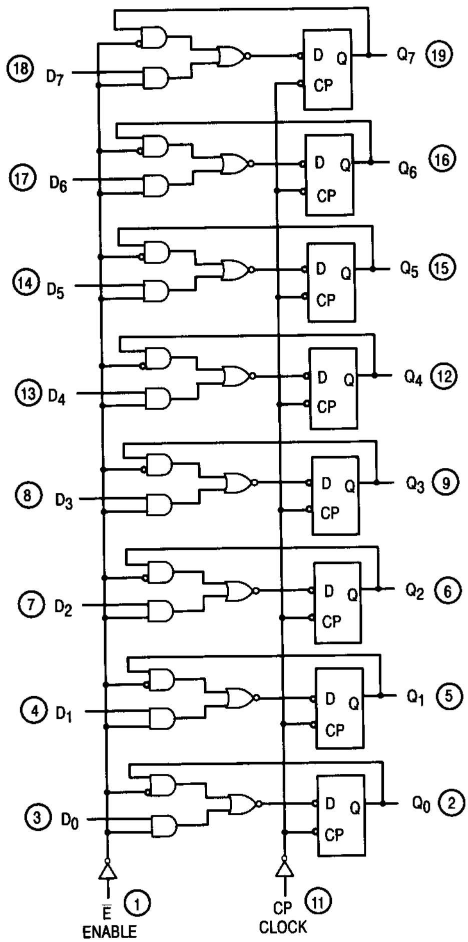
D-Type Flip-Flop With Enable

ELECTRICALLY TESTED PER:
MIL-M-38510/32504

The 54LS377 is an 8-bit register built using advanced Low Power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common clock enable.

- 8-Bit High-Speed Parallel Registers
- Positive Edge-Triggered D-Type Flip-Flops
- Fully Buffered Common Clock and Enable Inputs
- True and Complement Outputs
- Input Clamp Diode Limits High-Speed Termination Effects

LOGIC DIAGRAM



Military 54LS377

AVAILABLE AS:

1) JAN: JM38510/32504BXA
2) SMD: N/A
3) 883: 54LS377/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\overline{E}$	1	1	1	GND
Q_0	2	2	2	V_{CC}
D_0	3	3	3	V_{CC}
D_1	4	4	4	V_{CC}
Q_1	5	5	5	V_{CC}
Q_2	6	6	6	V_{CC}
D_2	7	7	7	V_{CC}
D_3	8	8	8	V_{CC}
Q_3	9	9	9	V_{CC}
GND	10	10	10	GND
CP	11	11	11	CP1
Q_4	12	12	12	V_{CC}
D_4	13	13	13	V_{CC}
D_5	14	14	14	V_{CC}
Q_5	15	15	15	V_{CC}
Q_6	16	16	16	V_{CC}
D_6	17	17	17	V_{CC}
D_7	18	18	18	V_{CC}
Q_7	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	$\uparrow$	X	No Change	No Change
L	$\uparrow$	H	H	L
L	$\uparrow$	L	L	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial

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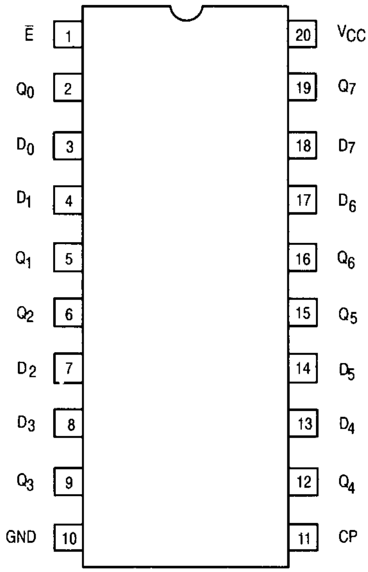
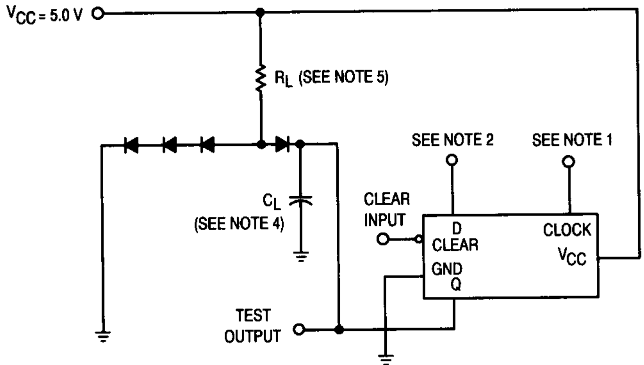
CONNECTION DIAGRAM



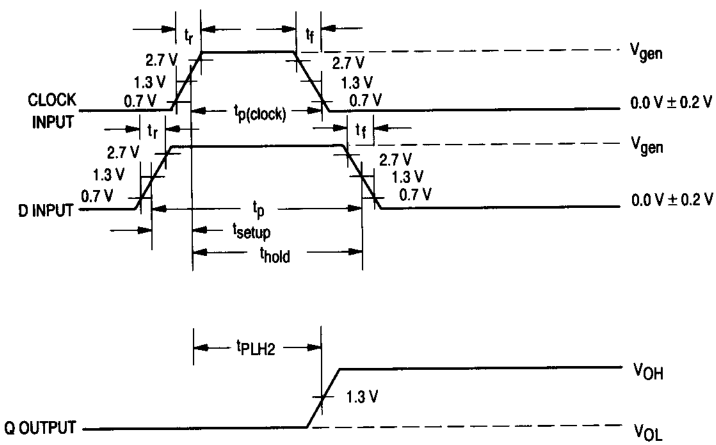
Pin Names		Loading (Note a)	
		HIGH	**LOW**
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
Q_0-Q_3	True Outputs (Note b)	10 U.L.	5(2.5) U.L.
Q_0-Q_3	Complemented Outputs (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) Temperature Ranges.

AC TEST CIRCUIT



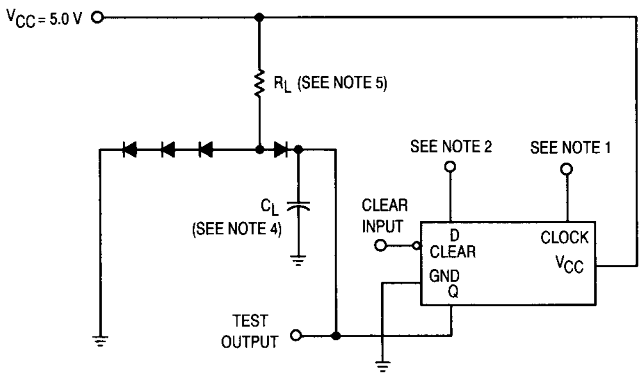
HIGH-LEVEL SWITCHING WAVEFORMS



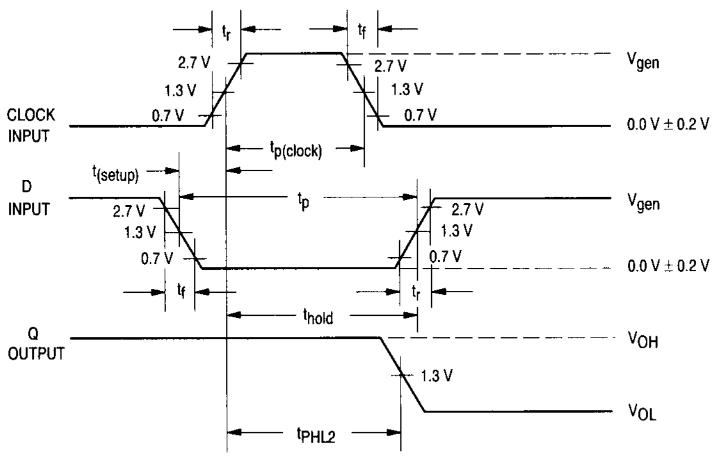
NOTES:

1. Clock input pulse has the following characteristics:
   V_{gen} = 3.0 V ± 0.2 V, $t_r \le$ 15 ns, $t_f \le$ 6.0 ns, $t_{p(clock)}$ = 30 ns, and PRR ≤ 1.0 MHz.
2. D input has the following characteristics:
   V_{gen} = 3.0 V ± 0.2 V, $t_r \le$ 15 ns, $t_f \le$ 6.0 ns, t_{setup} = 20 ns, t_{hold} = 5.0 ns, t_p = 25 ns, and PRR is 50% of the clock PRR.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 kΩ ± 5.0%.

AC TEST CIRCUIT



LOW-LEVEL SWITCHING WAVEFORMS



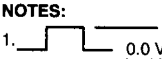
NOTES:

1. Clock input pulse has the following characteristics:
   V_{gen} = 3.0 V ± 0.2 V, t_r ≤ 15 ns, t_f ≤ 6.0 ns, t_p(clock) = 30 ns, and PRR ≤ 1.0 MHz. When testing f_{MAX}, PRR = see table, and $t_0 = t_1$ ≤ 6.0 ns.
2. D input has the following characteristics:
   V_{gen} = 3.0 V ± 0.2 V, t_r ≤ 15 ns, t_f ≤ 6.0 ns, t_{setup} = 20 ns, t_{hold} = 5.0 ns, t_p = 25 ns, and PRR is 50% of the clock PRR. For f_{MAX}, $t_0 = t_1$ ≤ 6.0 ns.
3. All diodes are 1N3064, or equivalent.
4. C_L = 50 pF ± 10% (including jig and probe capacitance).
5. R_L = 2.0 kΩ ± 5.0%.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = – 0.4 mA, V_{IH} = 2.0 V, $\overline{E}$ = 0.7 V, other inputs are open, CLK = (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, $\overline{E}$ = 0.7 V, other inputs are open, CLK = (See Note 1).
V_{IC}	Input Clamping Voltage		– 1.5					V	V_{CC} = 4.5 V, I_{IN} = – 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{OS}	Output Short Circuit Current	– 15	– 100	– 15	– 100	– 15	– 100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, $\overline{E}$ = 0.7 V, CLK = (See Note 2), V_{OUT} = GND.
I_{IL1}	Logical "0" Input Current	– 105	– 345	– 105	– 345	– 105	– 345	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V ($\overline{E}$), other inputs are open.
I_{IL2}	Logical "0" Input Current	– 160	– 400	– 160	– 400	– 160	– 400	µA	V_{CC} = 5.5 V, V_{IL} = 0.4 V, other inputs are open.
I_{CC}	Power Supply Current Off		32		32		32	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs), CLK = (See Note 2).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output High-Low	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output Low-High	5.0 —	32 27	5.0 —	42 37	5.0 —	42 37	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX}	Maximum Clock Frequency	30 30		25		25		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

NOTES:

1.  2.5 V minimum/5.5 V maximum
0.0 V

2.  2.5 V minimum/5.5 V maximum
0.0 V