Le71HE0011
Le78D11 /Le77D11
Evaluation Board, Revision D1 User's Guide

Rev. A, Version 1

March 5, 2003

Document Number: 081081

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CHAPTER

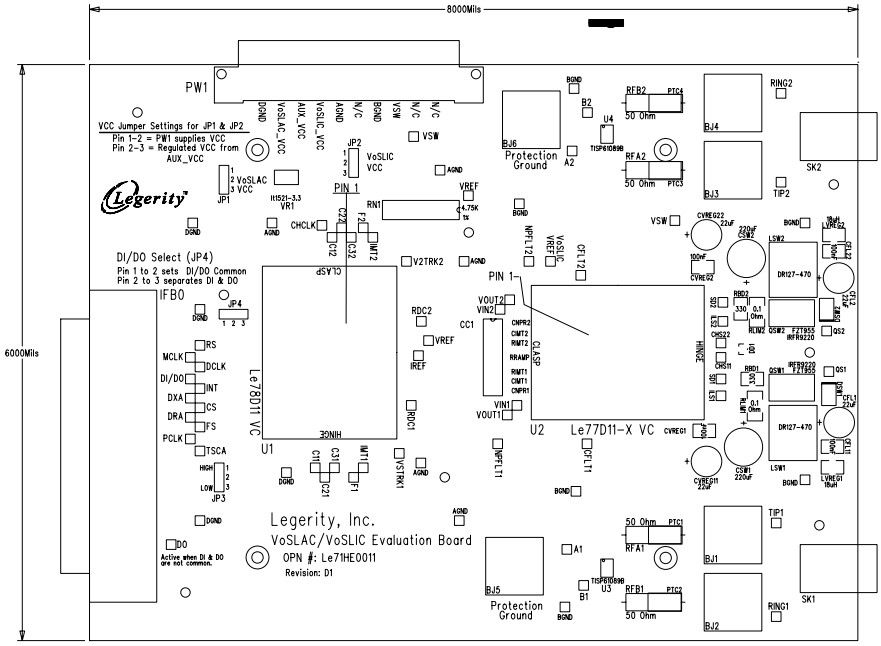
1 INTRODUCTION

1.1 OVERVIEW

The Legerity Le71HE0011 evaluation board provides a platform to evaluate the capabilities of the Le78D11 (rev. A2) and Le77D11 SLIC (rev. BAxx) devices. The evaluation board provides a flexible platform to evaluate both of the device's channels. All digital control signals and voice band signals have test points for easy probing. All user selectable components are mounted on component carriers for easy modification where required. All power is brought to the board via a single keyed connector.

Detailed device explanations, operational circuit descriptions and required formulas can be found within the individual data sheets. Figure 1–1 below shows the physical layout of the Le71HE0011 evaluation board.

Figure 1–1 Le71HE001x Evaluation Board, Rev. D1 Silk-Screen



CHAPTER

2 BOARD SETUP AND CONNECTION

2.1 BOARD FEATURES

The Le71HE0011 evaluation board features the following:

- Four layer board
  - Layer 1: Top routed traces
  - Layer 2: Internal voltage planes (variable 3.3 V/Fixed 3.3 V and VPOS)
  - Layer 3: Internal ground planes (DGND, AGND and BGND)
  - Layer 4: Bottom routed traces

2.2 BOARD MODIFICATIONS

2.2.1 BGND-to-AGND

The BGND-to-AGND connections for the PCB (printed circuit board) is made via the two jumpers located underneath the Le77D11 device socket. The jumpers keep AGND and BGND potentials to within 50 mV of each other.

2.2.2 Surge Protection

The surge protector for the board is the Power Innovations® TISP61089B. The TIP/RING signals are routed through the part. The switcher junction of DSW, CFL and LVREG generates the gating signal for the Power Innovations part. This junction will typically be 8-10 volts above the ringing signal. The two "Protection Ground" banana jacks (BJ5 and BJ6) allow for the surge signal to bypass the BGND plane up to the common BGND connection at PW1. In order for BJ5 to go directly to the PW1 connector the wire jumper, located 0.125 in. to the right of the connector, must be cut and a *short* banana jack must be placed from BJ5 to BJ6.

The VA and VB sense resistors are surface mounted resistors whose values are 243 kΩ and 232 kΩ, respectively.

2.2.3 Unpopulated Components

Components not loaded at assembly time are listed in Table 2–1 below.

Table 2–1 Unpopulated Components

Component	Reason not Loaded
RXA1, RXB1, RXA2, RXB2	Not required
PTC1, PTC2, PTC3, PTC4	Board uses 50 Ω wire wound resistors
CVT1 and CVT2	Not required
CFL11 and CFL22	Not required
CIMT1 and CIMT2	Not required

The FZT953 was changed to a FZT955 due to the higher voltage rating (200 V) of the FZT955. This will facilitate 100 V ringing on the PCB.

2.3 BOARD CONNECTIONS

2.3.1 Power

The power cable (IAV/IAV-DOV) brings all required power to the PCB via the 10-pin header, PW1. The pin out of the cable, and a short description, is provided in Table 2–2.

Table 2–2 PW1 10-Pin Connector Power Cables

Pin #	Signal	Description	Board
1	DGND	Digital ground	DGND
2	+ 3.3 V	Variable V_{CC} supply	VoSLAC_VCC
3	AUX_VCC	Supply for 3.3 V voltage regulator and pull up resistors	AUX_VCC
4	SLIC_VCC	V_{CC} supply for the Le77D11 device	VoSLIC_VCC
5	AGND	Analog ground	AGND
6	RING SOURCE	Not required	N/C
7	BGND	Battery ground	BGND
8	VBP	Positive voltage	VSW
9	VBL	Not required	N/C
10	VBH	Not required	N/C

VCC power to the Le78D11 and Le77D11 devices can be applied in the following ways:

- From a single fixed/variable supply via PW1
- From separate fixed/variable supplies via PW1
- From the on-board 3.3 V regulator VR1 via AUX_VCC
- One device from the fixed/variable supply, the other from VR1

Two jumpers, JP1 and JP2, select how power is applied to the devices (refer to "Jumper Settings" on page 9).

The battery ground plane for the Le77D11 device can be shorted to the AGND plane under the device socket.

2.4 TEST POINTS

The evaluation board contains a total of 74 test points, which are listed in the table below.

Table 2–3 Le71HE0011 Evaluation Board Test Points

Le71HE0011 Test Points				
$C1_1$	$C1_2$	$NPFLT_1$	$NPFLT_2$	QS_1
$C2_1$	$C2_2$	$CFLT_1$	$CFLT_2$	QS_2
$C3_1$	$C3_2$	A_1	A_2	TIP_1
F_1	F_2	B_1	B_2	$RING_1$
IMT_1	IMT_2	ILS_1	ILS_2	TIP_2
$VSTRK_1$	$V2TRK_2$	SD_1	SD_2	$RING_2$
RDC_1	RDC_2	$CHS1_1$	$CHS2_2$	
CHCLK	IREF	VREF (x3)	VSW (x2)	
$VOUT_1$	$VOUT_2$	AGND (x5)	BGND (x6)	
VIN_1	VIN_2	DGND (x4)		
PCM MPI Test Points				
MCLK	DRA [DD][1]	RS	INT [S2][1]	
DCLK [S0][1]	DXA [DU][1]	CS	FS [DCL][1]	
PCLK [FSC][1]	DIO [S1][2]	DO[2]	TSCA [G][1]	

Note:

1. *The bracketed [xx] signal names are for the GCI mode.*
2. *The PCB is designed to allow the Data In (DI) and the Data Out (DO) pins to be tied together and driven as a single line, or to be separated and driven as two independent signals via JP4. Refer to the section on Jumper Settings for a detailed explanation.*

2.5 TELEPHONE LINE INTERFACE

To interface the Le71HE0011 evaluation board to a telephone station set, plug the phone connector into the RJ-11 modular jack (SK1 or SK2). The TIP and RING banana jack pair (BJ1 and BJ2 or BJ3 and BJ4) are connected in parallel with the RJ-11 jack to allow the evaluation board to interface to telephony test equipment as well.

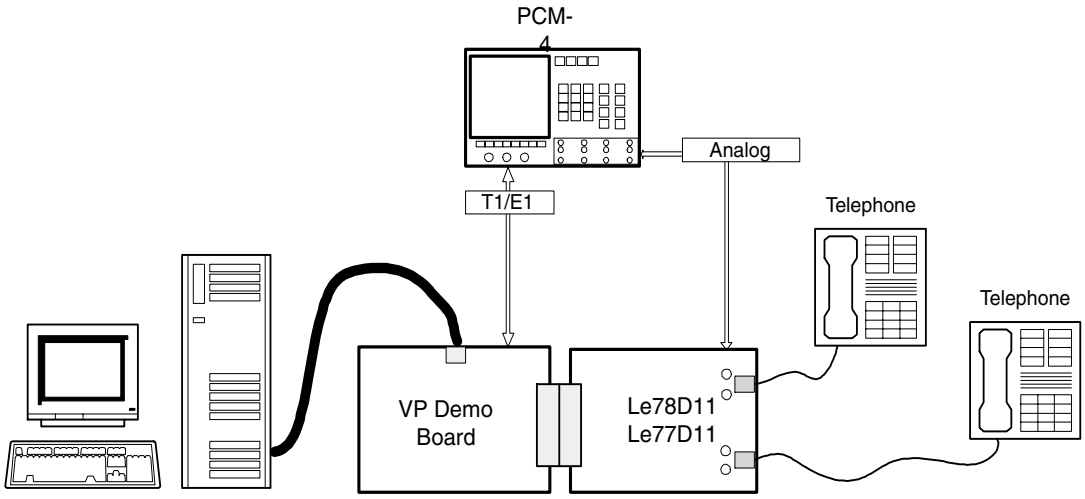
A tip/ring surge protection circuit is included on the board. The protection circuit is placed in line with the A_X and B_X leads of the Le77D11 device and sits between tip and ring resistors (RFA_X and RFB_X) as they connect to the TIP/RING banana jacks. The protection device is a Power Innovations® TISP61089B.

2.6 INTERCONNECTION OF THE LE71HE0011 EVALUATION BOARD

A representative connection of a complete Legerity evaluation platform setup is shown in Figure 2–1 and Figure 2–2 below.

Figure 2–1 shows the evaluation board connected to the 50-pin connector (SPA) of the VP Demo board. The host PC runs the VP-Script Software. Commands are passed through the VP Demo board, via the serial connection of COM1 or COM2, to the evaluation board.

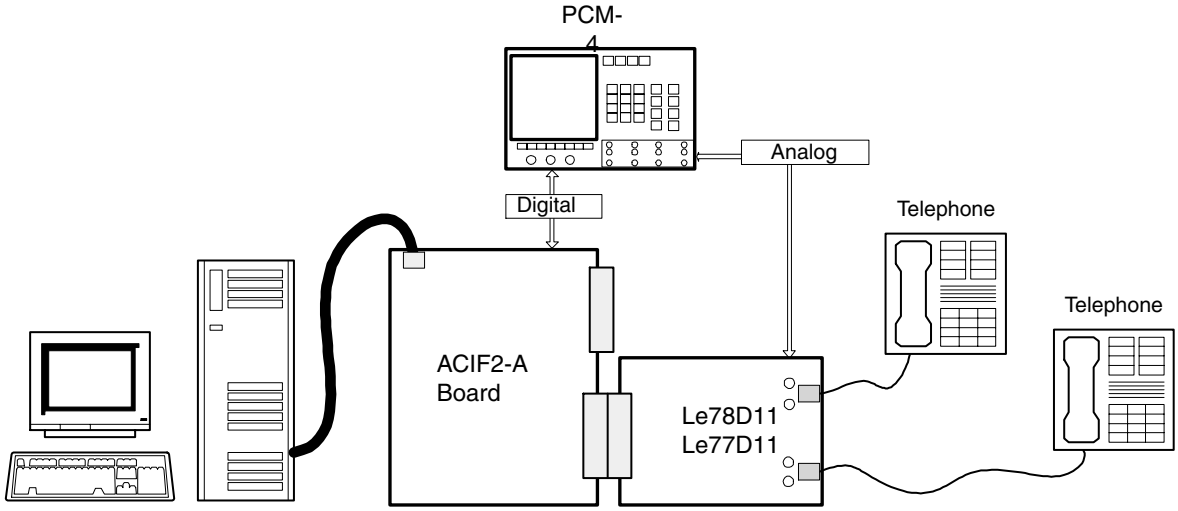
Figure 2–1 Le71HE0011 Evaluation Board Connection Diagram



Analog access to test equipment is connected to the tip/ring connectors of the Le71HE0011 evaluation board. Digital PCM access to test equipment is provided through the VP Demo Board.

Figure 2–2 shows the evaluation board connected to the 50-pin connector LNB#0 of the ACIF2-A Board. The host PC runs the WinACIF Software. Commands are passed through the ACIF2-A board, via the serial connection of COM1 or COM2, to the evaluation board.

Figure 2–2 Le71HE0011 Evaluation Board Connection Diagram



Analog access to test equipment is connected to the tip/ring connectors of the Le71HE0011 evaluation board. Digital PCM access to test equipment is provided through the ACIF2-A board.

2.7 PCM/MPI CONNECTIONS

All PCM/MPI interface signals are passed through the IFB0 connector. The three clock signals — MCLK, PCLK and DCLK — have guard band traces running along side the clock signals and are routed on the top layer of the evaluation board. All other PCM/MPI signals are routed on the bottom of the evaluation board. Table 2–4 shows the PCM/MPI connections.

Table 2–4 PCM/MPI Connections

Pin #	Signal	Pin #	Signal
1	RS	26	Digital Ground
2	MCLK	27	Digital Ground
3	DCLK	28	Digital Ground
4	N/C	29	Digital Ground
5	DI/DO	30	Digital Ground
6	INT	31	Digital Ground
7	DXA	32	Digital Ground
8	CS	33	Digital Ground
9	DRA	34	Digital Ground
10	N/C	35	Digital Ground
11	FS	36	Digital Ground
12	PCLK	37	Digital Ground
13-24	N/C	38-50	Digital Ground
25	DO		

The Le71HE0011 evaluation board has separate pins for the data in (DI) and the data out (DO). A single jumper (JP4) on the PCB allows the user to either make the two signals common (DIO) or separate them. Refer to "Jumper Settings" on page 9 for specific details. Also, refer to the Le78D11 device schematic page in "Evaluation Board Schematics" on page 15 for specific pin connections to the IFB0 connector.

CHAPTER

3 BOARD OPERATION AND CONTROL

3.1 SWITCHER CONFIGURATIONS

The Le71HE0011 evaluation board is designed to operate with a bipolar switcher configuration.

3.2 JUMPER SETTINGS

3.2.1 JP1 and JP2

Jumpers JP1 and JP2 configure the VoSLAC_VCC and VoSLIC_VCC applied to the devices to come from either an external variable power supply, via the PW1 connector, or from the on-board voltage regulator (VR1) which is powered by AUX_VCC. Table 3–1 below details the settings.

Table 3–1 JP1 and JP2 Jumper Settings

Jumper Row	Pins	Description
JP1	1-2	Sets the Le78D11 device voltage to be supplied from the PW1 VoSLAC_VCC input
JP1	2-3	Sets the Le78D11 device voltage to be supplied from the AUX_VCC via VR1
JP2	1-2	Sets the Le77D11 device voltage to be supplied from the PW1 VoSLIC_VCC input
JP2	2-3	Sets the Le77D11 device voltage to be supplied from AUX_VCC via VR1

3.2.2 JP3

The JP3 jumper has a dual purpose depending on the mode the Le78D11 device is set to operate in. In the PCM mode, JP3 will need to be set to pull the TSCA output pin high since TSCA, in the PCM mode, is an open-drain signal that is fed back to the ACIF2-A or VP demo board. In the GCI mode, this pin becomes the G input which can be strapped High or Low via the jumper. If JP3 is set to the HIGH position on the board the G pin can be programmed via the ACIF2-A board.

Table 3–2 JP3 Jumper Settings

Jumper Row	Pins	Description
PCM Mode		
JP3	1-2	Allows the TSCA condition to be monitored via the ACIF2-A board.
GCI Mode		
JP3	1-2	Straps the G input HIGH (logic 1). Not applicable in the VP demo board.
JP3	2-3	Straps the G input LOW (logic 0). Not applicable in the VP demo board.

3.2.3 JP4

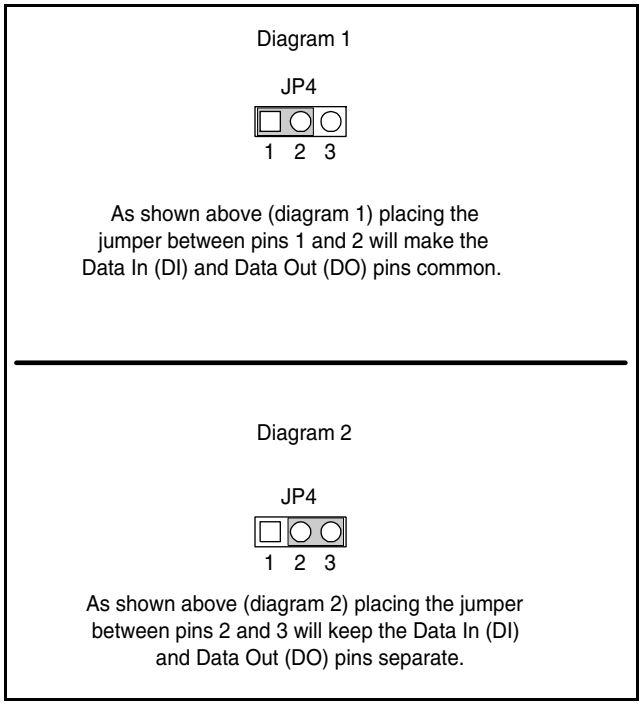
Jumper JP4 selects whether the DI and DO pins of the Le78D11 device are common to each other or are separate inputs.

Table 3–3 JP4 Jumper Settings

Jumper Row	Pins	Description
JP4	1-2	Shorts DI and DO together to allow them to be driven via a single source.
JP4	2-3	Separates DI and DO to allow the pins to be driven by separate sources. (default setting)

The DI (DATA IN) pin is connected directly to pin 5 of the IFB0 connector and to pin 1 of JP4. The DO (DATA OUT) pin is connected *only* to connected to pin 2 of JP4. The DO connection from pin 25 of the IFB0 connector is routed to JP4 pin 3. The diagram below details both settings for JP4.

Figure 3–1 JP4 Jumper Settings



When using the VP Demo Board, the setting will be diagram 2 (Data In and Data Out separate). This will set the evaluation board to be compatible with the startup configuration of the VP-Script and Mini-PBX software.

When using the ACIF2-A Board, the setting will be diagram 1 (Data In and Data Out common). This will set the evaluation board to be compatible with the startup configuration of the WinACIF software.

3.3 COMPONENT CARRIERS

The Le71HE0011 evaluation board has two headers on it, RN1 and CC1. RN1 holds the resistor network that is used to improve the accuracy of the IDC, VA, VB and VBAT readings. The Le78D11 device has a register that can be programmed to use the external resistors. The reference voltage for the external resistors is VREF. The resistors are optional and not populated.

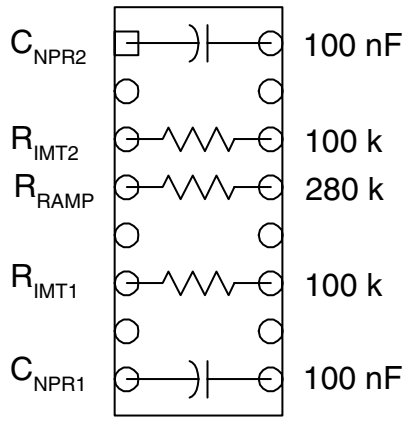
Table 3–4 details the components placed on CC1 when the Le77D11 device is configured for bipolar operation:

Table 3–4 CC1 Components

Component	Description
$CNPR_X$	This capacitor determines the polarity reversal time.
RRAMP	This resistor controls ramp rate for bipolar operation.
$RIMT_X/CIMT_X$	This resistor and capacitor sets the 2-wire impedance (Z_{2WIN}), 4-wire to 2-wire gain (G_{42}) and 2-wire to 4-wire gain (G_{24})

Figure 3–2 below illustrates the positioning of the components on the CC1 header. It must also be noted the 600 Ω and 900 Ω stated below are for the Le77D11 device only, not the whole board.

Figure 3–2 CC1 Component Carrier Values



The value of R_{IMT1} and R_{IMT2} will change depending on load resistance (refer to Table 3–5).

Table 3–5 R_{IMT1} and R_{IMT2} Resistors Values

R_{LOAD}	R_{IMT1} and R_{IMT2} Value
600 Ω	100 k
900 Ω	133 k

CHAPTER

4 SOFTWARE OPERATION

4.1 OVERVIEW

Two control platforms allow the user to communicate with the Le71HE0011 evaluation board. The first platform is the VoicePath demo board and the VP-Script program or the VoicePath Mini-PBX software. The second platform is the ACIF2-A hardware board along with its accompanying WinACIF software program. A third software program, WinSLAC2™ software, is used to calculate the required coefficients needed by the Le77D11/Le78D11 chip set.

The WinSLAC2 software models the Le77D11/Le78D11 chip set, calculates programmable coefficients for optimizing two-wire impedance, hybrid balance and transmit and receive responses. WinSLAC2 also calculates and predicts transmission performance for:

- Two-Wire Return Loss
- Four-Wire Return Loss
- Transmit and receive attenuation distortion
- Transmit and receive path equalization
- Two-wire stability

For a more detailed description refer to the *WinSLAC2 Software User's Guide*, document ID #080779.

The VoicePath demo board is one of the control platforms that can be used for communicating with the evaluation board. The VP-Script program uses a command menu to send information to and receive information from the evaluation board (supports PCM mode only). Refer to the *VP-Script Software User's Guide*, document ID #080757, for more detailed information.

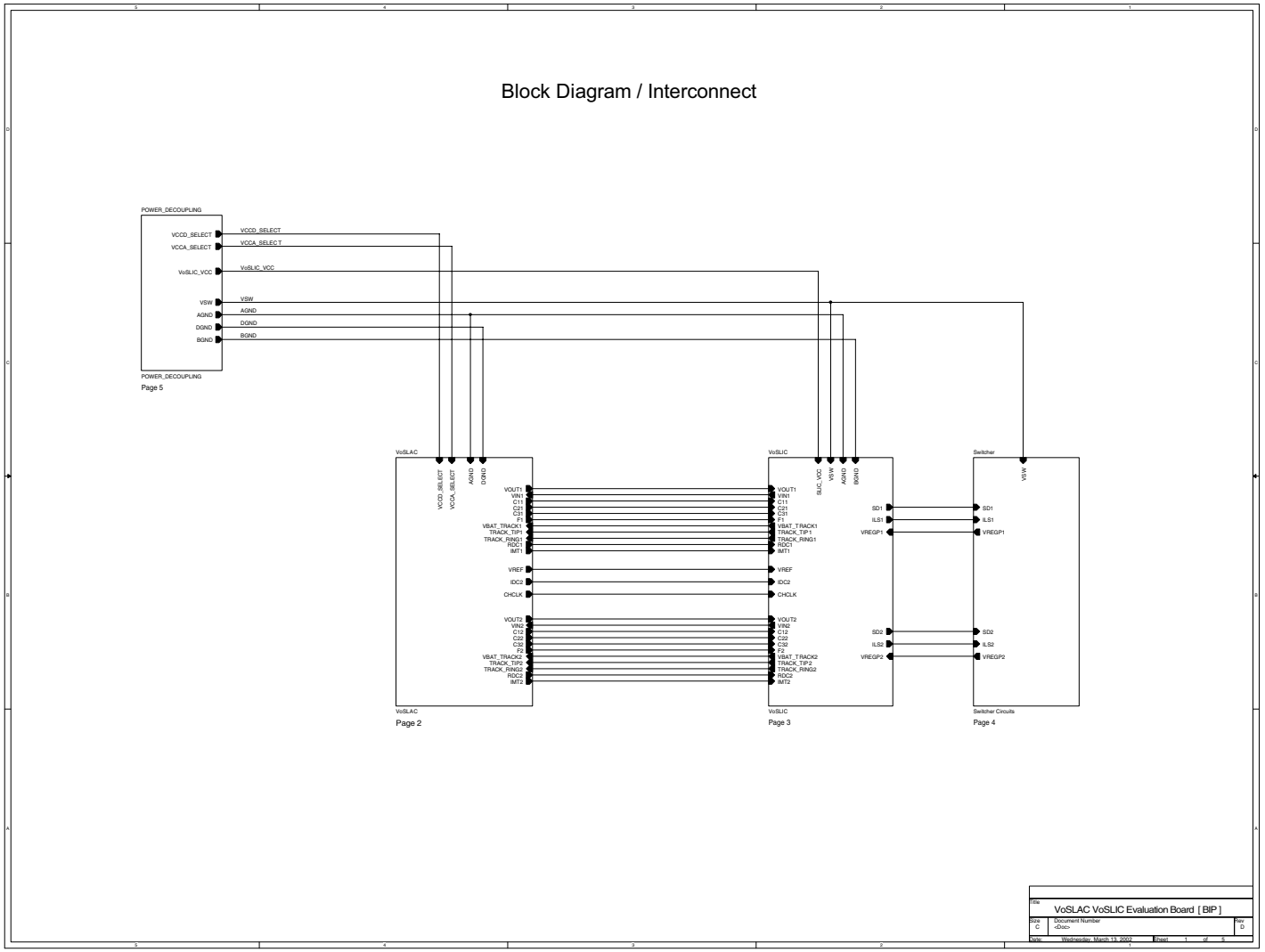
The ACIF2-A hardware board and the WinACIF Software are an alternate platform that can be used to communicate with the chip set. Once the software has been initialized with the correct chip set configuration, a command menu is used to send information to and receive information from the Le77D11/Le78D11 chip set (supports PCM and GCI modes). Refer to the *WinACIF User's Guide*, document ID #080269, for more detailed information.

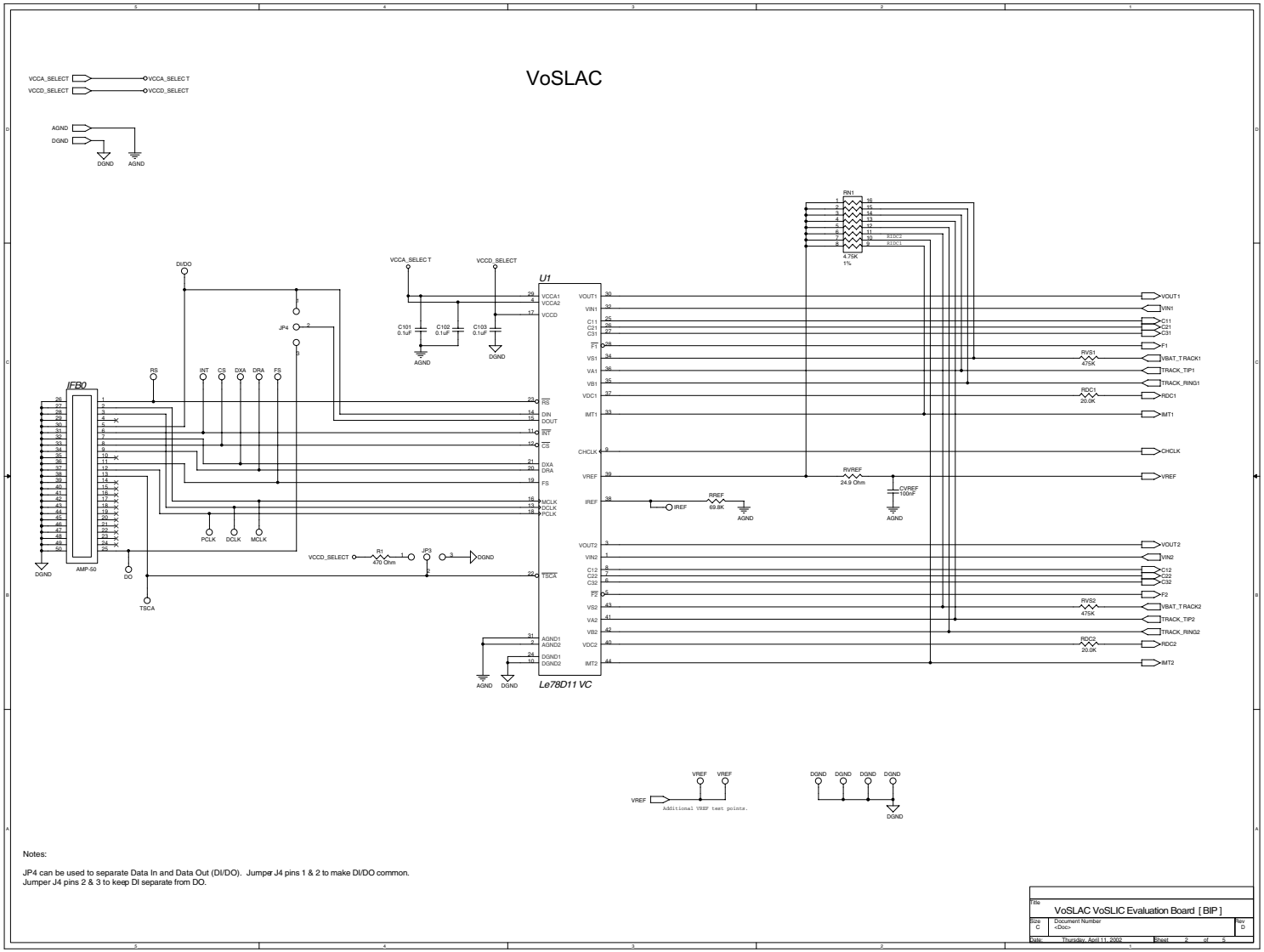
CHAPTER

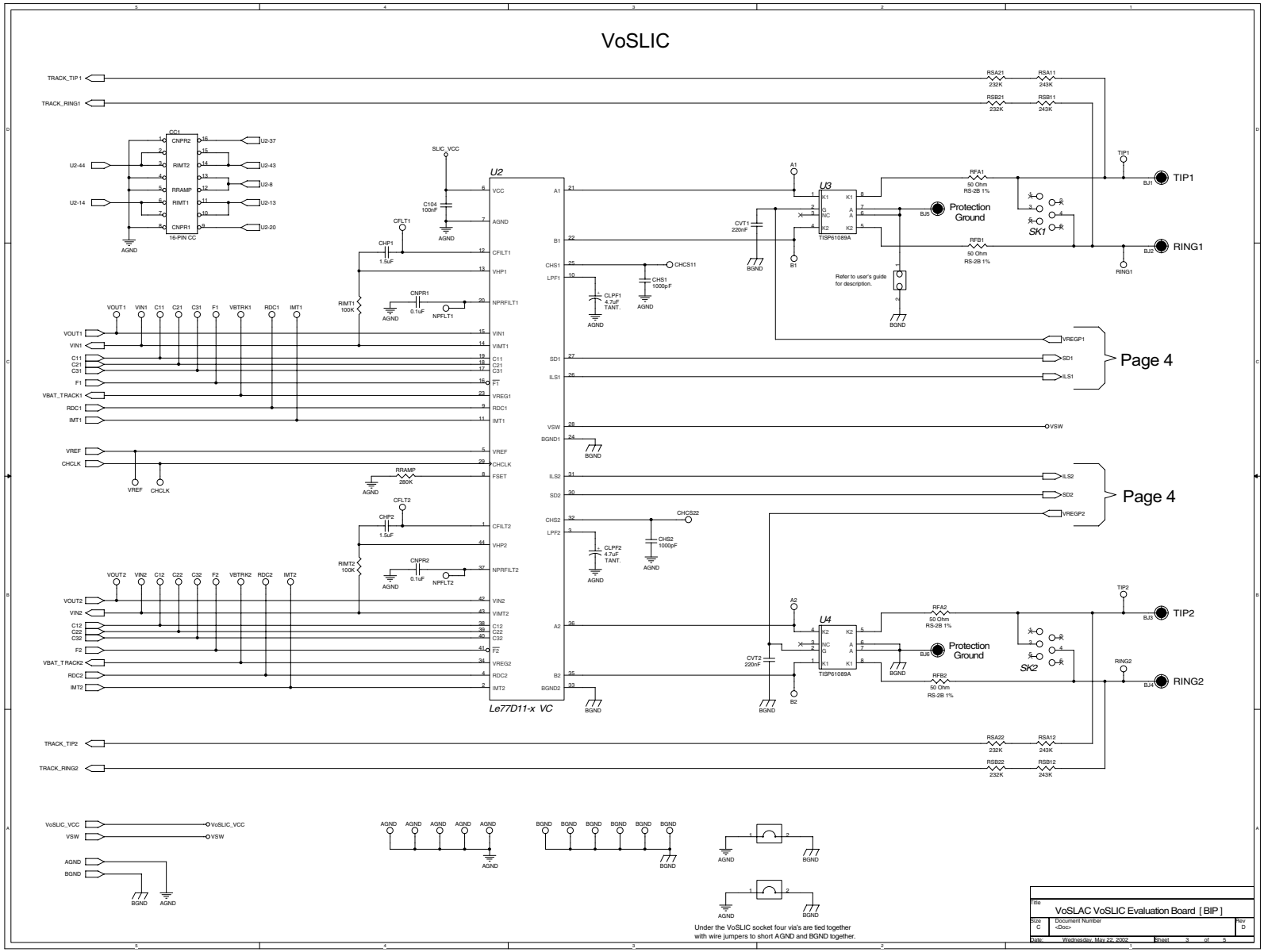
5 EVALUATION BOARD SCHEMATICS

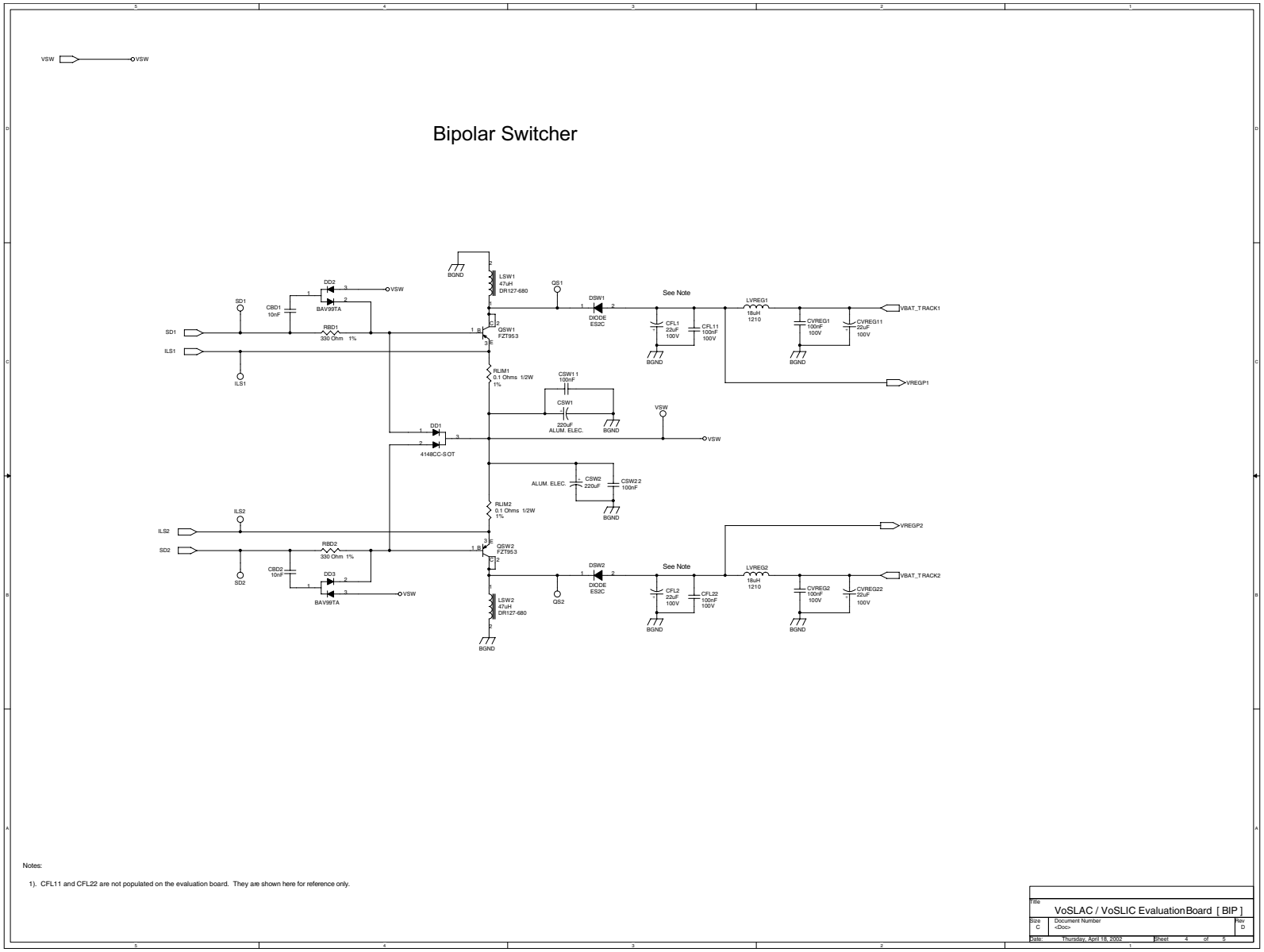
5.1 EVALUATION BOARD SCHEMATICS

A bill of materials and schematic for the Le77D11/Le78D11 bipolar configuration are included on the following pages.


Block Diagram / Interconnect
POWER_DECOUPLING
VCCD_SELECT
VCCA_SELECT
VoSLIC_VCC
VSW
AGND
DGND
BGND
Page 5
VoSLAC
Page 2
VoSLIC
Page 3
Switcher
Switcher Circuits
Page 4
VoSLAC VoSLIC Evaluation Board [BIP]
Wednesday, March 13, 2002


VoSLAC
VCCA_SELECT
VCCD_SELECT
AGND
DGND
DI/DO
JP4
C101 0.1uF
C102 0.1uF
C103 0.1uF
U1
Le78D11 VC
IFB0
AMP-50
DO
TSCA
PCLK
DCLK
MCLK
R1 470 Ohm
JP3
RN1 4.75K 1%
RVS1 475K
RDC1 20.0K
RVREF 24.9 Ohm
CVREF 100nF
RREF 69.8K
IREF
RVS2 475K
RDC2 20.0K
VOUT1
VIN1
C11
C21
C31
F1
VBAT_TRACK1
TRACK_TIP1
TRACK_RING1
RDC1
IMT1
CHCLK
VREF
VOUT2
VIN2
C12
C22
C32
F2
VBAT_TRACK2
TRACK_TIP2
TRACK_RING2
RDC2
IMT2
Additional VREF test points.
Notes:
JP4 can be used to separate Data In and Data Out (DI/DO). Jumper J4 pins 1 & 2 to make DI/DO common.
Jumper J4 pins 2 & 3 to keep DI separate from DO.
VoSLAC VoSLIC Evaluation Board [BIP]
Document Number
<Doc>
Thursday, April 11, 2002

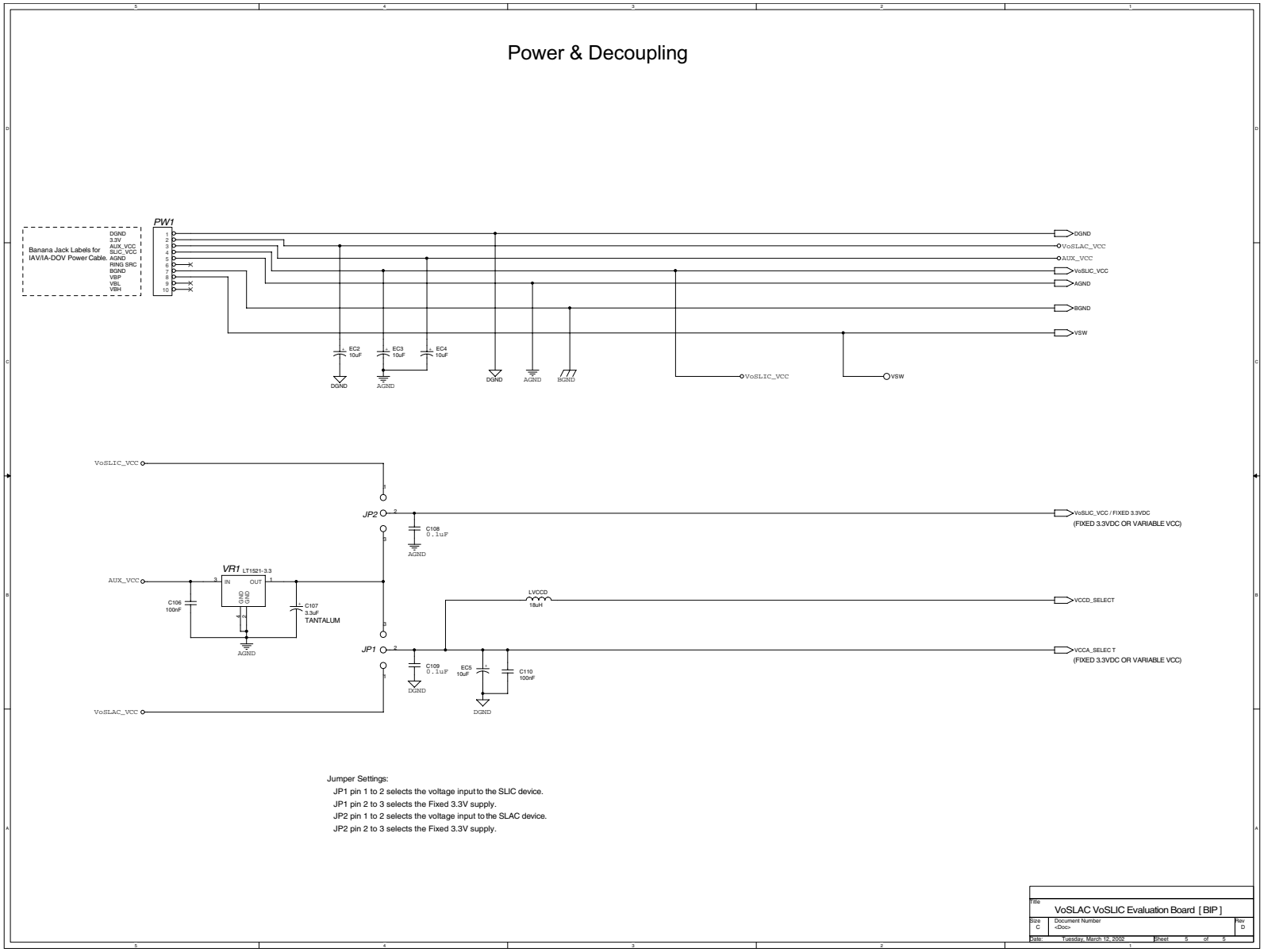

VoSLIC
TRACK_TIP 1
TRACK_RING1
U2
Le77D11-x VC
U3
U4
TISP61089A
Protection Ground
TIP1
RING1
TIP2
RING2
Page 4
Page 4
SK1
SK2
Refer to user's guide for description.
Under the VoSLIC socket four via's are tied together with wire jumpers to short AGND and BGND together.
Title
VoSLAC VoSLIC Evaluation Board [BIP]
Size C
Document Number <Doc>
Rev D
Date: Wednesday, May 22, 2002
Sheet 3 of 5



Notes:

1). CFL11 and CFL22 are not populated on the evaluation board. They are shown here for reference only.

Title	VoSLAC / VoSLIC Evaluation Board [BIP]	
Size: C	Document Number: <Doc>	Rev: D
Date: Thursday, April 18, 2002	Sheet 4 of 5	


Power & Decoupling
PW1
Banana Jack Labels for IAV/IA-DOV Power Cable.
DGND
3.3V
AUX_VCC
SLIC_VCC
AGND
RING SRC
BGND
VBP
VBL
VBH
EC2 10uF
EC3 10uF
EC4 10uF
VoSLIC_VCC
VSW
JP2
C108 0.1uF
VoSLIC_VCC / FIXED 3.3VDC
(FIXED 3.3VDC OR VARIABLE VCC)
VR1 LT1521-3.3
IN
OUT
C106 100nF
C107 3.3uF TANTALUM
LVCCD 18uH
VCCD_SELECT
JP1
C109 0.1uF
EC5 10uF
C110 100nF
VCCA_SELEC T
(FIXED 3.3VDC OR VARIABLE VCC)
Jumper Settings:
JP1 pin 1 to 2 selects the voltage input to the SLIC device.
JP1 pin 2 to 3 selects the Fixed 3.3V supply.
JP2 pin 1 to 2 selects the voltage input to the SLAC device.
JP2 pin 2 to 3 selects the Fixed 3.3V supply.
VoSLAC VoSLIC Evaluation Board [BIP]
Document Number
<Doc>
Tuesday, March 12, 2002

5.2 BILL OF MATERIALS

VoB Bipolar Evaluation Board
Revision: D1

Part Type	SM Size / TH Spacing	Voltage / Tol.	SM / TH	Qty	Designation	Vendor / Part Number
Capacitors						
1nF Ceramic	0805	50V / 10%	SM	2	CHS1, CHS2	Panasonic / ECJ-2VC1H102J
10nF Ceramic	1206	16V / 10%	SM	2	CBD1, CBD2	Panasonic / ECJ-3VC1C103K
100nF Ceramic	0805	16V / 10%	SM	9	C101, C102, C103, C104, C106, C108, C109, C110, CSW11, CSW22, CVREF	Panasonic / ECJ-1VC1C104K
100nF Ceramic	1210	100V / 10%	SM	2	CFL11, CFL22	DO NOT POPULATE (Nova Cap / 1206B104J101N)
100nF Ceramic	1210	100V / 10%	SM	2	CVREG1, CVREG2	Kemet / C1210C104K1RAC
1.5uF Ceramic	0805	6.3V / 10%	SM	2	CHP1, CHP2	Panasonic / ECJ-2YB0J155K (DIGI-KEY / PCC1921CT-ND)
3.3uF Tantalum	3528	16V / 10%	SM	1	C107	Kemet / T491B335K016AS
4.7uF Tantalum	3216	10V / 10%	SM	2	CLPF1, CLPF2	Kemet / T491A475K010AS
10uF Tantalum	3528	16V / 10%	SM	4	EC2, EC3, EC4, EC5	Kemet / T491B106K016AS
22uF Alum. Elect.	0.1"	100V / 10%	TH	4	CFL1, CFL2, CVREG11, CVREG22	Panasonic / EEUFC2A220 (DIGI-KEY / P10770-ND)
220uF Alum. Elect.	0.2"	50V / 20%	TH	2	CSW1, CSW2	Nichicon / UPW1H221MPH
Transistors						
FZT955 200V PNP	SOT223	200V	SM	2	QSW1, QSW2	Zetex / FZT955
Diodes						
ES2C	DO-214AA		SM	2	DSW1, DSW2	General Semi. / ES2C DIODES inc. ES2C/A
4148-SOT	SOT23		SM	1	DD1	Fairchild / MMBD4148CC
BAV99TA	SOT23		SM	2	DD2, DD3	Zetex / BAV99TA (DIGI-KEY # BAV99ZXTR-ND)
Inductor						
47uH			SM	2	LSW1, LSW2	Cooper Coiltronics / DR127-470 or COEV / DQ1280-470
18uH	1210		SM	3	LVREG1, LVREG2, LVCCD	Panasonic / ELJ-PA180KF (DIGI-KEY # PCD1487CT-ND)
PTC						
MZ2			TH	4	PTC1, PTC2, PTC3, PTC4	Do Not Populate
Resistors						
0.1 Ohm	1210		SM	2	RLIM1, RLIM2	Vishay / CRCW1210R100JNTALR (SAP #) (Arrow 231-5433)
0.0 Ohm	1206		SM	1	RVREF	DIGI-KEY / 311-0.0ECT-ND
50 Ohm 1% RS-2B	TH		TH	4	RFA1, RFB1, RFA2, RFB2	Vishay / RS-2B-50-1% [Newark / 02F1195]
330 Ohm 1%	1210		SM	2	RBD1, RBD2	Vishay / CRCW1210P330F25RT6
470 Ohm 1%	1206		SM	1	R1	DIGI-KEY P470ECT-ND
20.0K 1%	1206		SM	2	RDC1, RDC2	DIGI-KEY / P20.0KFCT-ND
69.8K 1%	1206		SM	1	RREF	DIGI-KEY / P69.8KFCT-ND
232K 1%	1206		SM	4	RSA21, RSB21, RSA22, RSB22	DIGI-KEY / P232KFCT-ND
243K 1%	1206		SM	4	RSA11, RSB11, RSA12, RSB12	DIGI-KEY / P243KFCT-ND
475K 1%	1206		SM	2	RVS1, RVS2	DIGI-KEY / P475KFCT-ND
Component Carrier Parts						
100nF Ceramic	0.2"	50V / 10%	TH	2	CNPR1, CNPR2 (See attached diagram.)	Kemet / C320C104K5R5CA
4.75K 1% 1/4W	TH		TH		RN1 thru RN8 (See attached diagram.)	Do Not Populate
100K 1% 1/4W	TH		TH	2	RIMT1, RIMT2 (See attached diagram.)	DIGI-KEY / 100KXBK-ND
280K 1% 1/4W	TH		TH	1	RRAMP (See attached diagram.)	DIGI-KEY / 280KXBK-ND
I.C.'s						
Le78D11 VC (VoSLAC)	44 TQFP		SM	1	U1	Legerity will provide these
Le77D11-x VC (VoSLIC)	44 TQFP EPADD		SM	1	U2	Legerity will provide these
LT1521-3.3	SOIC		SM	1	VR1	Marshall / LT1521CST-3.3 (Linear Technologies)
TISP61089B	SOIC		SM	2	U3, U4	Power Innovations / TISP61089B
Sockets						
44-pin TQFP			TH	2	U1, U2	Yamaichi / QFP11T044-001
16-pin DIP			TH	2	CC1, RN1	Samtec / ICO-316-NTT
Connectors						
AMP Champ 50-pin			TH	1	IFB0	Newark / 90F4961 [AMP 552726-1]
AMP 10-pin header			TH	1	PW1	Newark / 52F3052 [AMP 207398-1]
Banana Jack Red			TH	2	BJ1, BJ3	Newark / 39N868
Banana Jack Green			TH	2	BJ2, BJ4	Newark / 39N870
Banana Jack Black			TH	2	BJ5, BJ6	Newark / 39N869
Test Points			TH	72	RS, DI/DO, INT, CS, DXA, DRA, FS, PCLK, DCLK, MCLK, TSCA, IREF, CHCLK, VOUT1, VIN1, C11, C21, C31, F1, VBTRK1, RDC1, IMT1, CFLT1, NPFLT1, VREF (x3), CFLT2, NPFLT2, VOUT2, VIN2, C12, C22, C32, F2, VBTRK2, RDC2, IMT2, CHS11, A1, B1, TIP1, RING1, QS1, SD1, ILS1, VSW(x2), ILS2, QS2, SD2, CHS22, A2, B2, TIP2, RING2, AGND(x5), BGND(x6), DGND(x4), DO	Mouser / 151-205
16-pin Component Carriers			TH	2	CC1, RN1	Samtec / APO-316-T-C or APA-316-T-C
6-pin RJ11			TH	2	SK1, SK2	Newark / 87N981
1x3 Jumper			TH	4	JP1, JP2, JP3, JP4	Legerity will provide these
2 position shunt				4	N/A	Samtec / SNT-100-YW-T
Hardware						
3/4" Nylon standoff 4/40			TH	8	N/A	Newark / 30F1466
3/8" machine screw 4-40			TH	12	N/A	Newark / 30F082
4-40 Nylon nut 4/40 thread			TH	4	N/A	Newark / 50N5869

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